A 3GS/s 6-Bit Bipolar Flash ADC in 0.25 μm

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Abstract

We report on a flash Analog to Digital Converter (ADC) at 3 Giga samples per second (GS/s) which was developed using QUBIC4X: a 0.25 μm SiGeC process from NXP semiconductor. The ADC has a bandwidth of 1.5 GHz and a resolution of 6-bits. The design employs a differential structure. The ADC uses a parallel architecture consisting of the following components: track and hold, comparators, and a fat tree encoder. A system test validated the test bench, and an additive scrambler was used to eliminate long sequences consisting entirely of 0 or 1 . The core of the digital circuit is in Emitter-Coupled Logic (ECL). The input is adapted to 100 Ω differential, and the outputs use standard Low Voltage Differential Signaling (LVDS). The operating voltage is 0.5 Volts. The complete system has a power consumption of 2.6 Watts and the Effective Number of Bits (ENOB) is higher than 5 at Nyquist frequency (1500 MHz).

INTRODUCTION

Heterodyne receivers have generally been used in radio astronomy to bring high frequencies down to frequencies which can be directly treated by digital processing systems. Such a system has its associated complexity (see e.g. Fig: 1a) and an important goal is to do away with the heterodyne mixing, and instead to process directly the received frequency (RF) of the radio receiver. In order to dramatically reduce the system complexity, the goal is to acquire the whole frequency band between 300 MHz and 1.5 GHz (UHF-L band) using only one receiver (Fig: 1b). [1, 2].

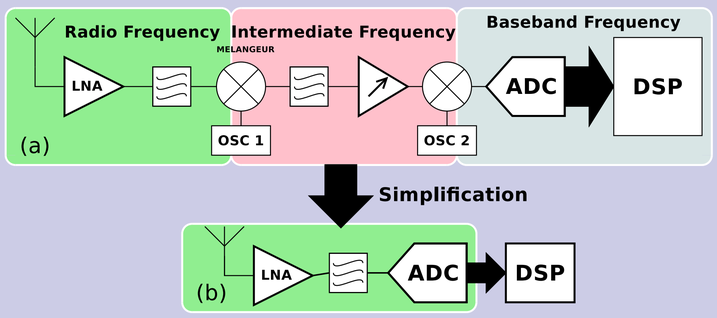

Figure 1: a. heterodyne receiver on L-band ($ADC << 1GS/s$) b. Radio receiver simplified L-band ($ADC > 3GS/s$)

ADC REQUIREMENTS

High sampling rate (< 3 GS/s)
Minimum bandwidth of 1.4 GHz
6-bit ADC

ADC ARCHITECTURE

Our flash ADC is composed of the following stages (Fig: 2): a track and hold (T/H), comparators, a bubble correction, a fat tree encoder, and a scrambler. A test board was constructed in order to validate the behaviour of the chip. Each block is fabricated in differential bipolar technology. The digital part is based on Emitter-Coupled Logic (ECL) and Current Mode Logic (CML) [3, 4].

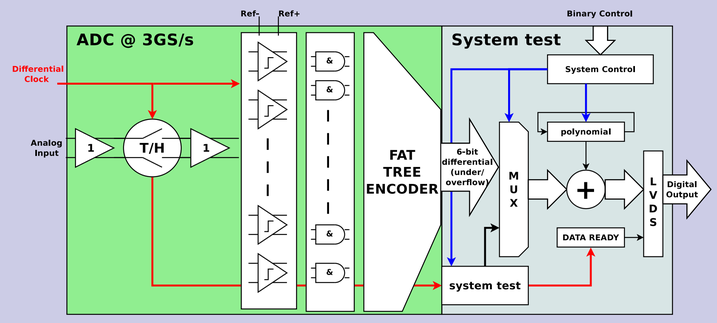

Figure 2: Block diagram of the ADC.

CIRCUIT IMPLEMENTATION

Track and Hold

The T/H study is based on [5, 6]. The goal is to reduce the feedthrough and the droop rate, to adapt the input and to have a low impedance on output. Three parts make up this T/H (Fig: 3): An input buffer, T/H (switch with a charge capacitance) and an output buffer.

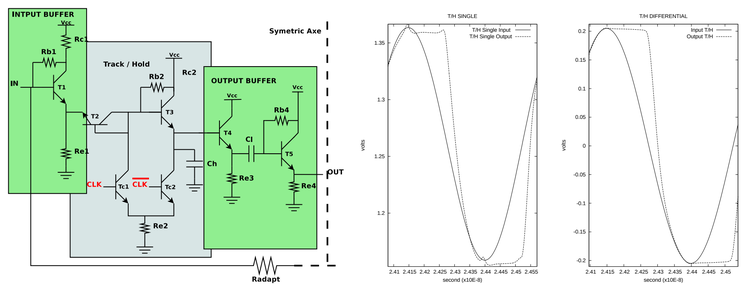

Figure 3: Track and Hold design and Transient simulations with input signal at 2 GHz and clock signal at 4 GHz single-ended and differential

Comparator

The pre-amplifier has a large bandwidth and provides sufficient gain to obtain a large voltage. Using a Monte Carlo statistical analysis, a yield higher than 90% is obtained at 3 GS/s for a quantum of 1 mV.

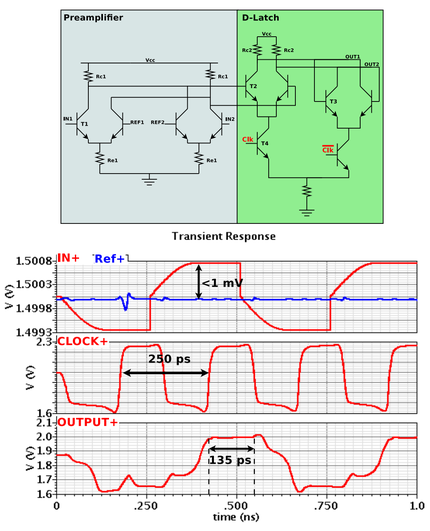

Figure 4: Comparator design: pre-amplifier and ECL D-latches

Digital

The digital part of the ADC is composed by a Bubble Correction (BC) and a Wallace Tree Encoder (WTE). Fig: 5 shows the gate architecture. Synchronization is improved by adding a D-Latch between the BC, the WTE, and the output digital part. This is similar to the method employed in the structure of the comparator.

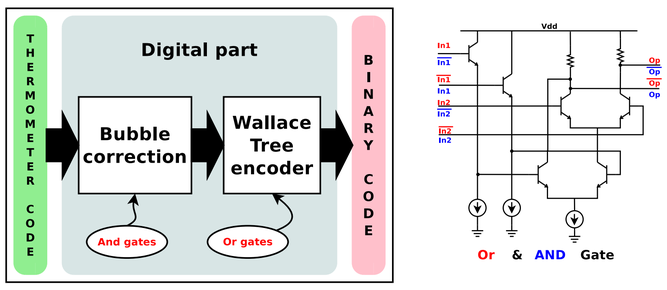

Figure 5: Digital part and digital gate

Integrated Test System

A test system is integrated on chip to evaluate the transmission to the data acquisition card (fig: 7). Random binary code is also integrated in the circuit for test purposes. The output data can be scrambled allowing the possibility to use Clock Data Recovery (CDR) at the output without sending the clock itself.

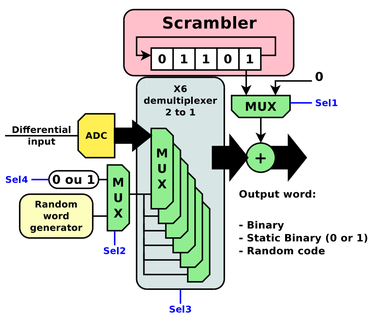

Figure 6: Output ADC design

ADC layout

The layout is designed with the overall goal of minimizing cost. The layout is divided into sectors that are isolated by a guard ring. Each ladder resistance is composed of ten resistances for improved matching. The comparator ladder is symmetrically divided in 2 blocks. The clock is distributed symmetrically with a clock regeneration for each 8 comparators. LVDS are integrated in Output Logical pads. The ADC layout with pads has a total area of 4.25mm^2 (fig: 7).

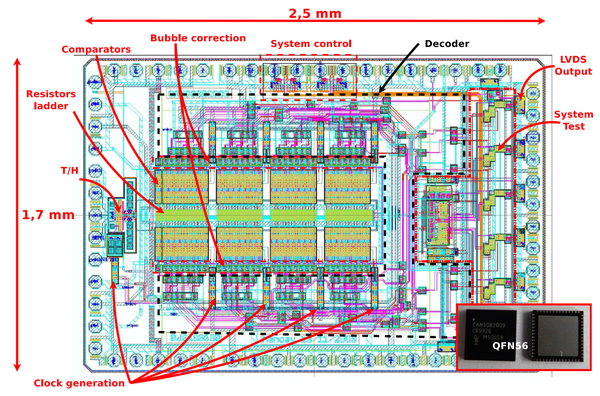

Figure 7: Layout

Simulation, Measurements and Results

Static and dynamic parameters have been characterized in simulation. Dynamic parameters were computed with a 700 points time resolution. The resistance and capacitance parasitic extraction simulation predicts an effective number of bits (ENOB) of 5.2 bits at 100 MHz to 5 bits at 1500 MHz (Fig: 9b). The static performance analysis of the flash ADC gives a DNL (Differential Non-Linearity) and INL (Integral Non-Linearity) smaller than 0.6 LSB.

Table 1: Specifications

Process	0.25 μm
Input range	0.5 V
Sampling rate	3 GS/s
Bandwidth	1500 MHz
Supply	2.5 & 2 V
Power diss.	2.6 W
Die area	4.25 mm^2

Table 2: Consumption Budget

Blocks	Supply	Current	Power
T/H	2.5 V	64 mA	160 mW
Comparators	2 V	468 mA	936 mW
Digital	2 V	470 mA	940 mW
System test	2 V	115 mA	230 mW
LVDS	2 V	189 mA	378 mW
Total	—	—	2644 mW

Table: 2 presents the power consumption budget for the ADC and Table: 1 presents specifications. Physical characterisation is in progress. Three test benches are being prepared for measurement. On the first test bench (Fig: 9a), the ADC outputs are acquired with a fast oscilloscope (see the eye diagram Fig: 8). For the second test bench, the data are sent via optical fibre directly to the data acquisition card (Vertex 6 FPGA board) using SFP+ connectors to evaluate static and dynamic parameters.

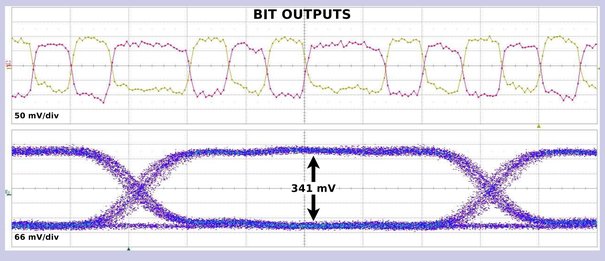

Figure 8: Digital results: 1-bit Eye diagram at 3 GS/s.

The third test bench uses external 1-to-8 demultiplexers designed at the Nançay Radio Astronomy Facility. The demultiplexer data rate is 375 MHz. Each ADC bit is connected to a demultiplexer to reduce speed data to easier acquisition. Matlab scripts are used for the ADC performance analysis.

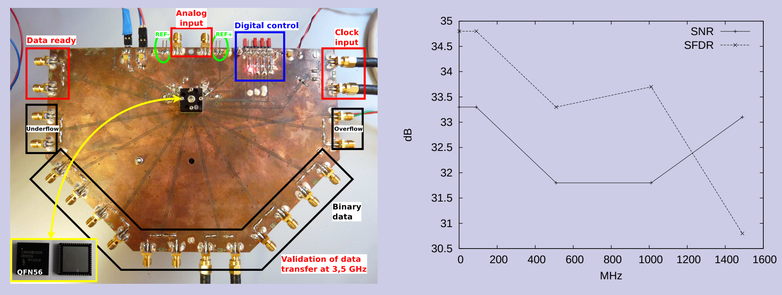

Figure 9: Test card and simulation results: a) Test card showing input and output ports. b) Dynamic simulation results.

Conclusions

The Flash ADC operates at 3 GS/s with an ENOB > 5 bits for input frequencies up to 1.5 GHz. The ADC was produced with the 0.25 μm QUBIC4X technology of NXP. It consumes 2.6 W. Efforts will be made to reduce the general power consumption in a next generation chip.

References

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