OUT CH	VSI1 GEO	VSI1 ASTRO	VSI1 ASTRO2	VSI1 WASTRO	VSI1 LBA	VSI1 TEST 0	VSI1 TEST 1	VSI1 TEST Bin	VSI1 TEST TVG
1	1US	1US	1US	1US	1US	0	1	BinC0	TVG0
2	1UM	1UM	1UM	1UM	1UM	0	1	BinC1	TVG1
3	2US	2US	2US	2US	2US	0	1	BinC2	TVG2
4	2UM	2UM	2UM	2UM	2UM	0	1	BinC3	TVG3
5	3US	3US	3US	3US	5US	0	1	BinC4	TVG4
6	3UM	3UM	3UM	3UM	5UM	0	1	BinC5	TVG5
7	4US	4US	4US	4US	6US	0	1	BinC6	TVG6
8	4UM	4UM	4UM	4UM	6UM	0	1	BinC7	TVG7
9	5US	5US	9US	5US	3US	0	1	BinC8	TVG8
10	5UM	5UM	9UM	5UM	3UM	0	1	BinC9	TVG9
11	6US	6US	10US	6US	4US	0	1	BinC10	TVG10
12	6UM	6UM	10UM	6UM	4UM	0	1	BinC11	TVG11
13	7US	7US	11US	7US	7US	0	1	BinC12	TVG12
14	7UM	7UM	11UM	7UM	7UM	0	1	BinC13	TVG13
15	8US	8US	12US	8US	8US	0	1	BinC14	TVG14
16	8UM	8UM	12UM	8UM	8UM	0	1	BinC15	TVG15
17	1LS	1LS	1LS	1LS	1LS	0	1	BinC16	TVG16
18	1LM	1LM	1LM	1LM	1LM	0	1	BinC17	TVG17
19	8LS	2LS	2LS	2LS	2LS	0	1	BinC18	TVG18
20	8LM	2LM	2LM	2LM	2LM	0	1	BinC19	TVG19
21	9US	3LS	3LS	3LS	5LS	0	1	BinC20	TVG20
22	9UM	3LM	3LM	3LM	5LM	0	1	BinC21	TVG21
23	10US	4LS	4LS	4LS	6LS	0	1	BinC22	TVG22
24	10UM	4LM	4LM	4LM	6LM	0	1	BinC23	TVG23
25	11US	5LS	9LS	5LS	3LS	0	1	BinC24	TVG24
26	11UM	5LM	9LM	5LM	3LM	0	1	BinC25	TVG25
27	12US	6LS	10LS	6LS	4LS	0	1	BinC26	TVG26
28	12UM	6LM	10LM	6LM	4LM	0	1	BinC27	TVG27
29	13US	7LS	11LS	7LS	7LS	0	1	BinC28	TVG28
30	13UM	7LM	11LM	7LM	7LM	0	1	BinC29	TVG29
31	14US	8LS	12LS	8LS	8LS	0	1	BinC30	TVG30
32	14UM	8LM	12LM	8LM	8LM	0	1	BinC31	TVG31

OUT CH	VSI1 8bit	VSI1 GEO2							
1	1|2|3|4, U|L, bit0	1US							
2	1|2|3|4, U|L, bit1	1UM							
3	1|2|3|4, U|L, bit2	2US							
4	1|2|3|4, U|L, bit3	2UM							
5	1|2|3|4, U|L, bit4	3US							
6	1|2|3|4, U|L, bit5	3UM							
7	1|2|3|4, U|L, bit6	4US							
8	1|2|3|4, U|L, bit7	4UM							
9	5|6|7|8, U|L, bit0	5US							
10	5|6|7|8, U|L, bit1	5UM							
11	5|6|7|8, U|L, bit2	6US							
12	5|6|7|8, U|L, bit3	6UM							
13	5|6|7|8, U|L, bit4	7US							
14	5|6|7|8, U|L, bit5	7UM							
15	5|6|7|8, U|L, bit6	8US							
16	5|6|7|8, U|L, bit7	8UM							
17	9|10|11|12, U|L, bit0	9US							
18	9|10|11|12, U|L, bit1	9UM							
19	9|10|11|12, U|L, bit2	10US							
20	9|10|11|12, U|L, bit3	10UM							
21	9|10|11|12, U|L, bit4	11US							
22	9|10|11|12, U|L, bit5	11UM							
23	9|10|11|12, U|L, bit6	12US							
24	9|10|11|12, U|L, bit7	12UM							
25	13|14|15|16, U|L, bit0	13US							
26	13|14|15|16, U|L, bit1	13UM							
27	13|14|15|16, U|L, bit2	14US							
28	13|14|15|16, U|L, bit3	14UM							
29	13|14|15|16, U|L, bit4	15US							
30	13|14|15|16, U|L, bit5	15UM							
31	13|14|15|16, U|L, bit6	16US							
32	13|14|15|16, U|L, bit7	16UM							

8bit mode is available. A preliminary selection of which USB or LSB of one of the four bbc available to send to the output is necessary. Only one bbc per group available in a Core2 can be selected. The section is done with

reg=bbc#,3,sideband

bbc#=>1|2|3|4 in Core2#1, 5|6|7|8 in Core2#2, 9|10|11|12 in Core2#3, 13|14|15|16 in Core2#4

sideband=>1 for USB, 2 for LSB

OUT CH	VSI2 GEO	VSI2 ASTRO	VSI1 ASTRO2	VSI2 WASTRO	VSI2 LBA	VSI2 TEST 0	VSI2 TEST 1	VSI2 TEST Bin	VSI2 TEST TVG
1	1US	1US	1US	9US	1US	0	1	BinC0	TVG0
2	1UM	1UM	1UM	9UM	1UM	0	1	BinC1	TVG1
3	2US	2US	2US	10US	2US	0	1	BinC2	TVG2
4	2UM	2UM	2UM	10UM	2UM	0	1	BinC3	TVG3
5	3US	3US	3US	11US	5US	0	1	BinC4	TVG4
6	3UM	3UM	3UM	11UM	5UM	0	1	BinC5	TVG5
7	4US	4US	4US	12US	6US	0	1	BinC6	TVG6
8	4UM	4UM	4UM	12UM	6UM	0	1	BinC7	TVG7
9	5US	5US	9US	13US	3US	0	1	BinC8	TVG8
10	5UM	5UM	9UM	13UM	3UM	0	1	BinC9	TVG9
11	6US	6US	10US	14US	4US	0	1	BinC10	TVG10
12	6UM	6UM	10UM	14UM	4UM	0	1	BinC11	TVG11
13	7US	7US	11US	15US	7US	0	1	BinC12	TVG12
14	7UM	7UM	11UM	15UM	7UM	0	1	BinC13	TVG13
15	8US	8US	12US	16US	8US	0	1	BinC14	TVG14
16	8UM	8UM	12UM	16UM	8UM	0	1	BinC15	TVG15
17	1LS	1LS	1LS	9LS	1LS	0	1	BinC16	TVG16
18	1LM	1LM	1LM	9LM	1LM	0	1	BinC17	TVG17
19	8LS	2LS	2LS	10LS	2LS	0	1	BinC18	TVG18
20	8LM	2LM	2LM	10LM	2LM	0	1	BinC19	TVG19
21	9US	3LS	3LS	11lS	5LS	0	1	BinC20	TVG20
22	9UM	3LM	3LM	11LM	5LM	0	1	BinC21	TVG21
23	10US	4LS	4LS	12LS	6LS	0	1	BinC22	TVG22
24	10UM	4LM	4LM	12LM	6LM	0	1	BinC23	TVG23
25	11US	5LS	9LS	13LS	3LS	0	1	BinC24	TVG24
26	11UM	5LM	9LM	13LM	3LM	0	1	BinC25	TVG25
27	12US	6LS	10LS	14LS	4LS	0	1	BinC26	TVG26
28	12UM	6LM	10LM	14LM	4LM	0	1	BinC27	TVG27
29	13US	7LS	11LS	15LS	7LS	0	1	BinC28	TVG28
30	13UM	7LM	11LM	15LM	7LM	0	1	BinC29	TVG29
31	14US	8LS	12LS	16LS	8LS	0	1	BinC30	TVG30
32	14UM	8LM	12LM	16LM	8LM	0	1	BinC31	TVG31

OUT CH	VSI2 8bit	VSI2 GEO2								
1	1|2|3|4, U|L, bit0	1LS								
2	1|2|3|4, U|L, bit1	1LM								
3	1|2|3|4, U|L, bit2	2LS								
4	1|2|3|4, U|L, bit3	2LM								
5	1|2|3|4, U|L, bit4	3LS								
6	1|2|3|4, U|L, bit5	3LM								
7	1|2|3|4, U|L, bit6	4LS								
8	1|2|3|4, U|L, bit7	4LM								
9	5|6|7|8, U|L, bit0	5LS								
10	5|6|7|8, U|L, bit1	5LM								
11	5|6|7|8, U|L, bit2	6LS								
12	5|6|7|8, U|L, bit3	6LM								
13	5|6|7|8, U|L, bit4	7LS								
14	5|6|7|8, U|L, bit5	7LM								
15	5|6|7|8, U|L, bit6	8LS								
16	5|6|7|8, U|L, bit7	8LM								
17	9|10|11|12, U|L, bit0	9LS								
18	9|10|11|12, U|L, bit1	9LM								
19	9|10|11|12, U|L, bit2	10LS								
20	9|10|11|12, U|L, bit3	10LM								
21	9|10|11|12, U|L, bit4	11LS								
22	9|10|11|12, U|L, bit5	11LM								
23	9|10|11|12, U|L, bit6	12LS								
24	9|10|11|12, U|L, bit7	12LM								
25	13|14|15|16, U|L, bit0	13LS								
26	13|14|15|16, U|L, bit1	13LM								
27	13|14|15|16, U|L, bit2	14LS								
28	13|14|15|16, U|L, bit3	14LM								
29	13|14|15|16, U|L, bit4	15LS								
30	13|14|15|16, U|L, bit5	15LM								
31	13|14|15|16, U|L, bit6	16LS								
32	13|14|15|16, U|L, bit7	16LM								

8bit mode is available in v105 only. A preliminary selection of which USB or LSB of one of the four bbc available to send to the output is necessary. Only one bbc per group available in a Core2 can be selected. The section is done with

reg=bbc#,3,sideband

bbc#=>1|2|3|4 in Core2#1, 5|6|7|8 in Core2#2, 9|10|11|12 in Core2#3, 13|14|15|16 in Core2#4

sideband=>2 for USB, 3 for LSB