

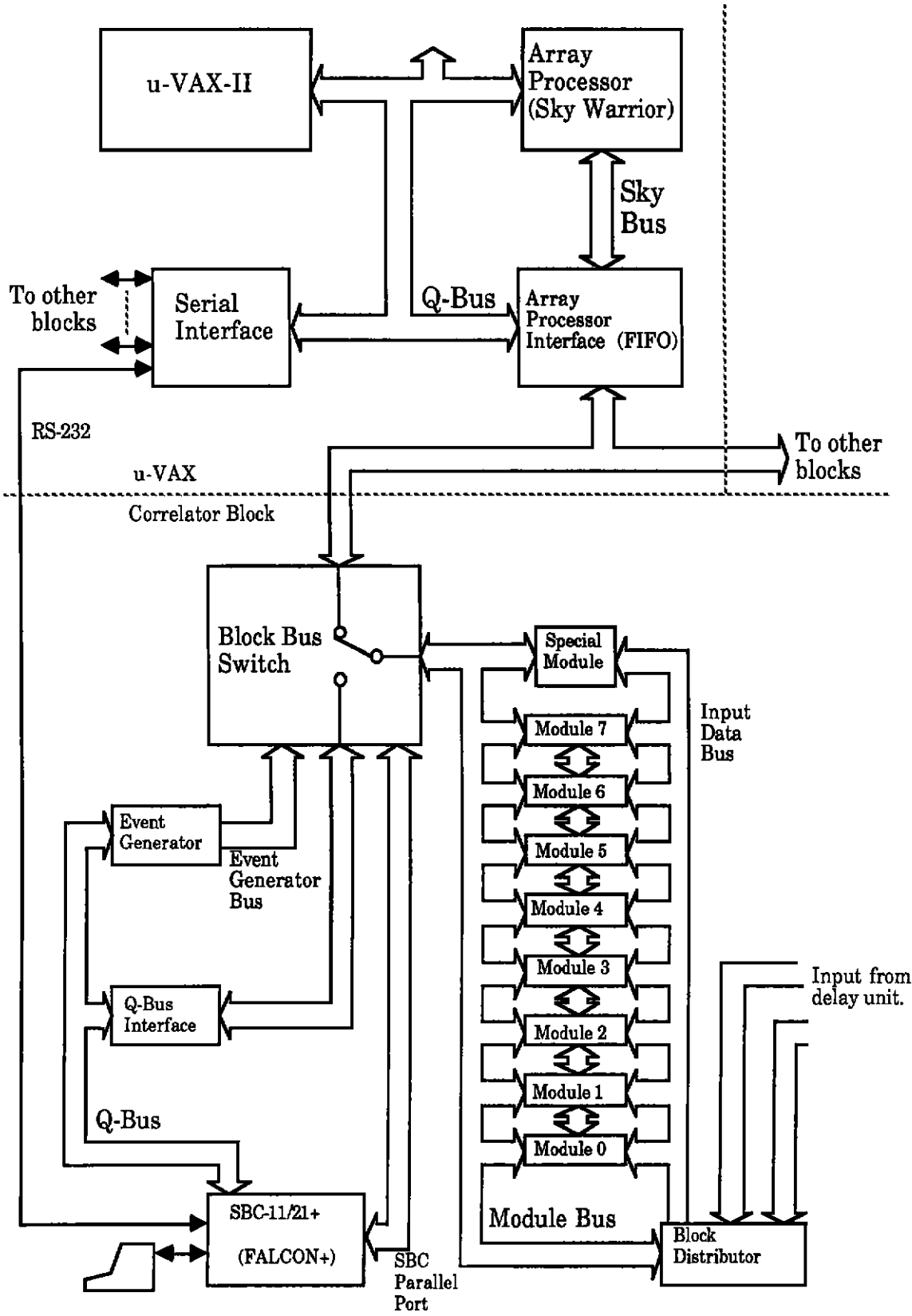
# AT Correlator Block Technical Information

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This document gives a technical description of parts of the Australia Telescope Correlator Block. The objective is to give a description of the capabilities and limitations of the correlator by showing the ways in which data and control information flow through the machine. Parts of the correlator for which the design has been completed are described in full, but parts which are still in preliminary stages are only described briefly.

## 1. The Correlator Block.

Each baseline of the telescope is handled by a correlator **Block** which is shown in Fig(1). The block contains eight correlating elements, known as the correlator **Modules**, numbered 0 through 7, and a special module attached at the end. Each of the 8 input buses (four from each antenna) going into the block are distributed to each module by the block distributor. The modules then individually select a pair of input buses for correlation. In addition to this, adjacent modules may be connected together (known as module **concatenation**) to increase the number of lags measured at a given input bandwidth. The modules are linked via the **Module Bus** which is used for control of the modules and for access to the correlated data. Each module can be programmed to function in one or two bit mode and in one of six reconfigurations giving input data rates between 512 Msamples/sec and 16 Msamples/sec in one bit mode or 256Msamples/sec and 8 Msamples/sec in 2 bit mode. The special module is used for collecting polarization calibration data.



Fig(1): Correlator block functional layout.

Programming and configuring of the correlator modules is the task of a FALCON+ computer (LSI-11/21) which resides on its own Q-Bus in the block cabinet. The Q-Bus also contains an **Event Generator** and an interface to the Module Bus. The Event Generator is a device capable of producing 15 timing lines (events) to an accuracy of  $1\mu\text{S}$ . The timing information required to produce these events is distributed to all the event generators on a high speed serial bus. The event lines are used to control all aspects of the correlator which are time critical, *ie* those which occur during the actual observing. The FALCON+ computer is used for configuring and programming the modules and for performing tests of the hardware.

The correlator block receives its control information from a host computer through an RS-232 line. The computer at the other end of this line performs all the high level control functions and processing of the data. Details of the observing sequence (the information required to generate the appropriate events on the event generator) will be transmitted to each block via the RS-232 link and the block control computer (the FALCON+) will perform all the processing required during the actual observing session. The block communication lines will not carry any real-time data apart from error and informational messages.

The host computer has access to the correlated data through a bus connected to all blocks. This is connected to the module bus by a switch which is controlled by the block control computer. The external bus only has access to the memory in the modules containing the correlated data, not to the configuration registers in the modules. When the switch is set so that the block control computer has access to the modules, it can access the correlator data area (the accumulator memory) as well as the control registers and tables. Thus, the block control computer will be able to perform testing functions on the block components.

## 1.1 The Correlator Module.

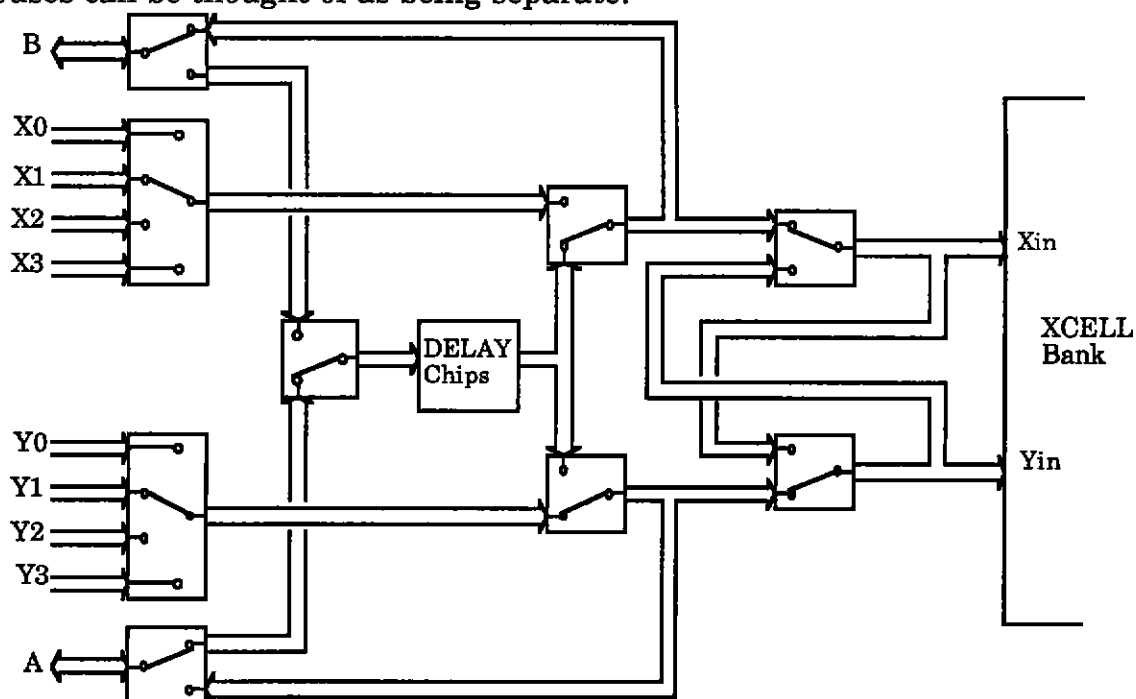
The correlator module itself is centered around a bank of 16 XCELL chips arranged into a 4x4 array providing the 1024 correlating elements. The module board also contains 2 DELAY chips which can be switched in to the data path when modules are being concatenated. The circuitry on the module falls into two functional sections, the **input switching** and the **accumulator memory** sections. These correspond to the circuitry at the input and output of the XCELL chips respectively.

### 1.1.1 Input Switching.

Each module is supplied with four input channels per antenna. The modules are also connected together in series by the A/B bus which is used for module concatenation. The input switching circuitry of the module

selects the required pair of inputs and directs this data to the inputs of the XCELL bank.

The data paths available in the module input switching section are shown in Fig(2). The eight input buses (each carrying 32 bits of information, some of which are unused depending upon the reconfiguration factor of the module) are labeled X0..X3 corresponding to one antenna and Y0..Y3 corresponding to the other antenna. Physically, these eight buses are paired and multiplexed onto two buses to travel along the block backplane. This is transparent to the user however, and the four buses can be thought of as being separate.



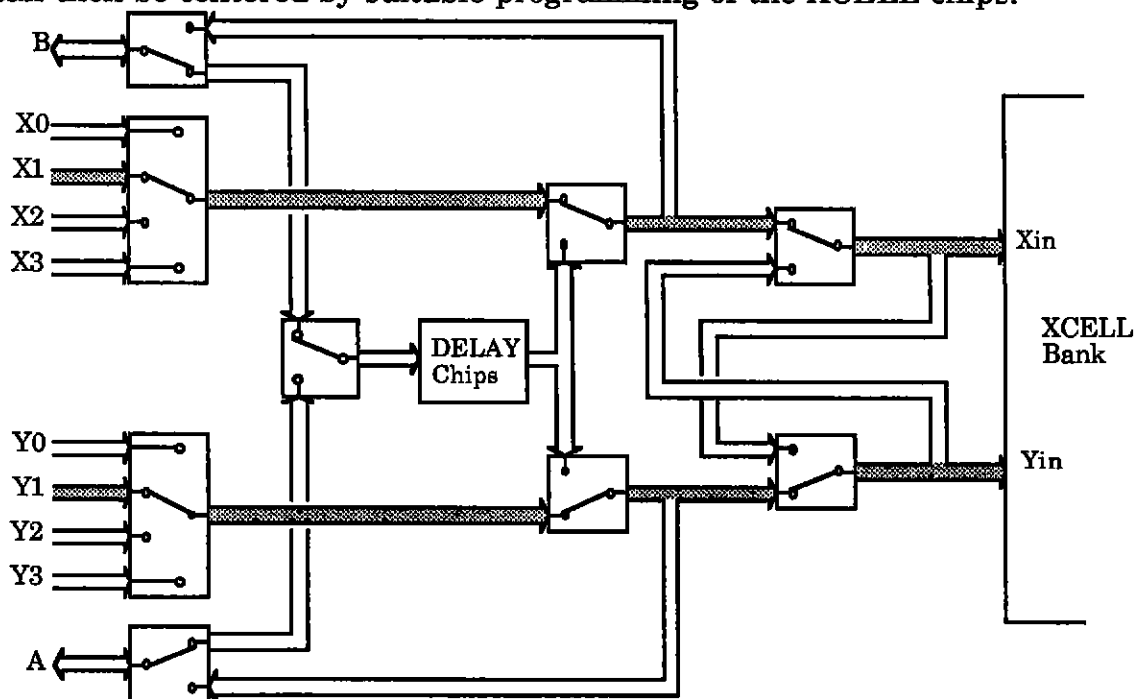
**Fig(2):** Correlator module input section.

The A/B bus is bidirectional and its direction depends upon whether the signal being delayed originated at an X or Y input. The block backplane is wired such that the B bus of module n is connected to the A bus of module n-1. This provides the mechanism for propagating data between adjacent modules. The A/B bus carries only 16 data lines and modules cannot be concatenated at reconfiguration zero.

Data can be switched along the data paths within the module in several useful ways. The following is a description of the most common configurations.

### 1.1.1.1 Single Module per Product.

The module input switching scheme used when a single module is to be used to correlate an X and a Y channel is shown in Fig(3). In this case the data is simply switched from the input buses to the input of the XCELL bank. Eight products per baseline can be formed when all modules in the block are set up in this way. The lag function produced by the XCELL bank can then be centered by suitable programming of the XCELL chips.



Fig(3): Single module configuration.

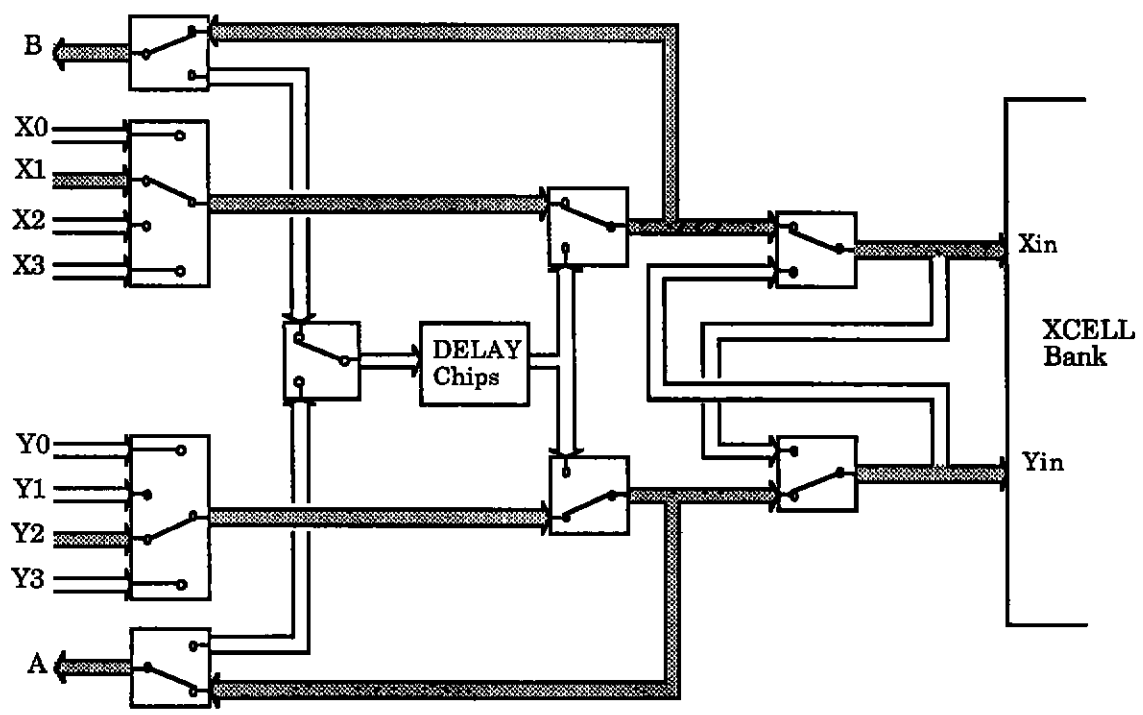
### 1.1.1.2 Multiple Modules per Product.

Each module in the block can be configured to measure the correlation function for a certain range in the lag domain. Modules in the block may also be concatenated so that adjacent modules measure the correlation function for adjacent lag ranges on the same product. This gives a greater number of lag channels and hence a greater number of frequency points for this product.

The amount of module concatenation which takes place is fully programmable, the only restriction being that only adjacent modules may be concatenated. For example, three modules at one end could be concatenated to measure the lag function from one pair of input channels and the remainder of the modules may be used individually. Alternatively, a second three may be chosen to measure the same lag channels on a

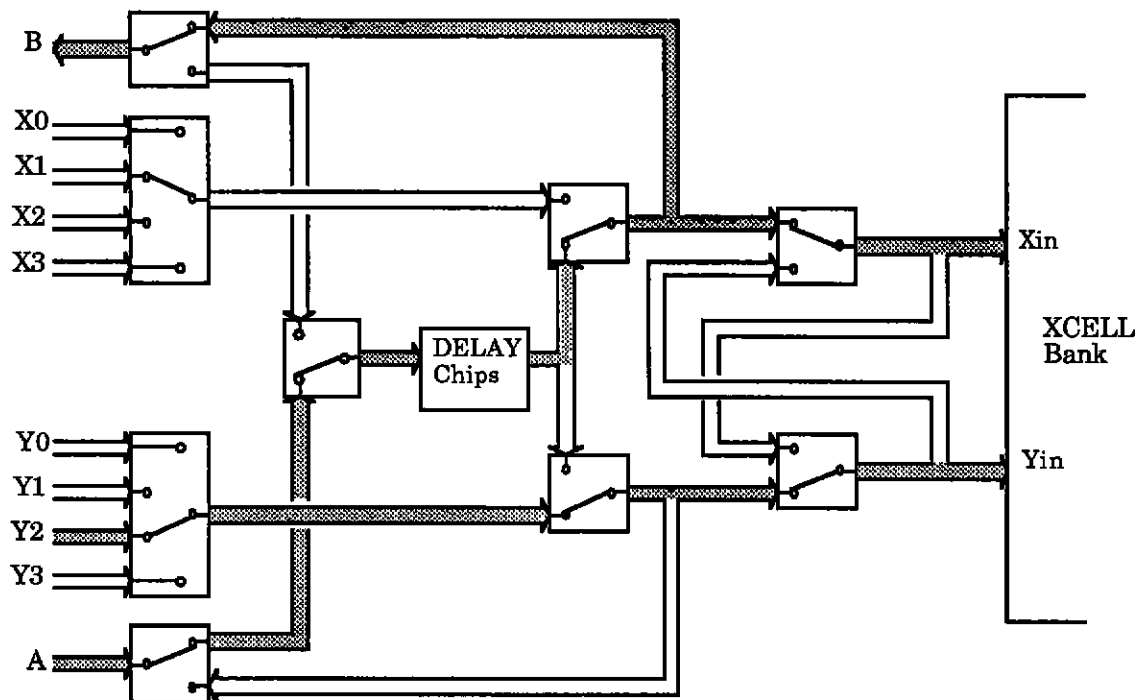
different product, leaving two which may be used individually or as another concatenated pair.

Module concatenation is made possible by the DELAY chips and the associated input switching on each module which is used to propagate data along the A/B bus. The useful configurations of the input switching circuitry are shown in Fig(4) through Fig(8). The data enters the concatenated module set at the centre module, as shown in Fig(4). On this module, both the A and B ports are configured as outputs and the data from the selected X and Y channels is made available on the B and A ports respectively, to appear at the A port of the next lowest numbered module and at the B port of the next highest numbered module.

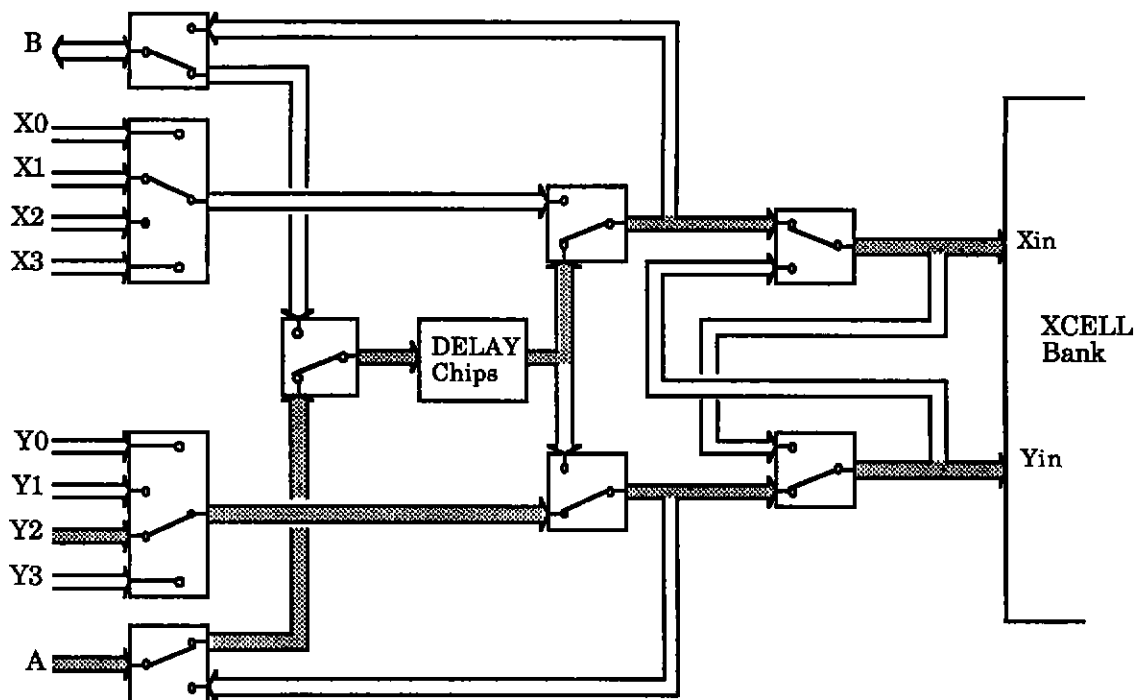


Fig(4): Central (first) module of concatenation.

The next lowest module is shown in Fig(5). In this case, the X input to the XCELL bank is not switched from the X input, but from the A port through the DELAY chips. The DELAY chips impose a delay equal to the width of the lag function measured by the XCELL bank on this input (first) module. Thus, the lag range measured by this module will be exactly adjacent to the lag range measured by the first module in the concatenated set.



**Fig(5):** Concatenated module in X lag direction.



**Fig(6):** Last module of concatenation in X lag direction.

Once the data has been delayed by the width of the correlation function, it is again passed out through the B port and is available to the next lowest module. This may be another module set up as shown in Fig(5) or it may be an X termination module, which is shown in Fig(6). The only difference between this and the previous is that the B port is not configured as an output and hence no data is passed out through it.

Delaying the data in the X direction generates lag values which are on one side of the lag range produced by the first module. The data can also be delayed in the Y direction to produce lag values on the other side. The Y input data on the first module appears on the A port of this module, which is connected to the B port of the next highest module. This module receives the data, puts it through the DELAY chips and presents it to the Y input to the XCELL bank as shown in Fig(7). In a similar manner to the X side of the concatenation, the delayed data is then output on the A port of this module. The last module in the Y concatenation is shown in Fig(8). This is the same as Fig(7) except that the A port is no longer configured as an output.

### 1.1.1.3 Autocorrelation.

A facility is provided which enables the correlator to be used in autocorrelation mode without having to physically supply the same data to both channels. This is shown in Fig(9) and Fig(10) for autocorrelation of the X and Y channels respectively. Note that this method of autocorrelation cannot be used in conjunction with module concatenation.

### 1.1.2 The XCELL Bank.

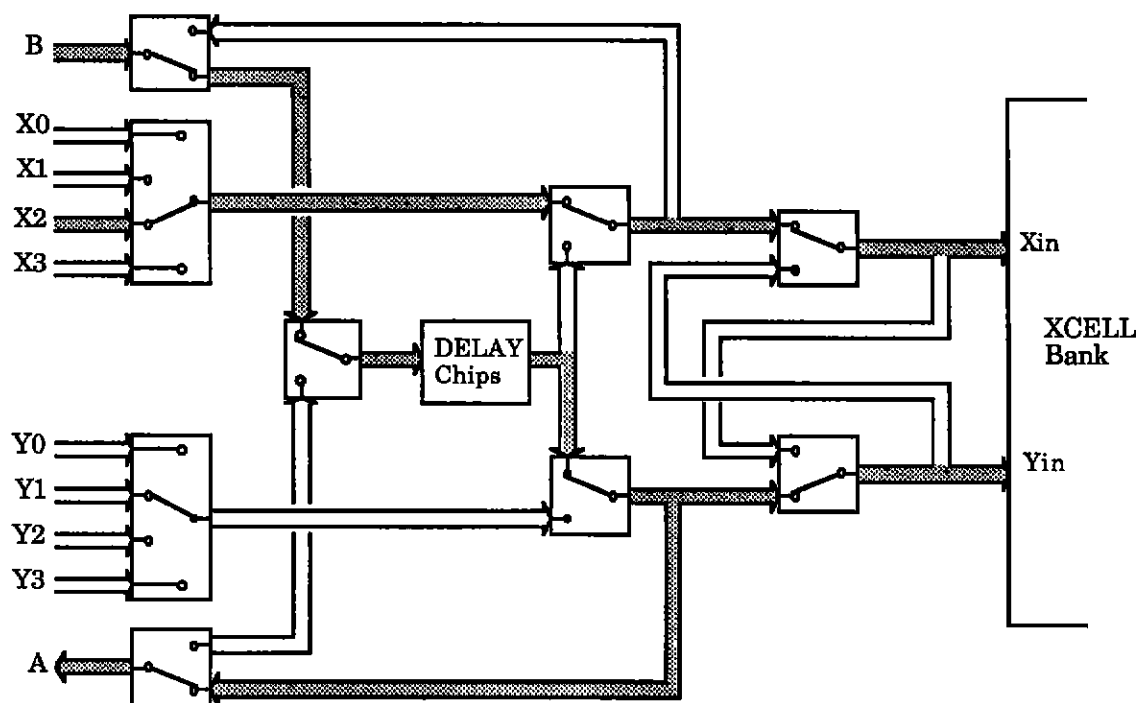
The XCELL bank is a 4x4 array of XCELL chips. Each XCELL chip is itself an 8x8 grid of accumulating elements. Thus, the entire XCELL bank looks like a 32x32 grid of correlating elements. It may be configured to correlate in either one or two bit mode. The 32-bit words are clocked in to the XCELL bank at a data rate of 16MHz. Not all of the 32-bits of the data word are used however, depending upon the **reconfiguration factor**. The reconfiguration factor is a number ranging from 0 to 5 and determines the number of lag channels measured by the correlator. The data rates and correlation channels for a single module at each reconfiguration factor are shown in Table(1). The lag weighting function for each reconfiguration is shown diagrammatically in Fig(11). Each diagram shows the lag channels on the horizontal axis and the number of correlating elements measuring that lag channel on the vertical axis. The value K is the reconfiguration factor. The value  $I_c$  is the number of input lines (of the possible 32) actually used by the XCELL bank. For example, at reconfiguration 2, only every fourth input line is used, because of the lower bandwidth. Fig(11) shows the centered lag spectrum. The XCELLs may also be programmed so that the



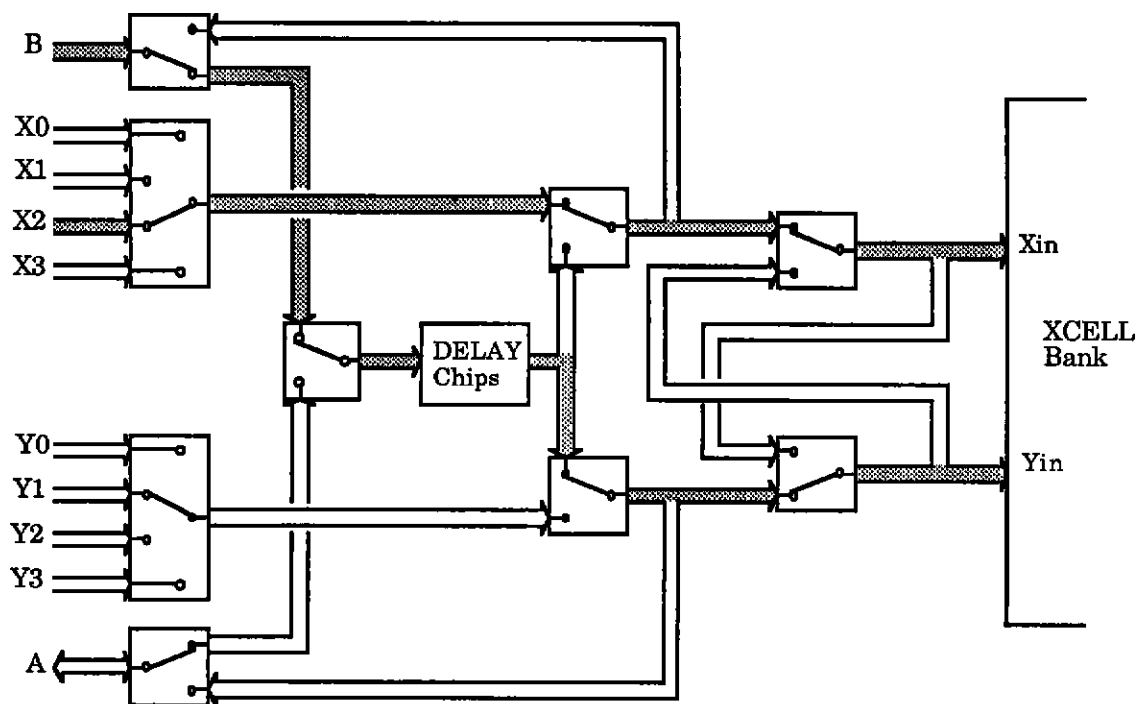
lag spectrum is one sided (*ie* occupies mainly positive lag channels) for module concatenation.

Reconfig. factor	# valid bits on input	Bandwidth		Lag Function Width	
		1-bit	2-bit	total	nominal
0	32	256MHz	128MHz	64	32
1	16	128MHz	64MHz	80	64
2	8	64MHz	32MHz	136	128
3	4	32MHz	16MHz	260	256
4	2	16MHz	8MHz	514	512
5	1	8MHz	4MHz	1024	1024

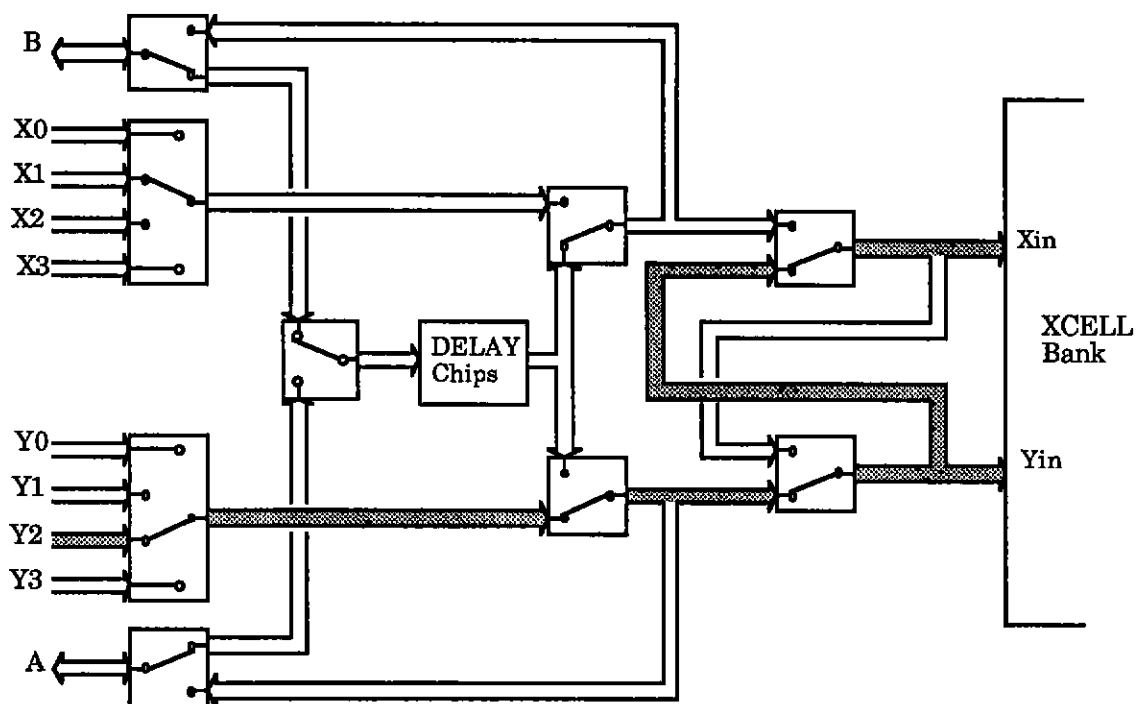
**Table(1):** Lag weighting function widths.



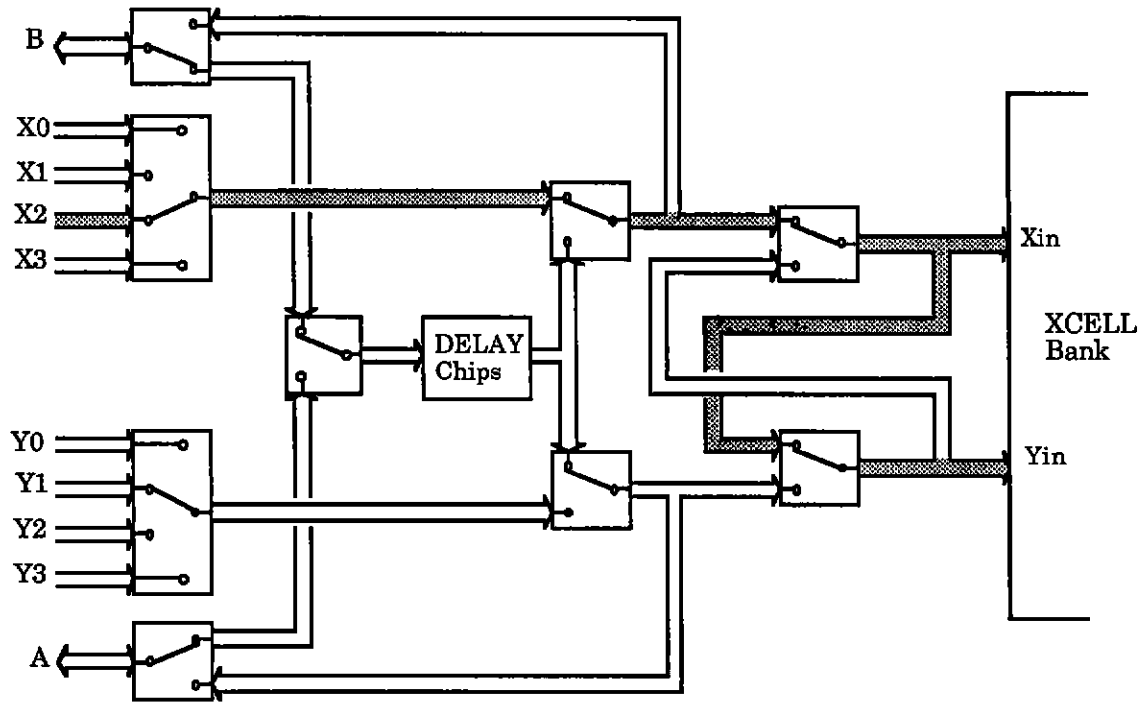
**Fig(7):** Concatenated module in Y lag direction.



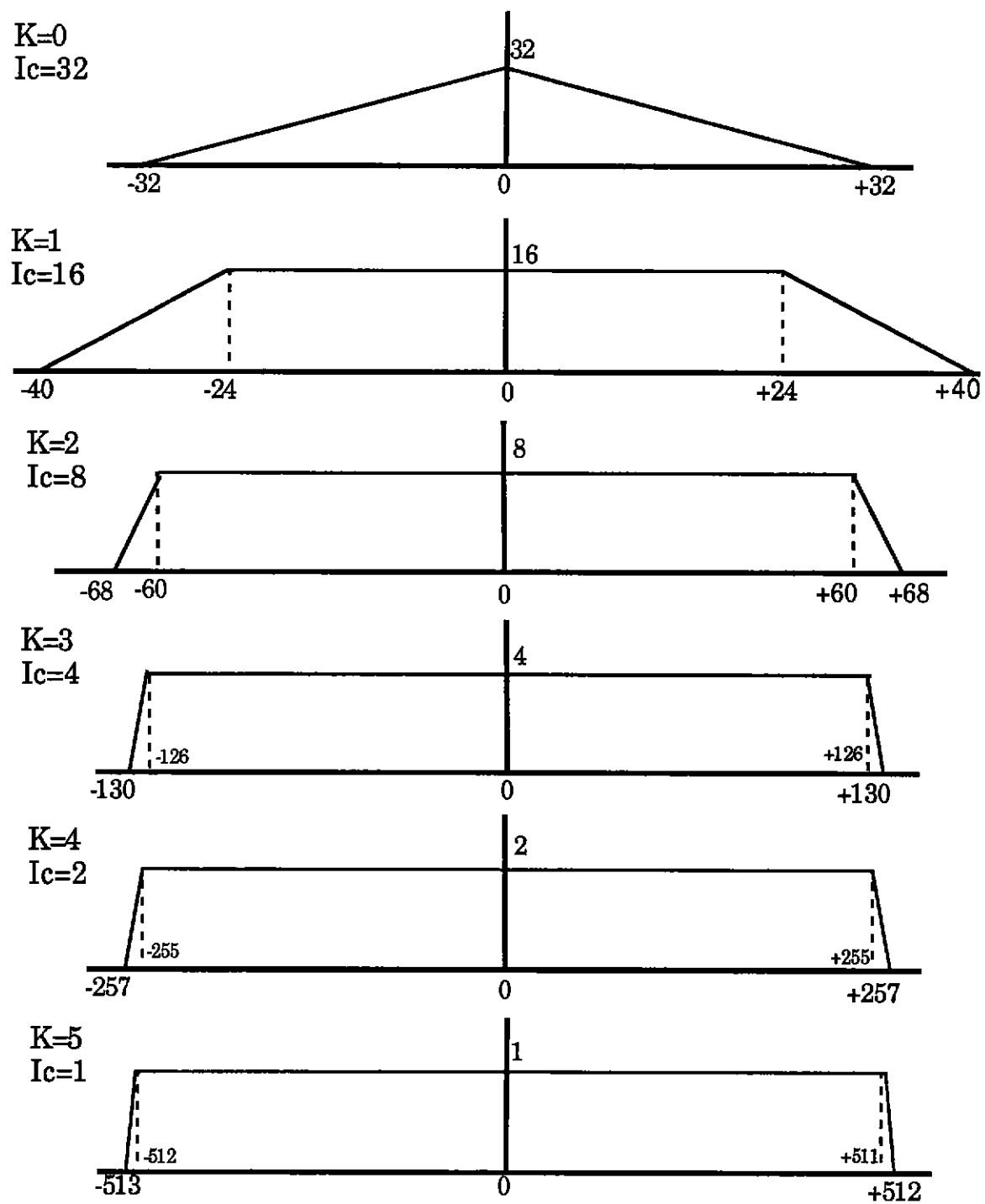
Fig(8): Last concatenated module in Y lag direction.



Fig(9): Autocorrelation of the Y input channel.



Fig(10): Autocorrelation of the X input channel.



Fig(11): Lag weighting functions.

For example, at reconfiguration factor 4, and 1-bit mode, bits 0 and 16 of the 32-bit data word carry valid data at a sample rate of 32Msamples/sec (2 lines clocked @16MHz). This is correlated by the XCELL bank to produce approximately 512 correlation channels. The "nominal" lag function width above differs from the "total" lag function width because the lag function weighting does not have vertical sides. The nominal lag function width quoted above is the number of lag channels between the half height points of the weighting function. The total width is the number of lag channels between the extreme ends of the weighting function.

### 1.1.3 Accumulator Memory and Module Control:

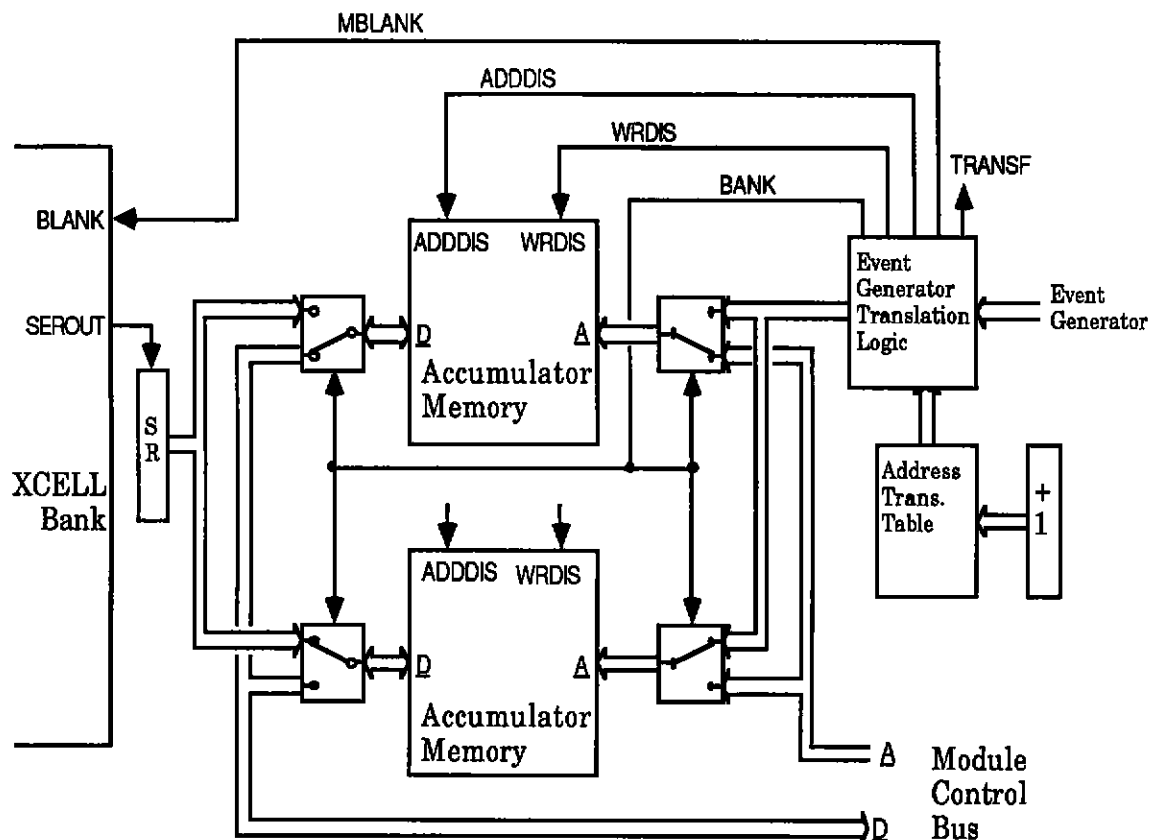
The raw correlated data emerges from the XCELL bank as a (one bit) serial data stream. The actual format of this is 1024 numbers, each 16 bits long. Since the accumulators in the XCELL chips do not provide enough dynamic range for the required integration time for the AT, external accumulator memory is provided. Thus, the **XCELL dump time** is defined as the time during which the XCELL chips accumulate the data and the **correlator integration time** is the time during which the accumulator memory accumulates the output from successive XCELL dumps.

The functional sections of the output and control section of the correlator module is shown in Fig(12). Two banks of **accumulator memory** are provided (8kx24-bit). These are provided so that while the XCELL data is being accumulated into one bank, the array processor interface can be reading the previously accumulated data from the other. Thus, the correlator integration time periods alternate between the two accumulator memory banks. The switching of these banks is essentially controlled by the event generator through the **Event Generator Translation Logic (EGTL)** via the **BANK** control line.

When writing to the accumulator, data that is presented to the memory for storage at an address will be combined with the data presently at that address according to the **ADDIS** and **WRDIS** inputs to the memory. When neither of these lines is active, the input is added to the contents of the memory location and the result written back to that location. When **ADDIS** is active, the addition does not take place, and the data presented at the input is written to the memory location. When **WRDIS** is active, the write does not take place and the current contents of that location are left undisturbed.

It would be undesirable to write the data from the XCELL bank directly into the accumulation memory because it emerges from the XCELL bank in an unnatural ordering (determined by the reconfiguration factor) and there are always 1024 numbers, some of these belonging to the same lag positions. In order that the data is written to the accumulator in the correct order, the **Address Translation Table (ATT)** provides the appropriate addresses. This is a memory (RAM) containing 8 banks of 1024

locations each and is loaded from the block control computer. It must contain the correct addresses to place the XCELL output data and the information required to generate the ADDDIS and WRDIS control lines.



Fig(12): Module accumulator memory and control section.

There are two other control lines for the block. The **MBLANK** line is an input to the XCELL bank which simply disables the accumulators in each XCELL chip. The **TRANSF** line when pulsed initiates the automatic transfer of data from the XCELL bank to the accumulator memory (an XCELL dump). It also effectively clears out the workspace of the XCELL accumulators so that they start accumulating fresh data. The XCELL dump takes 1024 $\mu$ S in one bit mode (2048 $\mu$ S in two bit mode) but does not interrupt the operation of the correlating elements of the XCELLs.

### 1.1.3.1 Event Generator Translation Logic:

The EGTL is shown in Fig(13) and serves several functions. Its inputs are the 15 event lines produced by the event generator (EGIN0..EGIN14) and the ATT data lines (ATTD0..ATTD11). It produces

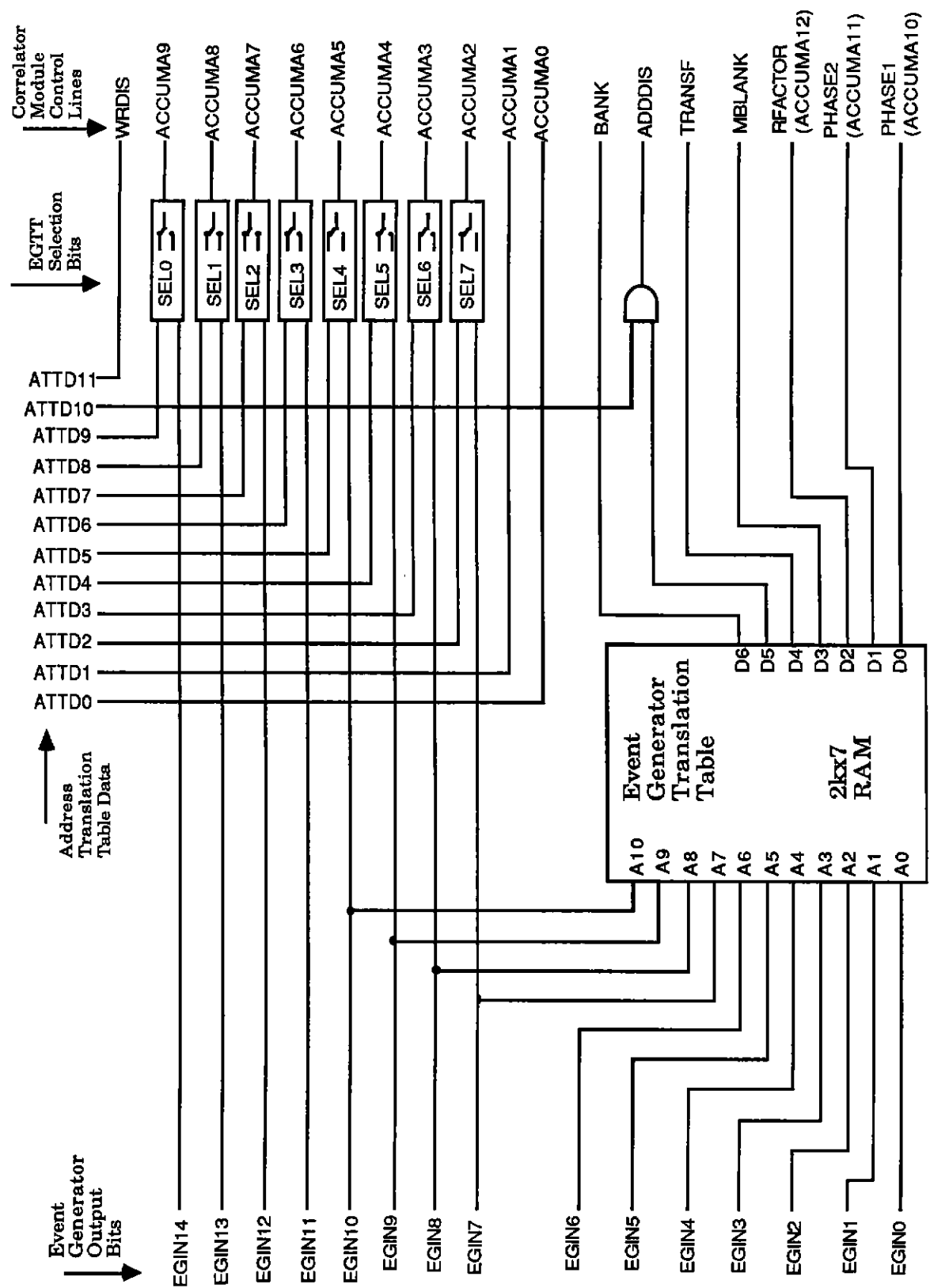
as its output the 13 accumulator memory address lines (ACCUMA0..ACCUMA12) and the five timing control lines (WRDIS, BANK, ADDDIS, TRANSF and MBLANK). Its provides a high degree of flexibility in controlling the modules during observing.

The function of the EGTL falls into two parts, providing the accumulator memory address lines and providing the high speed control lines. In the simplest mode of operation, the accumulator memory address is provided directly from the ATT and the high speed control lines come directly from the event generator. To configure the EGTL for this functionality, the **Event Generator Translation Table** (EGTT) is loaded such that it provides a one to one correspondence between lines A0..A6 and D0..D6, *i.e.* it behaves as if it were not present at all. The rest of the event generator lines then are not used and the 8 EGTL selection switches are set so that the accumulator memory address comes from the ATT data lines. These switches are controlled by data latched out of the FALCON+.

The write disable line, WRDIS, to the accumulator memory is also supplied from the ATT in this configuration. Normally, this will be inactive but can be set up for special purposes when only part of the lag function is required to be kept. The adder disable, ADDDIS, output is a combination of event generator and the ATT output. The accumulator memory adder needs to be disabled when writing the first data to the accumulator memory for each lag position in an integration cycle. Thus, D5 of the EGTT will need to be set during the first XCELL dump of an integration cycle and ATTD10 will be loaded with an active level corresponding to the first occurrence of each lag position.

The most significant three bits of the accumulator memory address are provided by the event generator. This allows for the data from sequential XCELL dump cycles to be accumulated into different pages of the accumulator memory. This may be useful if recirculation is employed or if phase switching is being implemented further upstream requiring the data from the different phases to be accumulated separately.

Considerable flexibility is built into the system by allowing the event generator outputs to be used in different ways through the EGTL. Some of the accumulator address lines can be put under control of the event generator by setting up the EGT selection switches differently before starting the observing session. If we change the switch associated with ACCUMA9 then we effectively have twice as many pages of accumulator memory (each half as large as before) in which to accumulate the XCELL data. More accumulator address lines can be placed under control of the event generator to enhance this effect. One use of this is in the case of pulsar observations where the accumulator memory can be better utilized in providing more bins per pulsar period at the expense of spectral data channels.



Fig(13): Event Generator Translation Logic.



The EGTL can also be used to provide modules with differing control timing by loading the appropriate data into the **Event Generator Translation Table (EGTT)**. For example, if the EGTT of one module is loaded such that D6 corresponds to A6 and another module is loaded so that D6 corresponds to A7 then the event generator can cause different timing to occur at the modules. This can also provide a timing control line depending upon a decoding of a subset of the event generator lines. For example, the MBLANK lines of all 8 modules could be controlled by three of the event generator lines if the observing task required that only one of the modules be accumulating data at any given time (*eg* for very fast pulsar observing).

## 2. The Correlator Control Computer.

Processing of the correlated data is performed by a uVAX-II running the MicroVMS operating system with a Sky Warrior array processor. This array processor uses the Q-Bus of its host computer to obtain its control information and a special high speed bus (the **Sky Bus**) to obtain the processed data from the correlator blocks, and for its own data storage. The correlated data is physically fetched from the correlator accumulator memories through a high speed long distance bus to a FIFO unit, and is then made available to the array processor.