

COMPACT ARRAY COMPUTERS AND SOFTWARE

The Compact Array of the AT consists of six 22-metre antennas arranged in a linear array of length 6 km. Each antenna contains two computers: the Antenna Control Computer (ACC) and the Position Control Computer (PCC). In the central control building is the correlator and the computers which control the array and the data processing and recording. The Correlator Control Computer (CCC) is a DEC μ VAX II (node name *SANCHO*). The CCC and ACCs are commanded by the synchronous computer (SYNCH) which is a DEC VAX 8250 (node name *NOEL*) and is in a VAXcluster with a second VAX 8250 (node name *LEON*) and a Hierarchical Storage Controller (HSC). Communication between the ACCs and *NOEL* is on a 38.4 kbaud serial line. Communication between the CCC and *NOEL* is on a 16-line parallel link with direct memory access (DMA) at each end of the link. Figure 1 is a diagram of the computers and their connections.

The Position Control Computer

The antennas have azimuth/elevation mounts, each axis being driven by a pair of DC motors. The function of the PCC is control the antenna position by commanding the motors through the Sweo motor controller. Each rate command is determined from the requested antenna position and position readings from the antenna's NPL encoders. Motor rate commands are issued at a rate of 15 Hz.

The main processor in the PCC is a National Semiconductor NS32016 unit. Rate commands are sent to the Sweo drive through a pair of serial lines (RS232) and AT datasets. Position requests are accepted from the ACC or the local control panel. The display/control panel contains two processors: an 80186 and an 8031, both by Intel. The NS32016 communicates with both the ACC and the control panel along an RS232 serial line at 4800 baud. Figure 2 shows the organization of the PCC.

Most of the NS32016 software is written in PASCAL. Assembly language is used for some interrupt handlers, device initialization and I/O routines.

The Antenna Control Computer

The function of the ACC is to provide demanded antenna positions for the PCC, configure receiver, local oscillators and samplers and to send status information to the control building.

The ACC is a DEC PDP 11/73 with 512 kbytes of memory, a NEC 360 kbyte floppy disk drive and controller, and two CAMINTON serial communications cards. One serial card has four RS232/RS422 channels used for communications with the control building and the antenna's datasets. The second has eight channels which can be configured for direct memory access (DMA). One of these channels is used for communication with the PCC. The ACC also has a frame grabber and an event generator which interface to the clock time signal and were designed and built within RP/ATNF.

The datasets provide all the interfaces with the antenna hardware and are used for controlling devices and for reading status values from a number of monitor points in those devices. Each antenna has about 400 monitor points which return information on the cryogenics, receiver frontends, LO settings and levels, power supply voltages and currents, etc.

The ACC software runs under the Micropower PASCAL operating system and is written in PASCAL. The ACC software has two high priority loops driven by external events:

Servo loop Initiated by receipt of data from the PCC. ACC responds by sending the next antenna position (Az,El) to the PCC. The servo loop operates at 15 Hz.

Integration cycle Stopped and restarted by the event generator. At present the cycle time is 10 seconds. During each cycle the LO and sampler phase rotation parameters for the next cycle are read from the DECNET line to NOEL and the event generator is configured for the next cycle.

The lower priority tasks interrogate datasets for monitor point values and return them to NOEL and maintain a status display. Figure 3 summarises the ACC tasks.

The Correlator Control Computer

The function of the CCC is to control all processing of IF signals from the antennas. This processing includes delay, correlation, transformation and formatting.

The CCC is a μ VAX II running VMS. It has 9 Mbytes of memory and two disks of 70 and 150 Mbyte capacity. It commands the LSI 11/21 computers controlling the delay unit and correlator modules through RS232 serial lines. The CCC contains a Sky Warrior array processor which is used to process the correlated data. Formatted data is sent to NOEL on the parallel link where it is recorded on disk.

The Synchronous Computer

The function of the synchronous computer is to provide the CCC and the ACCs with the data needed to make an observation. It also receives formatted visibility data from the CCC and records it on disk.

The synchronous computer, NOEL, is a VAX 8250 with 8 Mbytes of memory and is clustered to an HSC giving it access to two TU78 magnetic tape drives, three RA81 disks (400 Mbytes) and an 800 Mbyte MRA800 disk. The main observing programs run on NOEL and are written in FORTRAN with some VAX MACRO subroutines. A number of tasks run during observations. Inter-task communication is through areas of memory configured as shared FORTRAN common blocks and through VMS mailboxes. Figure 4 shows the organization of the observing tasks and areas of shared memory. Commands are sent to the ACCs and antenna monitor point information is returned to NOEL on a serial line using DECNET. Communication with the CCC (commands for the correlator and visibility data from the correlator) is on a parallel link using the VMS DMA device driver and software-written on site.

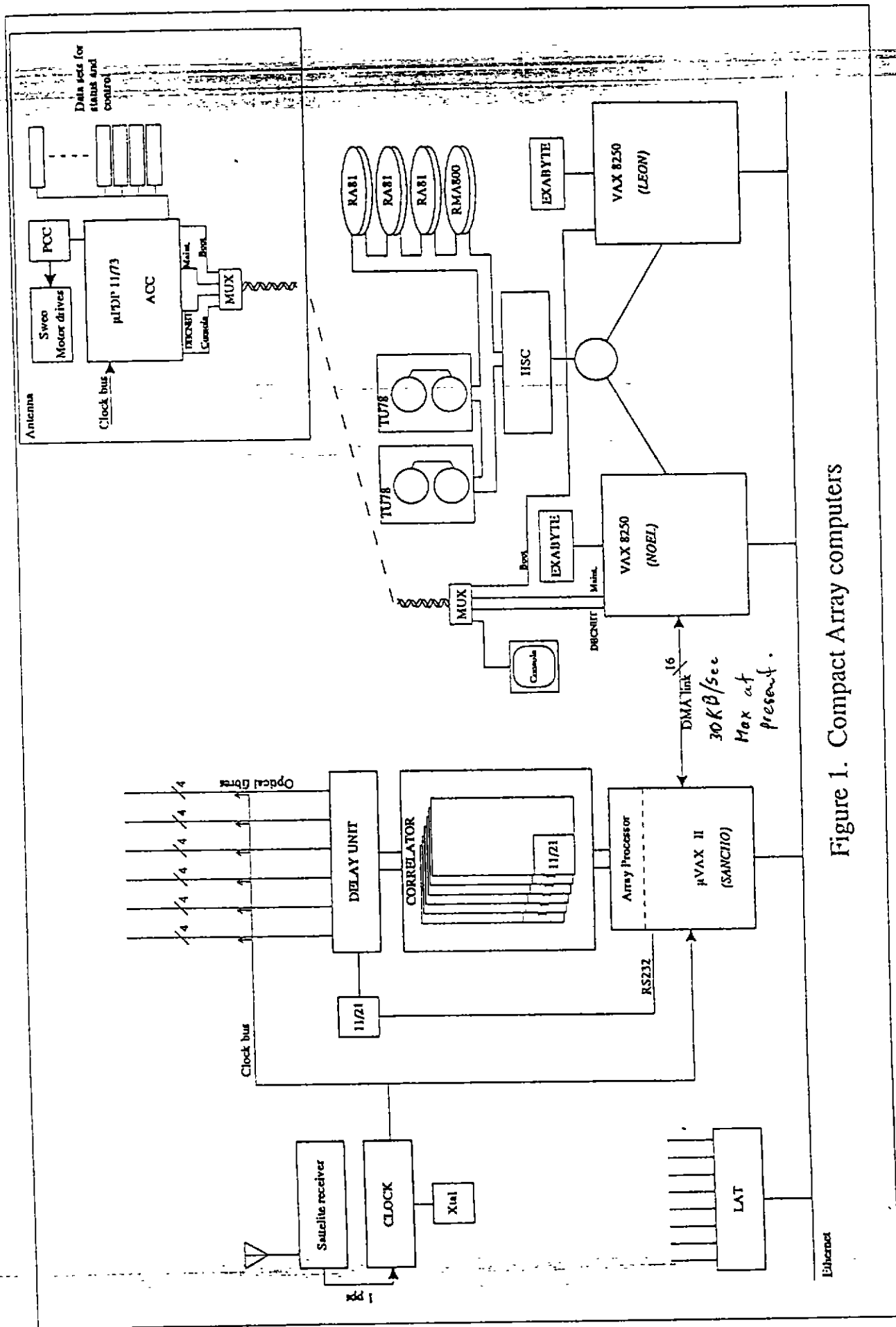
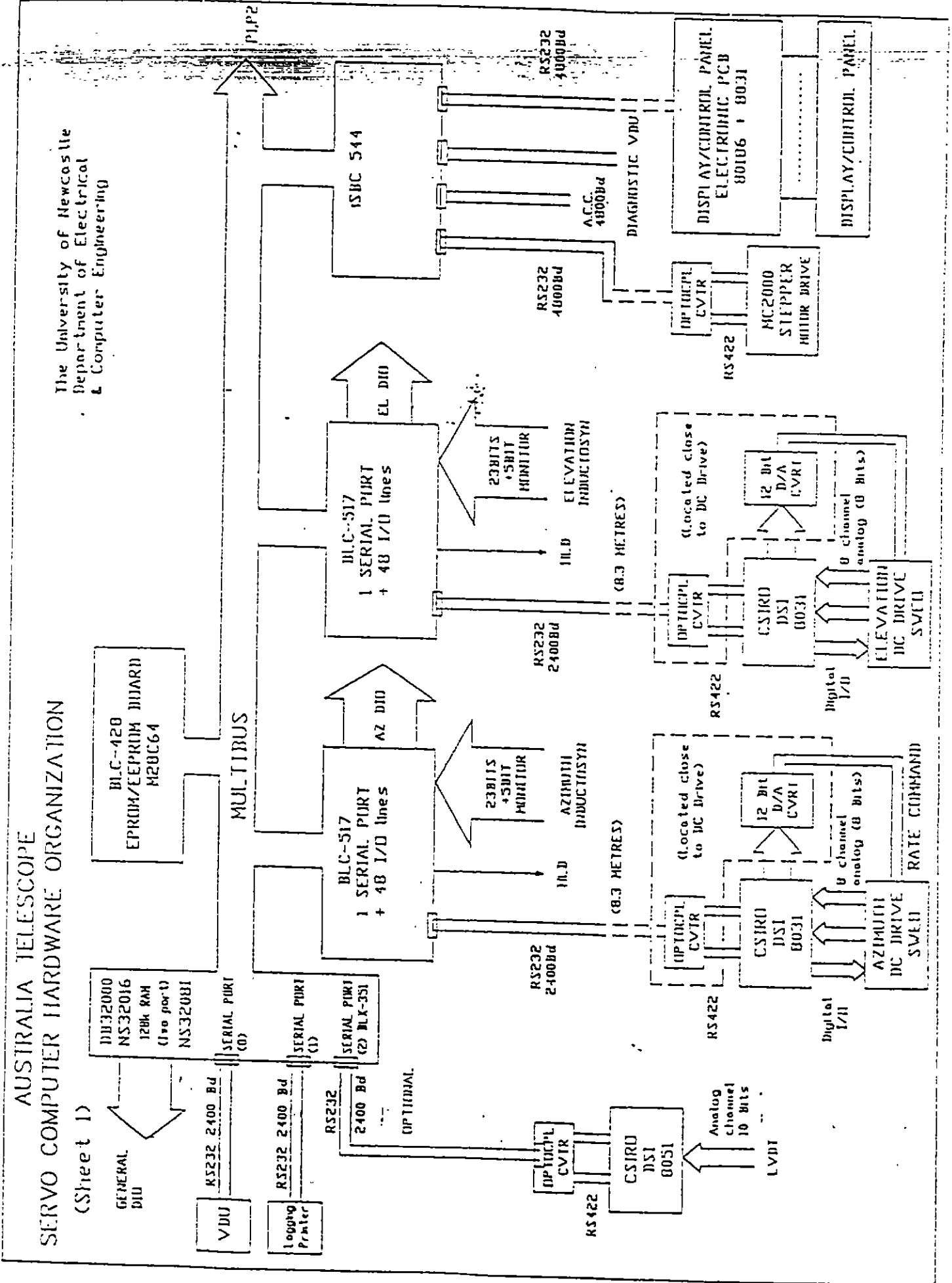


Figure 1. Compact Array computers

Ethernet

Figure 2



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Department of Electrical
& Computer Engineering

AUSTRALIA TELESCOPE
SERVO COMPUTER HARDWARE ORGANIZATION
(Sheet 1)

GENERAL DIU
10132000
NS32016
128k RAM
(128k par. 1)
NS32081

VDU
Logging Printer

MULTIBUS

SERIAL PORT (0)
SERIAL PORT (1)
SERIAL PORT (2) BLC-351

BLC-420
EPROM/EEPROM BOARD
M28C64

BLC-517
1 SERIAL PORT
+ 48 I/O lines

ISBC 544

RS232 2400 Bd
OPTICPL CVTR
CSIRO DS1 0031
Digital I/O
12 Bit D/A CVTR
8 channel analog (8 Bits)

AZIMUTH INDUCTION SYNTH
AZ DIU

23BITS +5BIT MONITOR
ELEVATION INDUCTION SYNTH
EL DIU

RS232 4000 Bd
DIAGNOSTIC VDU
DISPLAY/CONTROL PANEL
ELECTRONIC PCB
80106 + 8031
MC2000 STEPPER MOTOR DRIVE
DISPLAY/CONTROL PANEL

RS232 2400 Bd
OPTICPL CVTR
CSIRO DS1 0031
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12 Bit D/A CVTR
8 channel analog (8 Bits)

AZIMUTH DC DRIVE SWELL
RATE COMMAND

ELEVATION DC DRIVE SWELL

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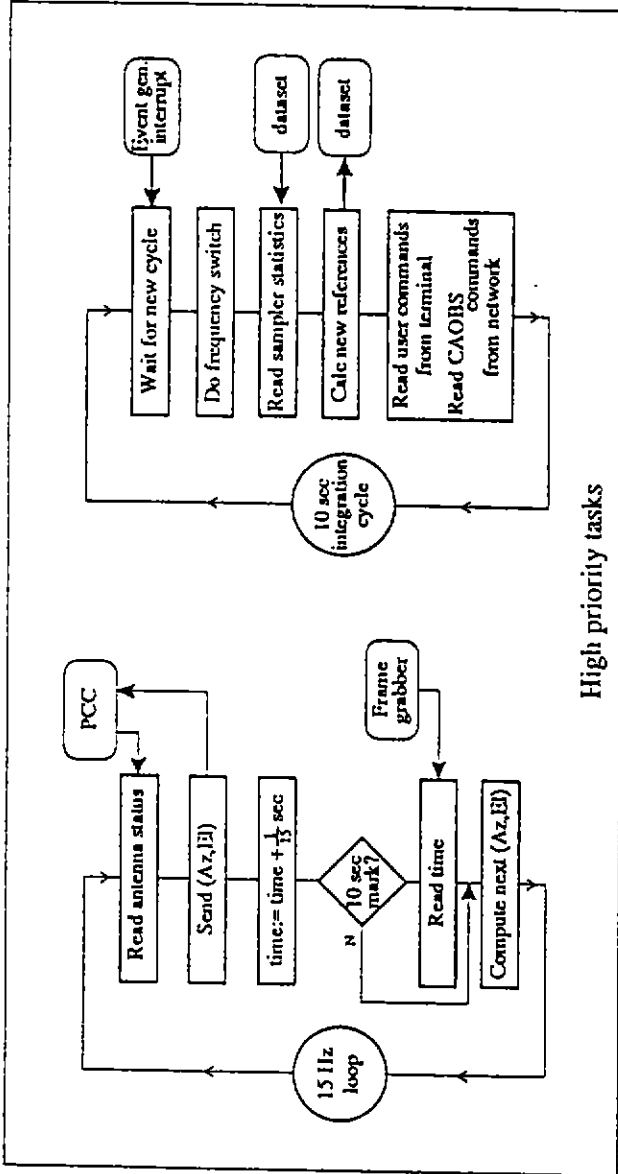
RS232 2400 Bd
OPTICPL CVTR
CSIRO DS1 0031
Digital I/O
12 Bit D/A CVTR
8 channel analog (8 Bits)

AZIMUTH DC DRIVE SWELL
RATE COMMAND

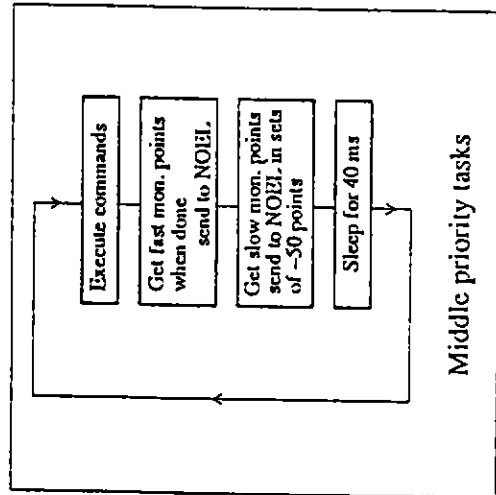
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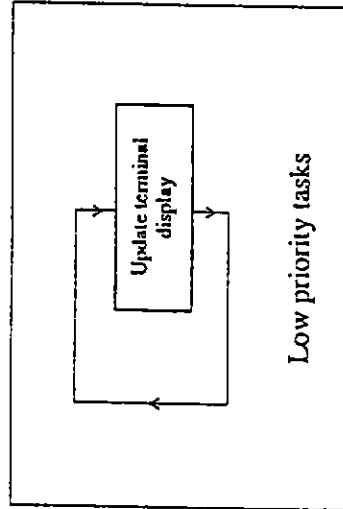
PIP2



High priority tasks



Middle priority tasks



Low priority tasks

Figure 3. ACC task summary

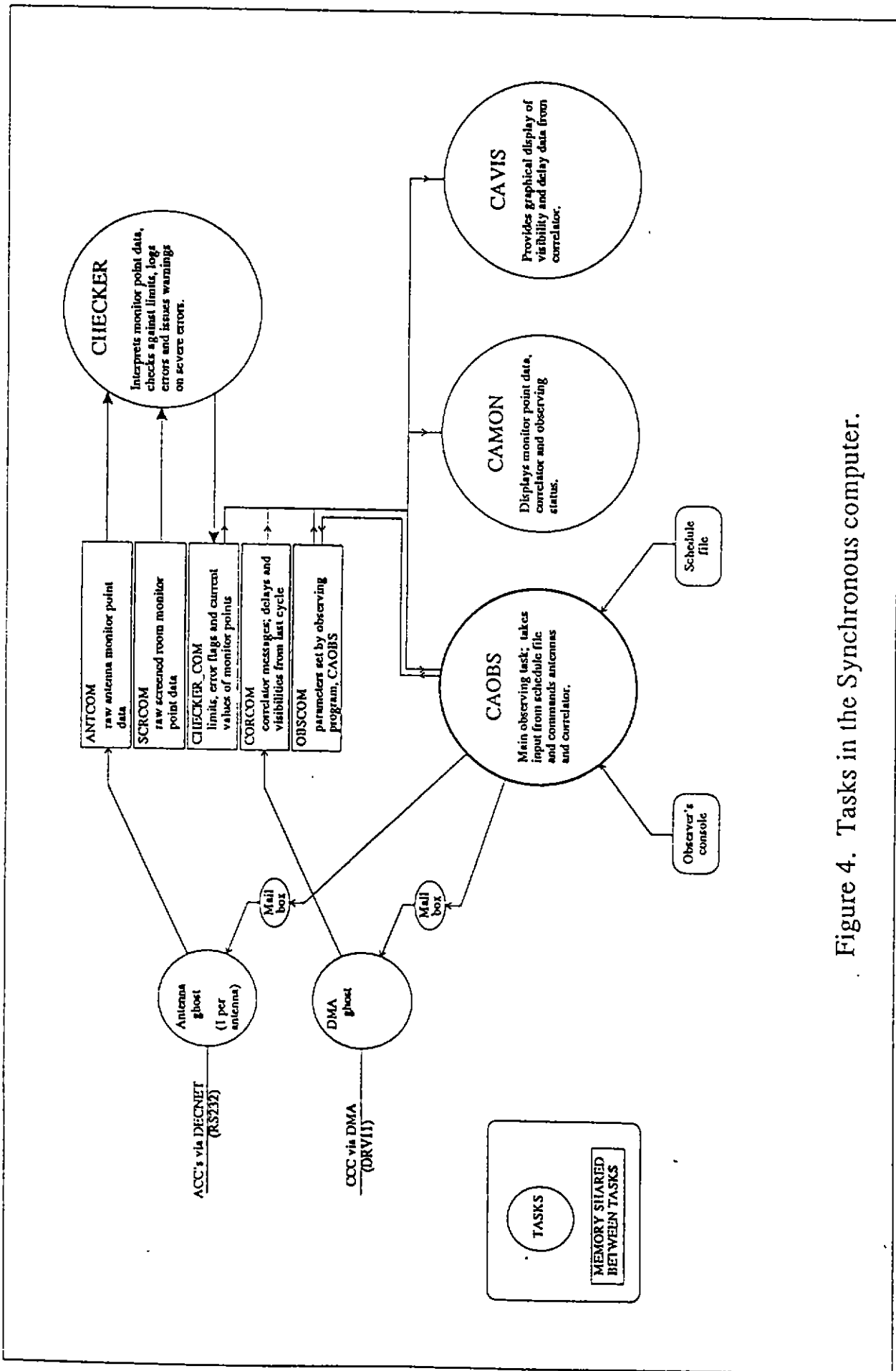


Figure 4. Tasks in the Synchronous computer.