A range of low-noise amplifiers have been designed for both the new and the proposed observing bands for the Australia Telescope National Facility Compact Array antennas. The amplifiers, which operate in three bands in the range 16 GHz to 115 GHz, use indium phosphide based high electron mobility transistor, monolithic microwave integrated circuit technology. We will describe the amplifier design and report the room temperature on-wafer performance of these amplifiers.

1 Introduction

The Australia Telescope Compact Array, situated near Narrabri in northern New South Wales, consists of six 22-metre dish antennas. Five of the antennas are moveable on an east-west rail track three kilometres in length, while the sixth dish is fixed at a position three kilometres further to the west. At present, the Compact Array can operate at a range of frequencies in the 1 to 10 GHz band.

The Australia Telescope National Facility is currently enhancing the frequency coverage of its Compact Array. Receiver systems covering two new observing bands, the 12 mm band (16-25 GHz) and the 3 mm band (85-115 GHz), are being designed and will be installed in the ATCA antennas. Provision has been made to add, later, a 7 mm band (30-50 GHz) to the new receiver package. A number of low-noise, indium phosphide based, monolithic microwave integrated circuit (MMIC) amplifiers have been designed to cover the new observing bands.

Indium phosphide based high electron mobility transistors (InP HEMT), cooled to cryogenic temperatures, have been used in the construction of wide band, millimetre-wave receivers with noise performance comparable with SIS mixer receivers [1]. Cryogenically cooled InP HEMT MMIC low-noise amplifiers have been reported with noise figures as low as 0.4 dB at 100 GHz [2].

2 Amplifier design, fabrication and performance

The MMIC amplifiers were designed for the advanced, 0.1 micron, InP HEMT process recently developed at TRW [3]. As the lowest noise performance has been reported for cryogenically cooled amplifiers, we intend to cool these amplifiers, but the transistor models are only valid for a range of temperatures around 25°C, and do not explicitly model device performance at cryogenic temperatures. Consequently, circuit performance was optimized for low noise, flat gain, good input and output return loss and stability using the (room temperature) models that were available.

When indium phosphide based transistors are cooled, their transconductance increases, leading to greater gain and lower noise. Some circuits, which are quite stable at room temperature, may become unstable, due to the increase in device gain, at cryogenic temperatures. This was a concern when the amplifiers were designed, as it is difficult to assess the stability of a circuit at cryogenic temperatures, especially at the higher frequencies where active device models and passive element models may not
be sufficiently accurate. As a result, a conservative approach was taken in the design, with every effort made to ensure the stability of the resulting circuits at cryogenic temperatures. In general, the stability factor, $K$, was kept greater than 4 at frequencies within the nominal band of the amplifier, and greater than 10 outside that band.

Source inductance was included in all HEMT stages to aid in levelling the gain across the band and to improve the amplifier stability. The source inductance in the first transistor is generally greater than that in the other transistors, and allows the input return loss of the amplifier to be increased while maintaining low noise figure in the design. Relatively large capacitors (10 pF in parallel with 1.2 pF) are used for RF bypass in the gate and drain bias networks. Small series resistances are used in the gate and drain bias lines to damp out any parasitic resonances.

The gain, input return loss and output return loss of the amplifiers, reported below, have been measured on-wafer, and only at room temperature.

### 2.1 The 16-25 GHz amplifier

This amplifier was designed for minimum noise in the 16 to 25 GHz band with flat, 30 dB gain and input and output return losses greater than 15 dB over the whole band, and better than 20 dB midband. The circuit uses three HEMTs, each with a total gate width of 120 microns, and is 3.1 mm x 2.25 mm. The simulated performance of the amplifier is shown in Fig. 1(a). Fig. 1(b) shows the layout of the amplifier circuit. Typical amplifier performance, shown in Fig. 1(c), is remarkably similar to the simulation. The main difference is that the measured input return loss near 25 GHz is 10 dB, rather than 18 dB as simulated. The noise figure of the amplifier, measured on-wafer up to 25 GHz, is

![Fig. 1](image_url)
shown in Fig. 1(d). The noise figure is somewhat higher than that predicted in the simulation.

2.2 The 30-50 GHz amplifier

This amplifier was designed for minimum noise in the 30 to 50 GHz band with flat, 30 dB gain and input and output return losses greater than 15 dB over the whole band, and better than 20 dB midband. The circuit uses a 4-finger HEMT, with a total gate width of 120 microns, in the first stage, followed by 4-finger HEMTs, each with a total gate width of 80 microns, in the three subsequent stages, and is 2.7 mm x 2.25 mm. The simulated performance of the amplifier is shown in Fig. 2(a). Fig. 2(b) shows the layout of the amplifier circuit.

The typical amplifier performance, shown in Fig. 2(c), is, again, similar to the simulation. The measured input and output return losses are both lower than that predicted by the simulation, especially at the high frequency end of the band. The noise figure of the amplifier, measured on-wafer between 30 and 39 GHz, is shown in Fig. 2(d).

![Fig. 2 30 - 50 GHz amplifier](image)

![Fig. 2](image)

2.3 The 85-110 GHz amplifier

This amplifier was designed for minimum noise in the 85 to 115 GHz band with 12 to 14 dB gain up to 110 GHz. Input and output return losses were designed to be greater than 10 dB in the frequency range 92 to 115 GHz, and better than 15 dB in the frequency range 95 to 105 GHz. The circuit uses four, 4-finger, HEMTs, each with a total gate width of 40 microns, and is 2.1 mm x 2.25 mm. The simulated performance of the amplifier is shown in Fig. 3(a). Fig. 3(b) shows the layout of the
amplifier circuit.

The typical amplifier performance is shown in Fig. 3(c). The measured input and output return losses are both lower than that predicted by the simulation. The gain is higher than predicted, but falls off quickly at the high frequency end of the band. The noise figure of the amplifier, between 90 and 98 GHz, is shown in Fig. 3(d). The estimated accuracy of the on-wafer noise figure measurement is ±1 dB. The noise figure is similar to that predicted by the simulation.

Conclusion

Low noise amplifiers, operating in three bands in the range 16 GHz to 115 GHz, have been described. The accuracy of the simulations indicates that circuits can be designed to work up to 120 GHz by relying on standard component models and foundry device models, with higher simulation accuracy being achieved at the lower frequencies.

References
