RF DESIGN OF A WIDEBAND CMOS INTEGRATED RECEIVER FOR PHASED ARRAY APPLICATIONS

SUZY A. JACKSON

CSIRO Australia Telescope National Facility and Macquarie University, Sydney, Australia.

(e-mail: Suzy.Jackson@csiro.au)

Abstract. New silicon CMOS processes developed primarily for the burgeoning wireless networking market offer significant promise as a vehicle for the implementation of highly integrated receivers, especially at the lower end of the frequency range proposed for the Square Kilometre Array (SKA).

An RF-CMOS "Receiver-on-a-Chip" is being developed as part of an Australia Telescope program looking at technologies associated with the SKA. The receiver covers the frequency range 500 MHz to 1700 MHz, with instantaneous IF bandwidth of 500 MHz and, on simulation, yields an input noise temperature of <50 K at mid-band. The receiver will contain all active circuitry (LNA, bandpass filter, quadrature mixer, anti-aliasing filter, digitiser and serialiser) on one 0.18 µm RF-CMOS integrated circuit.

This paper outlines receiver front-end development work undertaken to date, including design and simulation of an LNA using noise cancelling techniques to achieve a wideband input-power-match with little noise penalty.

Keywords: CMOS LNA, system-on-chip, RFIC, integrated receiver, astronomy, Square Kilometre Array, radio-on-chip

1. Introduction

The scientific demands of large collecting area and large field-of-view (FOV) below 1 GHz mean that the SKA will require either a large number of elemental receptors (aperture phased array) or a smaller number of flux concentrators, each with some form of focal plane array (FPA) to extend the low-frequency FOV. In either case, a large number of inexpensive, high performance receivers are required.

One method of realising the cost reductions necessary to fabricate these systems is to design a single integrated circuit containing the entire receiver chain. The fabrication processes heretofore popular for amplifiers and mixers in radio telescope receivers, namely gallium-arsenide (GaAs) and indium-phosphide (InP), whilst offering high performance in terms of noise temperature and high transistor f_T (unity current gain frequency), are unsuited to the integration of complex digital logic and are comparatively expensive to manufacture.

Current trends in RF-CMOS performance indicate that a single-receiver IC implemented using advanced deep-submicron CMOS processes is likely to meet the receiver requirements of the SKA, at least by the time the array is constructed post-2010. In order to begin the development process and gain valuable design experience, a rather more modest receiver is being developed using current CMOS processes. This paper describes work to-date in development of this prototype receiver.

2. CMOS for RF

Radio-astronomy receivers generally use either GaAs or InP transistors and MMICs as active elements. GaAs and InP are applicable to low-noise, high frequency use, as the processes offer very high f_T, low-noise transistors, and perform well when cooled to cryogenic temperatures. However, InP and GaAs are not amenable to the implementation of complex digital circuits (such as multi-bit

samplers) due to their relatively high power requirements, low integration levels, and prohibitive wafer costs.

Silicon CMOS is a mature process which is extremely popular for use with digital logic and low frequency analogue circuits. Enormous resources have been invested in CMOS over the last two decades in order to improve digital logic speed and levels of integration. More recently, the growth of the wireless networking and mobile telephone markets, with their requirement for low-power, inexpensive, highly integrated RF systems, has further driven developments in silicon CMOS, as well as creating a new Silicon Germanium (SiGe) process which adds Heterojunction Bipolar Transistors (HBTs) to a standard CMOS process (Subbana et al. 2000).

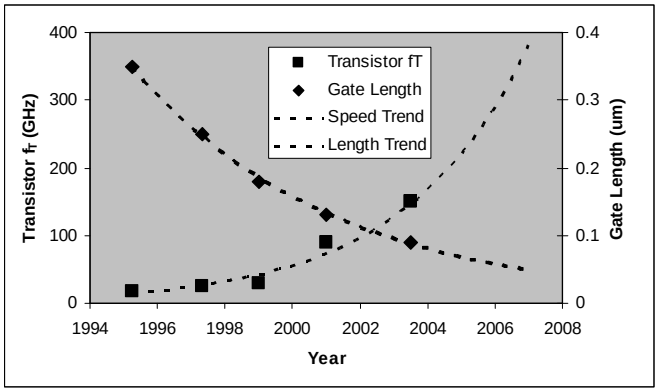

Figure 1. CMOS Performance Trends

Notwithstanding promising developments with SiGe, modern deep-submicron CMOS processes are becoming more applicable for use in radio astronomy receivers as feature sizes decrease and transistor f_T increases. By extrapolating representative performance and feature sizes from the last five CMOS generations (IBM 2004), as shown in Fig. 1, we see that by the time the SKA is built, cutting edge silicon CMOS processes may offer transistor f_T of around 400 to 500 GHz, exceeding the performance of today's mainstream GaAs processes. As such, it is anticipated that CMOS could be the technology of choice for building large numbers of high performance, inexpensive receivers covering the frequency range of 1 to 10 GHz.

3. CMOS low noise amplifiers

One of the key challenges faced in implementing a radio astronomy receiver in RF-CMOS is that of designing a Low Noise Amplifier (LNA) having adequate RF bandwidth and sufficiently low noise operation. Lee (1998) works through a derivation of MOSFET noise parameters. Whilst this approximation is accompanied by numerous caveats, most notably the validity of the three noise coefficients in the deep-submicron regime, it still provides some insight into the improvement in minimum noise temperature ($T_{N(min)}$) with increased process f_T:

$$T_{N(\min)} \approx 290 \frac{2}{\sqrt{5}} \frac{f}{f_T} \sqrt{\gamma\delta\left(1-|c|^2\right)} \qquad (K)$$

Where γ is the body effect coefficient,
δ is the gate noise coefficient, and
c is the gate/drain noise correlation coefficient.

f_T is the unity current gain frequency

NB: Use γ=2, δ=4, |c|=0.395 for typical short channel process

Applying this equation to the published data for current processes allows us to plot the trend for minimum LNA noise temperature as shown in Fig. 2, both for a nominal 10 GHz SKA RF frequency and a more modest 2 GHz. The latter figure is more applicable to a demonstrator project using current processes. In addition, noise performance of some representative CMOS LNAs is shown.

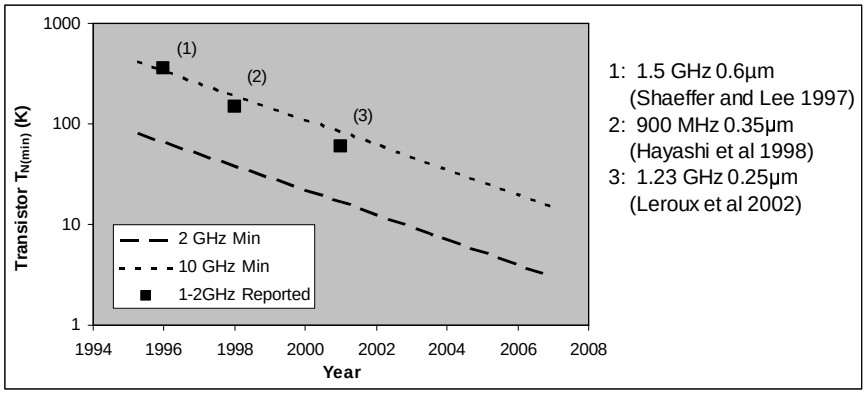

Figure 2. CMOS Minimum Noise Trends

The vast majority of CMOS LNAs encountered in the literature (Leroux et al. 2002; Hayashi et al 1998; Shaeffer and Lee 1997) are designed for low power portable devices, such as mobile telephones, wireless network adapters, and global positioning receivers. Power consumption in these typically battery powered devices is critical, and noise performance is traded in order to reduce power. The SKA application does not impose the strict operating power requirements of portable devices, so some design latitude is allowed.

Returning to the bandwidth – noise trade-off, we note that topologies providing a resistive input power match, such as the common-gate or shunt-series topology, add a significant noise penalty. In the case of the common-gate amplifier, this noise penalty is around 200 K (Lee 1998).

In order to achieve noise temperatures close to T_{min} across the operating band, the usual practice is to employ some method of impedance transformation on the LNA input. Accepted approaches include ¼ wave filter structures (large and noisy at low frequencies, and not amenable to integration on wafer) or, alternatively, using reactive components (inductive degeneration) to realise an impedance transformation for a common-source transistor. It is difficult to extend these topologies to broad band operation using integrated passive components, as the losses in the matching networks then dominate the LNA noise.

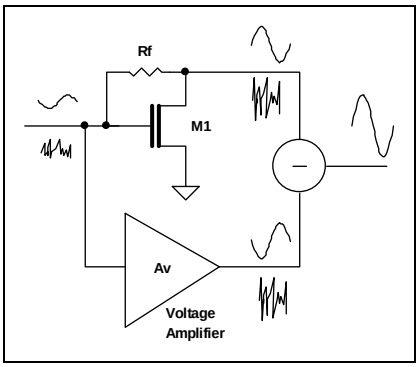

Figure 3. Noise Cancelling Principle (Bruccoleri 2004)

With the improvement in active device gain-bandwidth product it is possible, in principle, to depart from conventional RF topologies and to implement amplifiers using a variety of circuit designs hitherto restricted to the low frequency or video domain (Gray et al. 2001). One such approach is to utilise feedback or feedforward techniques to accomplish a broadband power match without sacrificing the amplifier noise match. The recent work of Bruccoleri (2004) is particularly relevant, as it establishes a means whereby the power matching and signal amplifying parts of the LNA may be separated and, by careful design, noise currents in the matching network can be cancelled in the amplifying section.

Fig. 3 demonstrates the generalised noise cancelling principle. M1 and R_f form a shunt-series matching amplifier, with modest noise performance. Drain current noise in M1 is present as a voltage at the drain node and as an in-phase voltage at the gate node, whereas the input signal is in anti-phase between the drain and gate nodes. It is possible therefore to cancel out M1's drain current noise using a voltage amplifier of the same gain as the matching network, and a difference network. In practice the voltage amplifier adds its own noise, but the power matching constraints for this amplifier are greatly relaxed, and it can be matched instead for low noise.

4. A prototype integrated receiver

An overall schematic for the prototype receiver IC is shown in Fig. 4. The receiver uses image-free direct conversion of a 500 to 1700 MHz RF band to baseband. The 500 MHz bandwidth complex baseband signals are digitised by two 512 Msps ADCs.

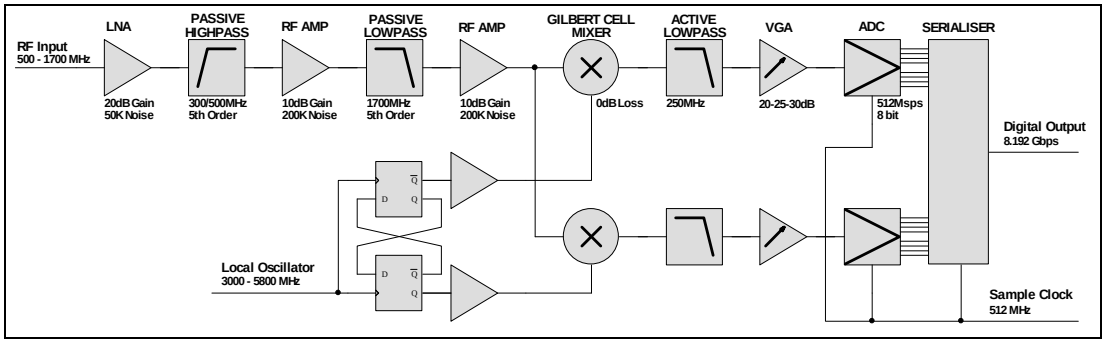

Figure 4. Receiver RFIC Overall Schematic

The RF bandwidth, IF bandwidth and noise specifications for the receiver have been optimised so that acceptable performance is possible with contemporary CMOS processes. Local Oscillator (LO) and sample clock inputs, and digitised receiver output, connect directly to fibre interfaces, reducing leakage into the RF input. The conversion chain is designed to maximise dynamic range, so that it may be used in comparatively hostile RF environments.

5. Low noise amplifier

The topology chosen for the LNA (Fig. 5) is based on the active feedforward noise-cancelling approach, using a common-gate matching stage with a common-source amplifying stage. In such an arrangement the noise cancelling criteria are met when the voltage gain of each signal path is equal.

The main amplifying transistor (M2) dominates the noise of the circuit, so the design process starts with the choice of an appropriately sized transistor and selection of a minimum noise bias point. Simulations on a simple test circuit showed that the minimum noise (and maximum transconductance) for the process of interest (IBM 0.18 μm) was achieved at around 20 μA/μm drain current density, and that noise temperature decreased with increasing gate width. However, gate-source capacitance (C_{gs})

and gate-drain capacitance (C_{gd}) also scale with gate width. As this capacitance is across the source, it degrades the power match and introduces significant gain slope. A compromise was reached at 700 μm gate width, this figure being distributed across 200 gate fingers to minimise gate resistance.

The cascode transistor (M3) improves gain somewhat by reducing the Miller capacitance. Some inductance (L1) in series with the load resistor (R2) on the amplifying side peaks the gain slightly, improving both the gain slope and the noise cancelling across the RF bandwidth.

A second stage (M4 and M5) gives additional gain and provides the differencing action between the amplifying and matching subcircuits. This stage also provides a high input impedance, maximising gain in the first stage and matching the amplifier to a 50 Ω load.

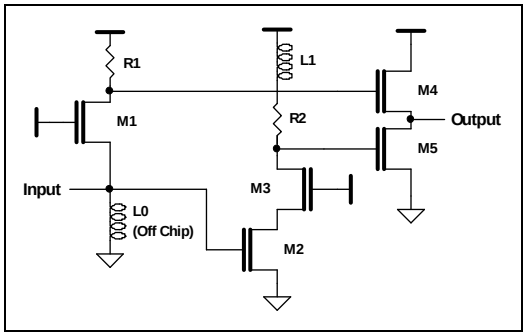

Figure 5. Simplified LNA Schematic

The amplifier is laid out in a six-layer process, as shown in Fig. 6. It occupies 0.08 mm^2 of die. A 33 pF off-chip coupling capacitor and 22 nH shunt inductor provide a DC bias feed for the common-gate stage.

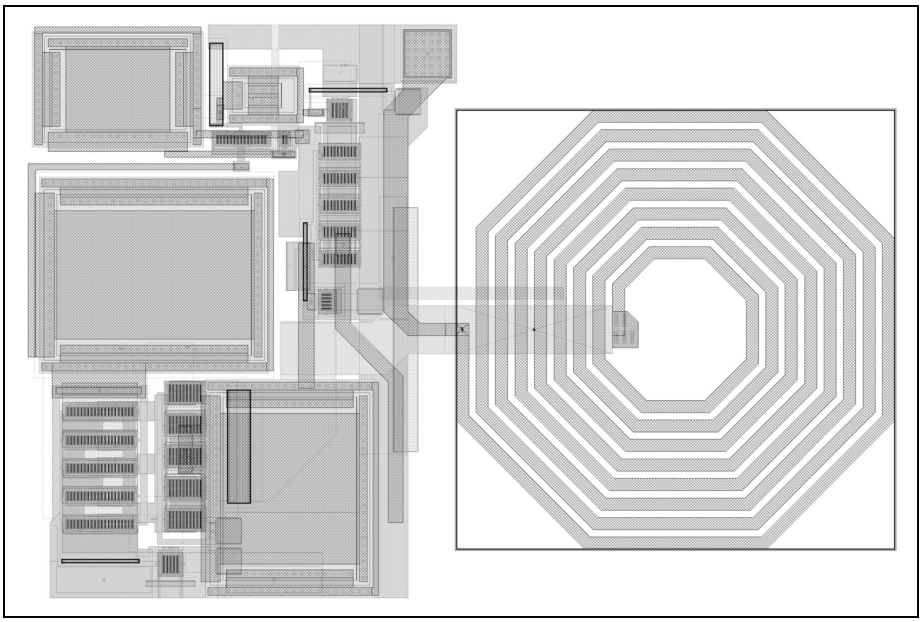

Figure 6. LNA Layout

Simulated results for the amplifier are shown in Fig. 7. Wiring parasitics account for approximately 2 dB gain and 8 K additional noise at 1.7 GHz, mainly through increased capacitance to substrate. Wiring parasitics also degrade the input return loss by approximately 1 dB. Note that the

simulated performance includes the effect of minimum sized input and output bond pads, as well as bondwires and off-chip input shunt inductor losses. The amplifier has more than 18 dB gain across the 500 to 1700 MHz RF bandwidth, with better than 50 K noise temperature between 600 and 1400 MHz (as a comparison the mid-band figure without noise cancellation is approximately 180 K). Input return loss (relative to 50 Ω) is approximately 8 dB across the band, whilst output match is better than 15 dB. Input match may be traded for noise temperature by varying the size of M2, whilst adjusting R2 to ensure the cancelling criteria are met. The amplifier has a 1 dB compression point of -4 dBm, whilst drawing 23 mA with V_{dd} = 1.8 V. It is possible to extend the lower cutoff frequency to 300 MHz by increasing the off-chip shunt inductance. Note that with a future implementation in 0.13 µm CMOS, one may expect a noise temperature of approximately 20 to 30 K at band centre with similar input match.

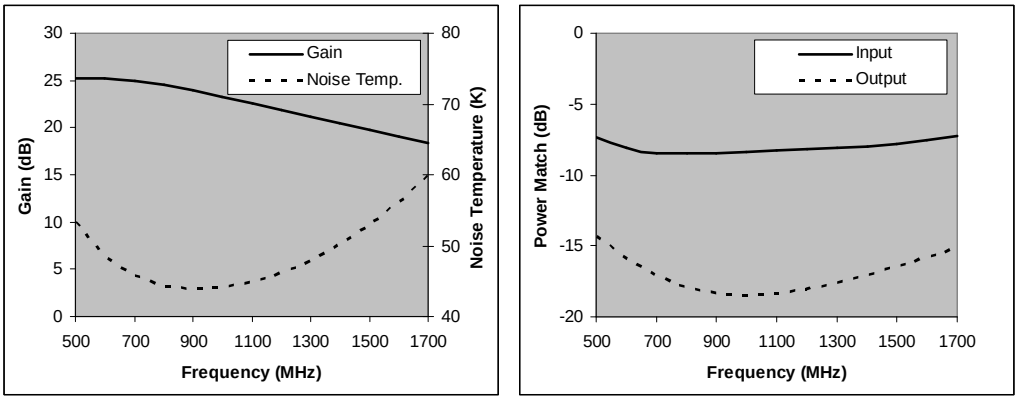

Figure 7. LNA Simulated Performance (Including Layout Parasitics)

6. RF amplifier

In order to ensure that the full dynamic range of the LNA is preserved, a moderate gain, moderate noise temperature, relatively high power RF amplifier (Fig. 8) was designed as a general purpose gain block. This amplifier utilises a simple inverter topology, with feedback to set the input power match at 50 Ω. M1 is biased with a conventional current mirror, whilst an additional DC feedback loop adjusts the bias on M2 to maintain the output at V_{dd}/2, ensuring maximum signal swing. M2 is sized to match a 50 Ω load.

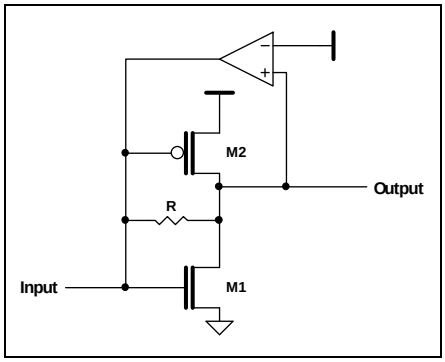

Figure 8. Simplified RF Amplifier Schematic

The amplifier is laid out in the same six-layer process as the LNA, and occupies 0.03 mm^2 of die. It is fully self-biasing. On simulation, the amplifier achieves 10 dB gain across a full decade bandwidth (200 MHz to 2 GHz), with <200 K noise temperature and >8 dB input and output return losses. The 1 dB compression point is +6 dBm at 1 GHz. This corresponds to a peak to peak voltage swing of 1.3 V with V_{dd} set at 1.8 V; the current drain is then 12 mA.

7. RF high-pass filter

The likely presence of strong interfering signals, especially those in the FM broadcast band (88 to 108 MHz), requires the use of a high-pass filter early in the signal chain. This filter (Fig. 9) comprises a fifth-order 300 MHz Chebychev filter, followed by a third-order 500 MHz Chebychev filter, the latter able to be bypassed by virtue of a CMOS switch. This arrangement is necessary because a potential application for the prototype receiver requires operation down to 300 MHz, with relaxed noise and input power match requirements.

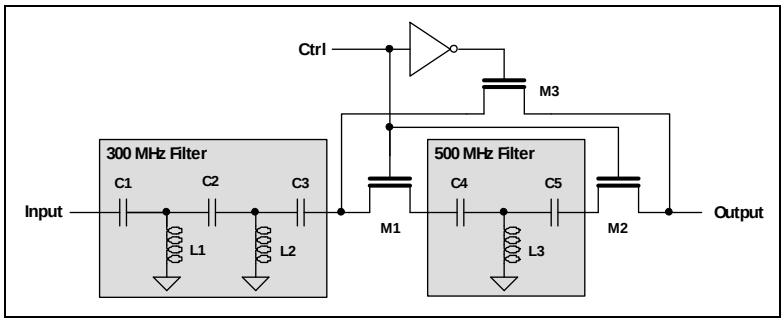

Figure 9. Simplified RF High-pass Filter Schematic

The simulated performance for the filter is shown in Fig. 10. The left hand plot shows the 300 MHz response, with the control input grounded, whilst the right hand plot shows the filter response with the control input held at 1.8 V, for a corner frequency of 500 MHz. Although the performance remains acceptable, the additional shunt capacitance of the switch (M1 through M3) is evident in the output return loss, especially with the 500 MHz filter switched in.

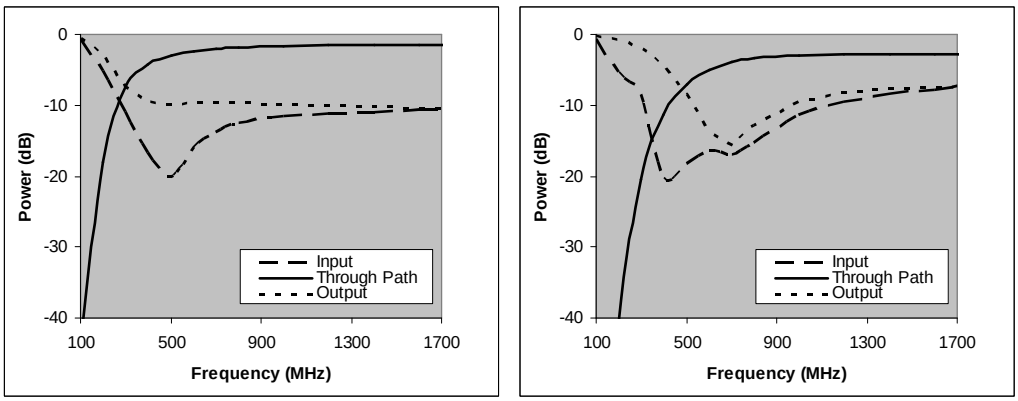

Figure 10. High-pass Filter Simulated Performance

8. Conclusion and further work

Results to-date of a development program for a CMOS integrated receiver, including an LNA with better than 50 K mid-band noise temperature and operation over a 500 MHz to 1700 MHz bandwidth have been described. Work performed so far on the prototype receiver indicates that some of the limitations of CMOS, such as substrate loss and poor quality passives, may be overcome by utilising circuit topologies developed for low frequency analogue and video applications. Testing of fabricated devices will begin in late 2004 and the full integrated receiver is scheduled for tests in early 2006.

Acknowledgements

This work is supported by The Australia Telescope National Facility (ATNF) and Macquarie University. The Australia Telescope is funded by the Commonwealth of Australia for operation as a National Facility managed by CSIRO. This work is funded by a Major National Research Facilities grant. I thank my supervisors, Dr Jeffrey Harrison (Macquarie University) and Dr Peter Hall (ISPO) for their patient guidance and wisdom, and for encouraging me to explore unusual circuit topologies.

References

Bruccoleri, F.: 2004, *Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Cancelling*, IEEE J. Solid-State Circuits. **39**, 275-282.

Gray, P. R., Hurst, P. J., Lewis, S. H., and Meyer, R. G.: 2001, *Analysis and Design of Analog Integrated Circuits*, 4th Ed, John Wiley and Sons, New York.

Hayashi, G., Kimura, H., Simomura, H., and Matsuzawa, A.: 1998, *A 9 mW 900 MHz CMOS LNA With Mesh Arrayed MOSFETs*, Symposium on VLSI Circuits, 84-85.

IBM: 2004, *RF-CMOS Process Specifications* [online], IBM Semiconductor, Available from: http://www-306.ibm.com/chips/techlib/techlib.nsf/literature/Foundry [Accessed 12 Mar 2004]

Lee, T. H.: 1998, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, Cambridge.

Leroux, P., Janssens, J., and Steyaert, M.: 2002, *A 0.8-dB NF ESD-Protected 9-mW CMOS LNA Operating at 1.23 GHz*, IEEE J. Solid-State Circuits. **37**, 760-765.

Shaeffer, D. K., and Lee, T. H.: 1997, *A 1.5-V 1.5-GHz CMOS low-noise amplifier*, IEEE J. Solid-State Circuits. **32**, 745-759.

Subbana, S. et al.: 2000, *Review of silicon-germanium BICMOS technology after 4 years of production and future directions*, Gallium Arsenide Integrated Circuit Symposium, 7-10.