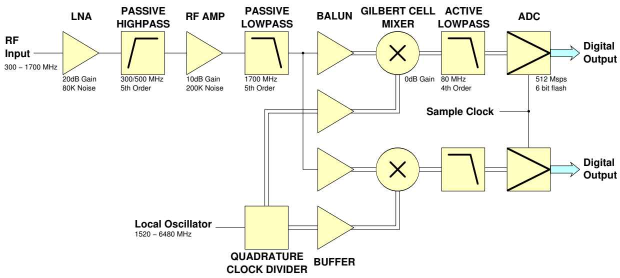
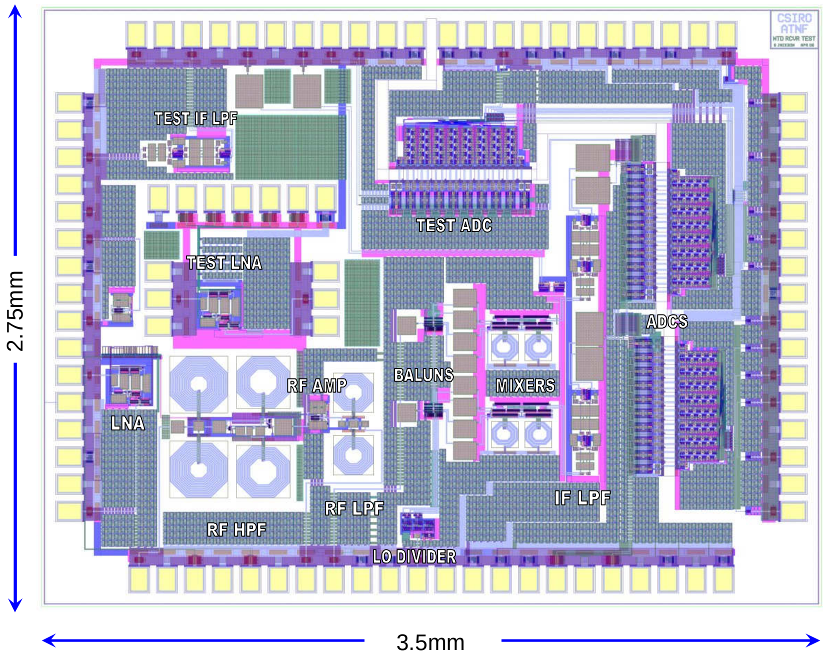
A Single-Chip RF-CMOS Receiver for SKA Pathfinders

Suzy Jackson (CSIRO ATNF), Peter Hall (International SKA Project Office),
Jeffrey Harrison (G2 Microsystems)

To achieve simultaneously the current mid-band SKA field-of-view (FoV) and collecting area specifications, millions of individual receivers are needed. Low-density, high wafer cost, GaAs and InP processes commonly used in today's radio-telescopes may not offer the cost and integration levels necessary to achieve an RF-system goal of under $5 per receiver. RF-CMOS and SiGe processes, with their low wafer costs and high integration levels, could be enabling technologies for SKA.

As part of a continuing research effort into receiver technologies for next-generation radio-telescopes, a single-chip RF-CMOS receiver has been developed to cover the 300 – 1700 MHz RF band. This receiver integrates a noise-cancelling LNA, RF filters and amplifiers, quadrature direct-conversion mixers, IF anti-aliasing filters, and six-bit ADCs into a commercially-available 0.18 µm RF-CMOS process. The receiver is a complete "RF to bits" solution in a single package. When coupled with a simple external LNA optimised for dense phased arrays or other complex feeds, the chip is a functional replacement for discrete RF systems in mid-band SKA pathfinders. Future designs, fabricated in faster CMOS processes may allow a complete, optimised, one-chip solution.





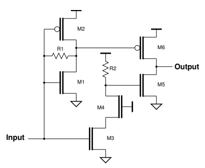
Design Overview:

The design covers an RF band from 300 – 1700 MHz, with a direct conversion to complex baseband. In principle the ADCs allow operation with up to a 512 MHz instantaneous RF bandwidth. For Australian NTD goals however the present chip incorporates an active low-pass baseband filter which limits the instantaneous bandwidth to 80 MHz.

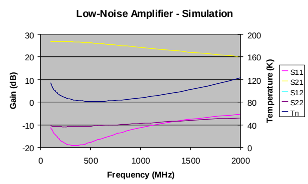
The receiver is implemented in a single 3.5 mm by 2.75 mm six-layer 0.18 µm RF-CMOS integrated circuit. We estimate an operational power consumption of ~1 W.

Low Noise Amplifier:

The Low Noise Amplifier (LNA) is a wideband noise-cancelling design, utilising a shunt-feedback matching amplifier and a cascode common source voltage amplifier. The circuit has inherently broadband performance, with T_n being 80 K mid-band, degrading to 110 K at the band edges. Gain is better than 20 dB to 2 GHz. It occupies 0.04 mm² and consumes 70 mW.

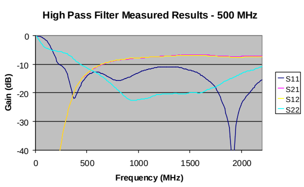


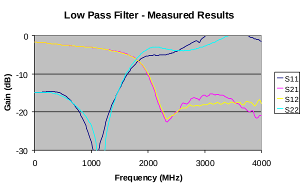
LNA Topology



RF Band Filtering:

RF band selection is performed by separate high-pass and low-pass passive Chebyshev filters. The high-pass circuit comprises a fifth-order 300 MHz filter, followed by a switchable 500 MHz third-order filter, allowing a selectable band edge. The low-pass filter is a single 1700 MHz fifth-order filter. The filters occupy 0.4 mm² and 0.09 mm² respectively. Measured results from a test chip are shown.



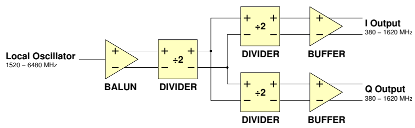


Mixer:

A pair of Gilbert-cell mixers perform direct conversion to complex baseband. The mixers use a fully-differential topology to minimise second-order distortion. Each mixer occupies 0.08 mm² and consumes 90 mW. Its accompanying active balun occupies 0.01 mm² and consumes 40 mW.

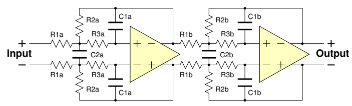
Quadrature LO Generator:

An accurate quadrature LO is generated from a four-times reference tone, using high-speed differential Current Mode Logic (CML) comparators and dividers.



IF Filter:

For the NTD application, the IF filter is a four-pole Chebyshev multiple-feedback design, using high-speed two-stage opamps.



ADC:

The ADC is a six-bit flash design, utilising two stages of averaging termination and interpolation, with distributed sample and hold. Rather than using comparators, the ADC uses fixed-gain error amplifiers. The output of each error amplifier is averaged with those of neighbouring amplifiers to reduce systematic offsets caused by process variations. The thermometer-to-binary encoder uses a fat-tree topology, with two stages of pipelining to increase speed. Under simulation, the ADC is capable of operating to better than 800 Msps with full 6-bit performance. Each ADC occupies 0.3 mm² and consumes 200 mW.