VSI Port Technologies

Report on a Search for Interconnect Technologies suitable for VSI [0], related Digital Correlators, and general High Speed Digital Data Streams.

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Introduction

The development of an electrical specification for VSI is more than choosing an acceptable connector, cable and pinout combination. It encompasses the more general problem of finding an efficient way of transferring increasingly large amounts of high speed data between cabinets, and within cabinets across backplanes to and from circuit cards and shielded modules. The cost of materials, time, complexity and board real estate have already become disproportionately high as data volumes exceed the capacity of traditional technological solutions.

Accessibility

There are clear advantages if the specification has its roots in a similar, familiar and much larger market, preferably governed by recognised standards. Networking protocols and dedicated data cables in popular equipment are obvious candidates for consideration.

For example, the generalised definition of DTS, expounded as “equally applicable to recording (disc, tape, optical), and *real-time or near-real-time data transmission over networks* or dedicated wires” suggests even the possibility of adopting a high level network protocol such as Ethernet with all its existing paraphernalia. In this case the excess capabilities in permanent point to point applications would trade off against the added versatility and ready availability of interface cards and drivers.

At the other extreme a popular high performance connector could provide the basis for a direct-connect interface, and networking facilities when required would necessarily be embodied in a DTS. Either way global access to products and their documentation is an imperative for VSI.

Auxiliary Functions

A trend evident in contemporary cabled data protocols is the inclusion of simple low level structures to help configure and verify correct operation of the interface. These include reporting connectivity, activity and status of transceivers, the type, model and configuration of "other end" equipment, forcing loop-back etc. In some cases redundant codes also provide command sequences between physical layer components at either end of the link.

System robustness may be enhanced by adding some such ideas to VSI, eg. provide the means for a DTS to identify the source of particular bit streams in a multi-cable interface.

Compatibility

There is a natural tendency to retain past practices in the name of compatibility. However the familiar ECL/ribbon-cable/IDC transitions format has become relatively expensive in terms of $, real-estate, dissipation and power supplies, when compared with alternatives now available. In any case the possibilities of cross-connecting existing systems by simple conversion cables are few and have generally been eschewed in favour of inserting an active device such as the S2 VIA.

There would seem to be no real barrier to using a completely different technology for the VSI, save only that its logical format allows a straightforward interface to be constructed, if necessary, to connect to an older system.

RFI & EMI

Open cables carrying high speed data are inevitably sources of RFI, not only from the signal waveforms but general 'garbage' from the source and destination circuits. Given the sensitive locations of much VLBI equipment, where screened rooms are not always available, a move to fully shielded cables seems inevitable. Strict statutory requirements for new equipment now in force around the world also point the same way.

Shielding also enhances EMI, a pertinent issue as differential ECL clock signals on ribbon cables have proved fairly vulnerable to fast transients associated with switched inductive loads (eg. air conditioner compressors). Differential signals with soft switching also greatly reduce ground currents and transients, and when carried in wide bandwidth screened cables provide the best option for copper connections.

VSI Port Proposals

Context

VSI is evolving in the context of current recorder type DTS's with capacities from 128Mbps to 2Gbps, with expected extensions towards 8Gbps on generalised DTS's in the near future. Current VLBI DAS's have one and two-bit sampled IF bandwidths from 62.5kHz to 64MHz and emit their data as 8 to 64 bit streams at rates from 125ksps to 32Msps. (Samples from 64 and 32MHz bands are demuxed down to 32Msps to match the present recorder input rate.) Expansion of the aggregate bit rate is likely to involve increasing interface bit rates to 64 and possibly 128Mbps before increasing the number of streams.

In many installations the available aggregate DAS output exceeds the DTS capacity by a significant factor so there are potentially many ways of choosing the set of active streams and their bit rates. When an experiment requires less than full capacity the range of permutations and combinations may further increase dramatically.

VSI Port Concept

To always design in an interface accommodating the maximum anticipated number of bit streams at the maximum possible rate would be expensive and unreasonable; to require the DTS to support arbitrary selections of bit streams and rates from this wide parameter space, doubly so. Consequently a modular design for the interface has been developed to give an efficient structure for small capacity systems while providing ready extensibility for large ones.

The formal interface model detailed below is based on the concept of a logical port with 1Gbps capacity. This figure arises naturally from a range of suitable technology. It compares well with current equipment, matching or exceeding the capacity of all recorders except the four-headstack MkIV. At the other end of the scale it is twice the interface capacity, but eight times the recording capacity, of the S2.

The port width of 16 bit streams compares with interfaces 8 wide for K4 and 16 for S2, specifications of both 8 and 16 in the Draft Proposal (pp.4 & 5), and 32 and 64 for the internal interfaces in VLBA and MkIV. The lower prescribed channel rate at 32MHz matches the normal interface clock on S2, VLBA and MkIV, and the bit stream rate CLOCK is always available so conversion to all current formats is well supported.

The Interface Model conforms with the Draft Proposal except that validity data is separated from the bit streams and placed in its own port(s). Also the proposed implementations use positive logic in the forms of PECL and LVDS rather than traditional ECL as specified.

Model features M1 to M9 define the necessary basic parameters of data transport across the Interface. M10 to M12 address the next level up, to make the description sufficient for DAS and correlator builders to design their interfaces with the DTS. Model specific nomenclature is explained briefly in the local glossary, MN, at the end.

Interface Model

M1. A VSI comprises one or more identical ports.

M2. Port capacity is 1024Mbps or more.

M3. Each port provides 16 data channels, a 1PPS channel and possibly other channels, all of which may transport a generic bit stream.

M4. Channel rates of 64Mbps and 32Mbps, plus possibly others, are provided.

M5. A bit stream CLOCK signal is available at the receiving port with rising edges nominally centred on channel time cells.

M6. 1PPS is exerted for one period of CLOCK. 1PPS transitions coincide with bit stream transitions. Any bit-serial data formats commence synchronously with 1PPS. Data coincident with 1PPS are considered to be the first data of the second.

M7. Validity data when required is carried on its own ports with channel allocation and stream formats identical to the associated signal data port.

M8. All active ports in a VSI are programmed/formatted identically.

M9. Connecting cable assemblies are reversible.

M10. A VSI need only comprise sufficient ports to support the gross capacity of the host equipment when operated at 32Mbps channel rate.

M11. A receiving port may be programmed to have 1, 2, 4, 8 or 16 active channels at each available channel rate, consistent with the maximum and minimum gross capacities of the host equipment. Data may be transmitted in more than the programmed number of channels but any excess will be ignored.

M12. DTS ports include a full cross-bar to select and match external to internal data channels.

MN. Nomenclature:

CLOCK	Bit stream clock as defined previously (Draft Proposal).
1PPS	1PPS as defined previously.
BS[n]	Bit Stream n " "
P[m], m=0,1,...	Port m.
PD[n], n=0..15	Port (or Parallel) Data channel n.
PD[m,n]	Data channel n on port m.
PCLK	Port (or Parallel) Clock, at the data channel rate.
PCE	PCLK Enable, at the bit stream rate (ie CLOCK rate).
P1PPS	Port 1PPS.
32/64*	MHz. Indicates channel rate in some port designs.
PID	Port IDentifier, a 16-bit binary number. See Appendix.
HPD	Hot Plug Detect " "
V+	+5V auxiliary power rail " "
SDA	Serial DAta
SCL	Serial CLock

Notes

M1, M3 and M5 ensure each port may stand alone, facilitating distributed processors.

M3 "other channels" may carry auxiliary timing information, port identification (PID), parity etc., not essential to VSI or port operation. Details t.b.a. following discussion.

M4 recognises the large base of current equipment with 32MHz system clocks whereas 64MHz is the expected norm for new CMOS instrumentation.

Minimal conformance with M4 does not constrain the bit stream rate (CLOCK) which may be the same as, or any binary fraction of, the channel rate (PCLK) in such port structures.

M7 ensures the efficient use of resources since validity information is not required across many interfaces.

M8 enhances expandability by deliberately constraining multiplexing and formatting options. It thereby simplifies programming structures and ensures that the interface complexity of terminal systems (DAS, DIB etc) grows only linearly with the number of ports, rather than as the square of the total number of channels.

M10 codifies what is implicit in para Operation of the DIB in the Draft. The full corollary is an extension of Other notes #4 to the 'channel domain'. ie. If the DAS sample rate exceeds the maximum channel rate, *or the number of selected sample bit streams exceeds the number of data channels,* the DAS has the responsibility to do the necessary (de)multiplexing before presentation to the interface.

M12 allows the DAS (correlator) to maintain a consistent bit stream mapping to the interface while facilitating M11. M12 and M11 together also provide a practical level of flexibility for the DTS in its own right.

M12 and M10 imply a complete system to connect DAS sample data streams to internal DTS data channels. The DAS is responsible for selection, demultiplexing (fast data) or combining (slow data) for the interface, and the DTS for selecting (in the sense of M11), and reordering bit streams.

Bit Stream Formats

While VSI and the DTS model are explicitly indifferent to data contents, sample formats and the way data is (de)multiplexed into generic bit streams are closely related subjects of interest to DAS and correlator builders alike. They are also relevant to the end user scheduling configurations for each experiment, so a consistent approach will benefit all concerned. The subject is left further consideration.

Proposed Port Implementations

Examination of a wide range of network and cabled data protocols and component catalogues yielded three suitable technologies on which to base a VSI. These are (1) fully serialised PECL SERDES (q.v.) with data, clock and synchronisation information

transmitted together in a single bit stream; (2) partially serialised LVDS SERDES with data in three streams transmitted in parallel with a clock signal in a small format cable; and (3) direct parallel transmission with LVDS interface chips transporting each data and timing channel on its own pair of lines.

More than one practical connector and cable combination was identified for each technology, including off-the-shelf and DIY cable assemblies, giving a total of nine VSI candidates. Most convey one Port per interconnect but two carry multiple Ports, thus minimising the number of cables at the cost of concentrating large amounts of data through one physical interface. At least two connector families are represented for each technology. Given the diversity of preferences expressed by the community all candidates are presented for consideration.

In both SERDES proposals the model interface is between the host bit streams and the port chipset, defined by a table of signal to pin allocations. Separate specifications are provided to define the physical interconnect between the chips across port connectors and the cable assembly. This distinction between logical and physical interfaces is unnecessary for the direct ports and only a single definition is required.

Bit streams/CLOCK running up to 128MHz and serial data to 1280Mbps command respect and need to be routed on well defined single-ended and balanced microstrip transmission lines respectively. Some care has been taken when assigning signals to chip and connector pins, to provide clean non-intersecting routing on the top PCB layer simultaneous with straightforward cable termination in DIY assemblies. Commercial cables made to a predefined standard were only considered if reasonable routing solutions were possible.

Component parts are specified from a small number of major manufacturers with global presence and universally accessible (ie. Internet) catalogues. Each proposed standard is followed by a list in brackets {} of suitable components found therein. True equivalents from other sources may of course be substituted.

A VSI CORRCLOCK port definition has been included. This provides the correlator to DOB timing and control functions using hardware compatible with the principal VSI proposals.

A Glossary at the end of this report expands some less familiar acronyms.

VSI-10x. Fully Serialised Ports

Features: +5V bipolar, 17-bit PECL SERDES driving single coax, STP/SQ/twinax cable or optical fibre.

PCLK: 8, 16, 32 & 64MHz.

CLOCK: = PCLK.

Capacity: 1024Mbps (1280Mbd line rate) at 64MHz.

Chipset: HDMP-1022 (Tx) & HDMP-1024 (Rx) [1].
5V @ 2W & 2.5W typ., MQuad-80 packages.

Configuration:
16-bit Single Frame Mode, Simplex Method III with LOOPEN inverter and EQEN set (or programmable?), FLAGSEL set. 1PPS is sent as FLAG.

Pin Allocation:

Signal Name	**Port Function**	**Tx Chip**		**Rx Chip**	
		Pin ID	Pin No.	Pin ID	Pin No.
CLOCK	PCLK	STRBIN	8	STRBOUT	35
1PPS	P1PPS	FLAG	60	FLAG	45
BS[k+0]	PD[0]	D0	59	D0	71
BS[k+1]	PD[1]	D1	58	D1	70
BS[k+2]	PD[2]	D2	57	D2	69
BS[k+3]	PD[3]	D3	56	D3	68
BS[k+4]	PD[4]	D4	55	D4	67
BS[k+5]	PD[5]	D5	54	D5	66
BS[k+6]	PD[6]	D6	53	D6	65
BS[k+7]	PD[7]	D7	51	D7	60
BS[k+8]	PD[8]	D8	50	D8	59
BS[k+9]	PD[9]	D9	49	D9	58
BS[k+10]	PD[10]	D10	48	D10	57
BS[k+11]	PD[11]	D11	47	D11	56
BS[k+12]	PD[12]	D12	46	D12	55
BS[k+13]	PD[13]	D13	45	D13	54
BS[k+14]	PD[14]	D14	40	D14	51
BS[k+15]	PD[15]	D15	39	D15	50

k = 0,16,32...

Waveforms & Timing:
Port Interface: ~HCT as per chipset data sheets.
Interconnect: ~ doubly terminated PECL as per chipset data sheets.

Options: 14-bit command codes mode available to send PID, time-code etc.
Interactive link synchronisation instead of training oscillator (ie. Simplex Method I) by using the back channel to extend variant **-10b**.
Optical fibre connection possible with variant **-10b**, Cable #2.

Link: **VSI-10a**

Port: BNC jack.

Transmitter		**BNC**	**Receiver**	
Pin ID	Pin No.	Pin No.	Pin ID	Pin No.
DOUT	17	1	LIN	18

Cable: BNC plug-plug, 50Ω low loss coax.
Length to ~30m depending on quality.

VSI-10b

Port: Die cast DB-9F with pin allocations as per Copper Fibre Channel [30] and 1000BASE-CX Gigabit Ethernet [31] standards.

Transmitter			**Receiver**		
Pin ID	Pin No.	**DB-9**	**DB-9**	Pin ID	Pin No.
DOUT	17	1	5	LIN	18
+5V	--	2	2	+5V	--
FAULT	--	3	3	FAULT	--
--	--	4	4	--	--
(Rx+)	--	5	1	(Tx+)	--
DOUT*	18	6	9	LIN*	17
EWRAP	--	7	7	EWRAP	--
PGND	--	8	8	PGND	--
(Rx-)	--	9	6	(Tx-)	--

+5V, FAULT, EWRAP & GND used by MIA's.
PGND is power ground, not connected to screens.
Rx pins 17 & 18 need series 24Ω each for net 150Ω termination.

{Connectors: Molex P/N 87204, also AMP P/N ? are special high speed variants, conventional short lead metal shell types should be adequate.}

Cable: #1: Copper Link

DB-9M-M with high speed dual 150Ω STP or SQ, pairs {1,6} and {5,9} crossed over, other pins not connected. Screens are grounded on both plugs via metal back-shells.
Length to ~30m depending on quality. (Standard cable assemblies include a back channel which is not used by **VSI-10b**, but see para Options: above.)

{Stock or custom assemblies from :
AMP P/N 621771-x (x=1..4,6,9), 1-621771-x (x=0,2,3), see [9];
Amphenol Interconnect [6]; W.L. Gore [7];
Molex P/N 73030-00xx, 73045-000x (15 parts, see [8]).

DIY assembly:
2 off AMP Amplimite P/N 748046-1 [13] with 1-747579-1 ferrule;
Amphenol Skewclear P/N 160-2299-998 dual STP cable [14].}

Cable: #2: Fibre Optic Link

EL/OP MIA (or MIA Pigtail), DB-9 to dual SC connectors. Single optical fibre to 500 metres (the MIAs support full duplex operation but the back channel/fibre is not used by **VSI-10b**, but see para Options: above).

{MIA's from W.L. Gore P/Ns FCN1039 & FCN1046-L.}

VSI-10c 8-Port Interconnect, 8Gbps

Port: Mini D Ribbon 26 position shielded ribbon/leaf contact latching receptacle.

Transmitter			Receiver		
Port.Pin ID	Pin #	**MDR-26**	**MDR-26**	Port.Pin ID	Pin #
P0.DOUT*	18	1	26	P0.LIN*	17
P0.DOUT	17	14	13	P0.LIN	18
P0.GND	GND	2	25	P0.GND	GND
P1.DOUT*	18	15	12	P1.LIN*	17
P1.DOUT	17	3	24	P1.LIN	18
P1.GND	GND	16	11	P1.GND	GND
P2.DOUT*	18	4	23	P2.LIN*	17
P2.DOUT	17	17	10	P2.LIN	18
P2.GND	GND	5	22	P2.GND	GND
P3.DOUT*	18	18	9	P3.LIN*	17
P3.DOUT	17	6	21	P3.LIN	18
P3.GND	GND	19	8	P3.GND	GND
sp0	--	7	20	sp0	--
sp1	--	20	7	sp1	--
P4.GND	GND	8	19	P4.GND	GND
P4.DOUT*	18	21	6	P4.LIN*	17
P4.DOUT	17	9	18	P4.LIN	18
P5.GND	GND	22	5	P5.GND	GND
P5.DOUT*	18	10	17	P5.LIN*	17
P5.DOUT	17	23	4	P5.LIN	18
P6.GND	GND	11	16	P6.GND	GND
P6.DOUT*	18	24	3	P6.LIN*	17
P6.DOUT	17	12	15	P6.LIN	18
P7.GND	GND	25	2	P7.GND	GND
P7.DOUT*	18	13	14	P7.LIN*	17
P7.DOUT	17	26	1	P7.LIN	18

Px.GNDs are twinax screens.
sp0, sp1 are spares t.b.a., eg. HDP and V+ respectively.

{Connectors:
3M .050" MDR series P/N 10226-1210VE, -1A10VE, -55G3VC, -6212VC; N10226-52x2VC. See [10].
AMP CHAMP .050 Series II P/N 2-178238..40-4, 2-175674-4, 2-175887-4, 2-175925-4, 2-176970..72-4, 2-917334-4. (10 parts, see [12]).
Molex P/N 52311-2690 [15].

nb. The three SMT connectors P/N 10226-1210VE, -1A10VE & 52311-2690 provide easier PCB routing for the prescribed pinout.}

Cable: Eight shielded 100Ω twinax pairs plus two singles in a shielded round cable terminated by shielded MDR-26 plugs. Length to 5m (stock 3M assembly) or 10m (DIY Skewclear assembly, attenuation limited).

{Stock cable assemblies from 3M P/N 14526-EZ5B-xxx-02C, (x=050,200,300,500; x = length in cm [16].)

DIY assembly:
2 off 3M MDR P/N 10126-3000VE connector with 10326-3210-00x or 10320-A200-00 backshell [10];
Amphenol Skewclear P/N 165-2499-972, 9-pair 100Ω twinax round cable [14]. Ignore drain wire for sp0-1 pair.}

Discussion: The HDMP-1022/24 chipset succeed the 1012/14 G-Link chips well known for their use in the MkIV series correlators. With a single chip per port providing robust communication on a single coax (**VSI-10a**) they provide the simplest imaginable solution for VSI. If the port is built instead with a Copper Fibre Channel connector (**VSI-10b**) the end user can at any time opt to connect with copper (Cable #1) or optical fibre (Cable #2) simply by changing the cable. Also since standard cables contain a back channel it is possible to implement interactive synchronisation (for faster lock-up) but this is not a necessity.

At US$60 per chip [2] this is not a cheap solution for a copper only port, although the simple interconnect provides some compensation. A scan of product listings for >600 IC manufacturers [3] revealed no equivalent, compatible or even competitive packaged devices (only a 1.0-2.5Gbps ASIC Core from TI [25]). Many companies list related products for Fibre Channel, Gigabit Ethernet and SONET but these are all too specialised to be useful for VSI.

The dismal history of TAXI chip survival raises a question over committing to this single-source product. For its part HP continues to invest heavily in fibre optic technology, and 1022/24 is the third(?) generation of general purpose G-Link chipsets. The size of their market, not the number of direct competitors, may be a better predictor of the product's longevity.

VSI-11x. Partially Serialised Ports

Features: +5V or +3V HCMOS, 21-bit LVDS (q.v.) SERDES, 8mm round cable, MDR-20 (34*10mm) or DB-15 (40*13mm) connectors.

PCLK: 32 & 64MHz.

CLOCK: <= PCLK, CLOCK conveyed by PCE.

Capacity: 1024Mbps (448Mbd line rate) at 64MHz.

Chipsets: [4], [5].
5V or 3.3V, 120-300mW/chip, TSSOP-48 packages.

Transmitters				**Receivers**		
P/N	Vcc	f_pMHz	Δt_{max}	P/N	Vcc	Δt_{min}
SN65LVDS95	3.3*	31-65	0.2	SN65LVDS96	3.3	4.0/4.0
DS90CR213#	5	20-66	0.7	DS90CR214	5	2.5/4.1
DS90CR215#	3.3	20-66	0.5	DS90CR216A	3.3	2.5/2.5
DS90CR217	3.3	20-75	0.2	DS90CR218	3.3	4.1/4.1

* Tolerates 5V inputs.
# Not recommended since large Δt_{max} severely reduces link skew margin.
Δt_{max} : Worst case deviation of TPPos from nominal, = transmitter skew.
Δt_{min} : Estimated RSRC/RHRC at 64MHz (bigger = better).
All chips are TIA/EIA-644 compatible and freely interconnect.
All Tx/Rx chips have the same footprint. In the following tables pins are identified (Pin ID) according to the TI notation.

Configuration:
There are no configuration options.

Pin Allocation:

Signal Name	**Port Function**	**Transmitter**		**Receiver**	
		Pin ID	Pin #	Pin ID	Pin #
--	PCLK	CLKIN	26	CLKOUT	23
1PPS	P1PPS	D0	44	D0	24
--	PCE	D1	45	D1	26
--	sp0	D2	47	D2	27
--	sp1	D3	48	D3	29
BS[k+0]	PD[0]	D4	1	D4	30
BS[k+1]	PD[1]	D5	3	D5	31
BS[k+2]	PD[2]	D6	4	D6	33
BS[k+3]	PD[3]	D7	6	D7	34
BS[k+4]	PD[4]	D8	7	D8	35
BS[k+5]	PD[5]	D9	9	D9	37
BS[k+6]	PD[6]	D10	10	D10	39
BS[k+7]	PD[7]	D11	12	D11	40
BS[k+8]	PD[8]	D12	13	D12	41
BS[k+9]	PD[9]	D13	15	D13	43
BS[k+10]	PD[10]	D14	16	D14	45
BS[k+11]	PD[11]	D15	18	D15	46
BS[k+12]	PD[12]	D16	19	D16	47
BS[k+13]	PD[13]	D17	20	D17	1
BS[k+14]	PD[14]	D18	22	D18	2
BS[k+15]	PD[15]	D19	23	D19	4
--	32/64*	D20	25	D20	5

k = 0,16,32...
32/64* may be a static programmed bit or hard wired in some installations.
sp0, sp1: spare channels t.b.a. eg. PID, format descriptor, time code, parity (requires both channels) etc.

Waveforms & Timing:

Port Interface: ~HCT or LVTTL as per chipset data sheets.
Interconnect: Levels per TIA/EIA-644, timing as per chipset data sheets.

Options: SHTDN* (tri-state Tx output, pin 27, silence Rx, pin 22) controlled automatically by HPD signal.

Link: **VSI-11a**

Port: Mini D Ribbon 20 position shielded ribbon/leaf contact latching receptacle.

Transmitter			**Receiver**		
Pin ID	Pin #	**MDR-20**	**MDR-20**	Pin ID	Pin #
Y0M	41	1	10	A0M	8
Y0.GND	LG	11,12	19,20	A0.GND	LG
Y0P	40	2	9	A0P	9
Y1M	39	3	8	A1M	10
Y1.GND	LG	13,14	17,18	A1.GND	LG
Y1P	38	4	7	A1P	11
Y2M	35	5	6	A2M	14
Y2.GND	LG	15,16	15,16	A2.GND	LG
Y2P	34	6	5	A2P	15
CLKOUTM	33	7	4	CLKINM	16
CLKOUT.GND	LG	17,18	13,14	CLKIN.GND	LG
CLKOUTP	32	8	3	CLKINP	17
sp0	--	9	2	sp0	--
sp.GND	GND	19,20	11,12	sp.GND	GND
sp1	--	10	1	sp1	--

xx.GND are twinax screens, connect to either pin shown on the plugs, return to LVDSGND (LG) on the PCBs.
GND is logic ground.
sp0, sp1 are spares t.b.a., eg. HPD and V+ respectively.

{Connectors:
3M .050" MDR series P/N 10220-1210VE, -55G3VC, -6212VC; N10220-52x2VC. See [10].
AMP CHAMP .050 Series II P/N 2-178238..40-2, 2-175674-2, 2-175887-2, 2-175925-2, 2-176970..72-2, 2-917334-2. (10 parts, see [12]).
Molex P/N 52515-2011, 52986-2021, 52871-2011 [15].}

Cable: Five shielded 100Ω twinax pairs in a shielded round cable terminated by shielded MDR-20 plugs. Length to 10m, skew limited.

{DIY assembly:
2 off 3M MDR P/N 10120-3000VE connector with 10320-3210-00x or 10320-A200-00 backshell [10];
Amphenol Skewclear P/N 165-2499-970, 5-pair 100Ω twinax round cable [14].}

VSI-11b

Port: : DB-15 metal shell receptacle with 4-40 screwlocks.

Transmitter			**Receiver**		
Pin ID	Pin #	**DB-15**	**DB-15**	Pin ID	Pin #
Y0M	41	1	8	A0M	8
Y0.GND	LG	9	15	A0.GND	LG
Y0P	40	2	7	A0P	9
Y1M	39	3	6	A1M	10
Y1.GND	LG	11	13	A1.GND	LG
Y1P	38	4	5	A1P	11
Y2M	35	5	4	A2M	14
Y2.GND	LG	13	11	A2.GND	LG
Y2P	34	6	3	A2P	15
CLKOUTM	33	7	2	CLKINM	16
CLKOUT.GND	LG	15	9	CLKIN.GND	LG
CLKOUTP	32	8	1	CLKINP	17
sp0	--	10	14	sp0	--
sp.GND	GND	12	12	sp.GND	GND
sp1	--	14	10	sp1	--

xx.GND are twinax screens, return to LVDSGND (LG) on the PCBs.
GND is logic ground.
sp0, sp1 are spares t.b.a., eg. HPD and V+ respectively.

{Connectors:
AMP Amplimite P/N 745782-4, -6; 754820-1, -7; 745984-4;
747845-4, -6; 747837-4. (8 parts, see [17]).}

Cable: Five shielded 100Ω twinax pairs in a shielded round cable terminated by shielded DB-15 screwlock plugs. Length to 10m, skew limited.

{DIY assembly:
2 off AMP Amplimite P/N 748048-1 [18] with 1-747579-1 ferrule;
Amphenol Skewclear P/N 165-2499-970, 5-pair 100Ω twinax screened round cable [14]. If lines sp0 and sp1 are not required then the 4-pair 165-2499-969 can be substituted and pins 10, 12 & 14 left NC}

VSI-11c

Port: Mini D Ribbon 20 position shielded ribbon/leaf contact latching receptacle using the VESA DFP standard [20] format and off-the-shelf cable assemblies.

Transmitter			**Receiver**		
Pin ID	Pin #	**MDR-20**	**MDR-20**	Pin ID	Pin #
Y0M	41	11	6	A0M	8
Y0P	40	12	5	A0P	9
Y0.GND	LG	13	4	A0.GND	LG
Y1M	39	1	16	A1M	10
Y1P	38	2	15	A1P	11
Y1.GND	LG	3	14	A1.GND	LG
Y2.GND	LG	14	3	A2.GND	LG
Y2M	35	15	2	A2M	14
Y2P	34	16	1	A2P	15
CLKOUT.GND	LG	4	12	CLKIN.GND	LG
CLKOUTM	33	5	11	CLKINM	16
CLKOUTP	32	6	10	CLKINP	17
sp0	GND	7	20	sp0	GND
sp1	--	8	19	sp1	--
sp2	--	18	18	sp2	--
sp3	--	19	8	sp3	--
sp4	--	20	7	sp4	--

xx.GND are twinax screens, return to LVDSGND (LG) on the PCBs.
GND is logic ground.
sp0..sp4 are spares t.b.a., eg. GND, V+, HPD, SDA and SCL respectively, as per the DFP standard.

{Connectors:
3M .050" MDR series P/N 10220-55G3VC, -6212VC;
N10220-52x2VC. See [10].
AMP CHAMP .050 Series II P/N 2-178238..40-2, 2-175674-2,
2-175887-2, 2-175925-2, 2-176970..72-2, 2-917334-2.
(10 parts, see [12]).
Molex P/N 52515-2011, 52986-2021 [15].
nb. this pinout is incompatible with the SMT footprints.}

Cable: Four shielded 100Ω twinax pairs plus five single wires in a shielded round cable terminated by shielded MDR-20 plugs. Length to 10m.

{Stock cable assemblies from 3M P/N 14520-EZAB-xxx-0EC, (x=060, 200, 300, 500, A00; x = length in cm, A00=>10m [19].)}

VSI-11d 2-Port Interconnect, 2Gbps

Port: Mini D Ribbon 26 position shielded ribbon/leaf contact latching receptacle.

Transmitter			Receiver		
Port.Pin ID	Pin #	MDR-26	MDR-26	Pin ID	Pin #
P0.Y0M	41	1	26	P0.A0M	8
P0.Y0P	40	14	13	P0.A0P	9
P0.Y0.GND	LG	2	25	P0.A0.GND	LG
P0.Y1M	39	15	12	P0.A1M	10
P0.Y1P	38	3	24	P0.A1P	11
P0.Y1.GND	LG	16	11	P0.A1.GND	LG
P0.Y2M	35	4	23	P0.A2M	14
P0.Y2P	34	17	10	P0.A2P	15
P0.Y2.GND	LG	5	22	P0.A2.GND	LG
P0.CLKOUTM	33	18	9	P0.CLKINM	16
P0.CLKOUTP	32	6	21	P0.CLKINP	17
P0. CLKOUT.GND	LG	19	8	P0. CLKIN.GND	LG
sp0	--	7	20	sp0	--
sp1	--	20	7	sp1	--
P1.Y0.GND	LG	8	19	P1.A0.GND	LG
P1.Y0M	41	21	6	P1.A0M	8
P1.Y0P	40	9	18	P1.A0P	9
P1.Y1.GND	LG	22	5	P1.A1.GND	LG
P1.Y1M	39	10	17	P1.A1M	10
P1.Y1P	38	23	4	P1.A1P	11
P1.Y2.GND	LG	11	16	P1.A2.GND	LG
P1.Y2M	35	24	3	P1.A2M	14
P1.Y2P	34	12	15	P1.A2P	15
P1. CLKOUT.GND	LG	25	2	P1. CLKIN.GND	LG
P1.CLKOUTM	33	13	14	P1.CLKINM	16
P1.CLKOUTP	32	26	1	P1.CLKINP	17

Px.xx.GNDs are twinax screens.
sp0, sp1 are spares t.b.a., eg. HDP and V+ respectively.

{Connectors:
3M .050" MDR series P/N 10226-1210VE, -1A10VE, -55G3VC, -6212VC; N10226-52x2VC. See [10].
AMP CHAMP .050 Series II P/N 2-178238..40-4, 2-175674-4, 2-175887-4, 2-175925-4, 2-176970..72-4, 2-917334-4.

(10 parts, see [12]).
Molex P/N 52311-2690 [15].
nb. The three SMT connectors P/N 10226-1210VE, -1A10VE & 52311-2690 provide easier PCB routing for the prescribed pinout.}

Cable: Eight shielded 100Ω twinax pairs plus two singles in a shielded round cable terminated by shielded MDR-26 plugs. Length to 5m (stock 3M assembly) or 10m (DIY Skewclear assembly, attenuation limited).

{Stock cable assemblies from 3M P/N 14526-EZ5B-xxx-02C, (x=050,200,300,500; x = length in cm [16].)

DIY assembly:
2 off 3M MDR P/N 10126-3000VE connector with 10326-3210-00x or 10320-A200-00 backshell [10];
Amphenol Skewclear P/N 165-2499-972, 9-pair 100Ω twinax round cable [14]. Ignore drain wire for sp0-1 pair.}

Discussion: The LVDS Channel Link/SERDES chipsets specified in **VSI-11** reduce the size/number of connectors and cables by serialising parallel data 7:1. Since the 32 or 64MHz PCLK is transmitted directly alongside the data, synchronisation is not an issue and operation is transparent between parallel interfaces. The constant frequency PCLK also effects the transfer of a high frequency system clock across the interface, consistent with the design of most current systems. Device cost is US$10 to $15 each [2].

Serialisation from 64 to 448MHz demands the use of constant impedance circuits and low dispersion cables with ~GHz bandwidth and tight pair-to-pair skew specifications. Unfortunately the cheap and ubiquitous Category 5 patch cables are excluded on the last count. However suitable cable products from global suppliers have been identified and combined with well established connector families to provide several solutions.

VSI-11a is the most compact format with signal pin allocations to facilitate cable assembly as well as easy PCB layout for the high speed balanced transmission lines required. **VSI-11b** substitutes the MDRs with more familiar but somewhat larger D-Sub connectors. These have the advantage of a wider range of products including fully screened panel mount types suitable for internal VSI cabling and floating blind-mate module connections.

VSI-11c specifies the VESA DFP cable designed for LVDS connection of personal computers to flat panel displays, and available off-the-shelf. While its format is less convenient it may in time become very widely available,

although there are competing standards such as P&D and DVI, not to mention proprietary formats like FlatLink, FPD Link and PanelLink!
VSI-11d also exploits an existing cable format to provide a double capacity connection in the same physical space and halve the number of cables required in wideband systems.

VSI-12x. Direct Parallel Ports

Features: +5V or +3V HCMOS LVDS (q.v.) transmitters and receivers, MDR-40 (47*10mm) connectors with 33mm flat ribbon coax, or DB-50 (70*16mm) connectors with 15mm round ribbon twinax.

PCLK: <= 128MHz.

CLOCK: = PCLK.

Capacity: 1024Mbps at 64MHz , 2048Mbps at 128MHz.

Chips: [5], [23].
5V or 3.3V, ~350mW Tx, 350-600mW Rx at 128Mbps, SOIC packages.

Transmitters					**Receivers**				
P/N	nTx	Vcc	Mbps	MHz	P/N	nRx	Vcc	Mbps	MHz
DS90C31B	4	5	128	64	DS90C32B	4	5	128	64
DS90C401	2	5	128	64	DS90C402	2	5	128	64
					DS90LV18A	1	3.3	256	128
					DS90LV28A	2	3.3	256	128
DS90LV31A	4	3.3	256	128	DS90LV32A	4	3.3	256	128
DS90LV47A	4	3.3	256	128	DS90LV48A	4	3.3	256	128
SN65LVDS31	4	3.3	256	128	SN65LVDS32	4	3.3	256	128
SN65LVDS3487	4	3.3	256	128	SN65LVDS3486	4	3.3	256	128
SN65LVDS9638	2	3.3	256	128	SN65LVDS9637	2	3.3	256	128

'Mbps' is max VSI channel bit rate, 'MHz' is max VSI PCLK frequency.

Most of these devices, including all the quads, have the same pinouts as their respective RS-422 antecedents, notably the alternation of differential polarity around the chip. This curious feature is accommodated in the connector pin assignments to avoid crossovers in the PC traces.
Types DS90LV47A/48A have flow-through pinouts, yielding the cleanest layout.

Configuration:
No configuration options.

Pin Allocation:

No specification.

Options: Use HPD to enable/shut down drivers and receivers.

Link: **VSI-12a**

Port: Mini D Ribbon 40 position shielded ribbon/leaf contact latching receptacle.

Signal Name	**Port Function**	**Connector**	
		Pol-Pin	Pol-Pin
1PPS	P1PPS	M - 1	P - 21
CLOCK	PCLK	P - 2	M - 22
BS[k+0]	PD[0]	M - 3	P - 23
BS[k+1]	PD[1]	P - 4	M - 24
BS[k+2]	PD[2]	M - 5	P - 25
BS[k+3]	PD[3]	P - 6	M - 26
BS[k+4]	PD[4]	M - 7	P - 27
BS[k+5]	PD[5]	P - 8	M - 28
BS[k+6]	PD[6]	M - 9	P - 29
BS[k+7]	PD[7]	P - 10	M - 30
BS[k+8]	PD[8]	M - 11	P - 31
BS[k+9]	PD[9]	P - 12	M - 32
BS[k+10]	PD[10]	M - 13	P - 33
BS[k+11]	PD[11]	P - 14	M - 34
BS[k+12]	PD[12]	M - 15	P - 35
BS[k+13]	PD[13]	P - 16	M - 36
BS[k+14]	PD[14]	M - 17	P - 37
BS[k+15]	PD[15]	P - 18	M - 38
--	sp0	M - 19	P - 39
--	sp1	20	--
--	sp2	--	40

k = 0, 16, 32...

Circuit ground connection is provided by the ribbon coax outer conductor.
Differential signal Pol(arity)-, M(inus)-, P(lus)-.
sp0, sp1 & sp2 are spares t.b.a., eg. PID, HPD and V+ respectively.

{Connectors:
3M .050" MDR series P/N 10240-1210VE, -55G3VC, -6212VC;
N10240-52x2VC. See [10].}

Cable: Forty conductor "Pleated Foil" (ribbon coax) external flat cable with metal back-shell plugs. Length to ~15m at 128MHz or ~20m at 64MHz, attenuation limited.

{Stock cable assemblies from 3M, P/N MS-90101x-040-NL-xxx.xN, (xxx.x = length in inches [24][26].)}

VSI-12b

Port: Metal shell DB-50F with 4-40 screwlocks.

Signal Name	**Port Function**	**Connector**			**IDC**
		Pol-Pin	Pol-Pin	GND	Pair
1PPS	P1PPS	M - 34	P - 1	35	2,1
CLOCK	PCLK	P - 18	M - 2	19	3,4
BS[k+0]	PD[0]	M - 36	P - 3	19	8,7
BS[k+1]	PD[1]	P - 20	M - 4	37	9,10
BS[k+2]	PD[2]	M - 38	P - 5	21	14,13
BS[k+3]	PD[3]	P - 22	M - 6	39	15,16
BS[k+4]	PD[4]	M - 40	P - 7	23	20,19
BS[k+5]	PD[5]	P - 24	M - 8	41	21,22
BS[k+6]	PD[6]	M - 42	P - 9	25	26,25
BS[k+7]	PD[7]	P - 26	M - 10	43	27,28
BS[k+8]	PD[8]	M - 44	P - 11	27	32,31
BS[k+9]	PD[9]	P - 28	M - 12	45	33,34
BS[k+10]	PD[10]	M - 46	P - 13	29	38,37
BS[k+11]	PD[11]	P - 30	M - 14	29	39,40
BS[k+12]	PD[12]	M - 48	P - 15	47	44,43
BS[k+13]	PD[13]	P - 32	M - 16	31	45,46
BS[k+14]	PD[14]	M - 50	P - 17	31	50,49
BS[k+15]	PD[15]	P - 49	M - 33	47	47,48

k = 0, 16, 32...

Differential signal Pol(arity)-, M(inus)-, P(lus)-.
GND pins return twinax drain wires in VSI cable. Some GND pins return two such wires.
IDC pairs not listed are all [GND,GND].

{Connectors:
AMP Amplimite P/N 747193-2 [17].}

Cable: #1: Minimum Loss, 24awg conductors.
Eighteen shielded 100Ω twinax pairs in a 15mm shielded round cable terminated by shielded DB-50 plugs. Length to ~30m at 128MHz or ~45m at 64MHz, attenuation limited.

{ DIY assembly:
2 off AMP Amplimite P/N 749760-1 [18] with 747580-6 ferrule;
Amphenol Skewclear P/N 165-2499-975, 20-pair 100Ω 24awg twinax jacketed round cable [14]. Ignore last two pairs.}

Cable: #2: Maximum Flexibility, 30awg conductors.
As for Cable #1 but substitute Skewclear P/N 165-3099-944 and ferrules 747580-8 for 10mm cable diameter.
Length to ~15m at 128MHz or ~20m at 64MHz, attenuation limited.

26 and 28awg cable is also available to give intermediate tradeoffs between length and attenuation.

Discussion: Simply converting from CMOS to LVDS to traverse the interconnect provides a VSI of minimum complexity which makes the most of available cable performance. The cost, compared with SERDES alternatives above, is a considerable increase in physical size of the interface hardware. Even so the PCB area required is about one third of an equivalent ECL interface and the power dissipation about one fifth. The cable types listed have much greater bandwidth than traditional PVC dielectric flat ribbons, and their screening provides much lower levels of cross-talk, RFI and susceptibility to EMI.

VSI-12a uses an atypically low loss .025" ribbon coax to provide practical length cables in a relatively compact format. Cable assemblies are made-to-order catalogue items. The component parts are also available but terminating the cable in the connectors may be difficult.

VSI-12b supports self assembly and the possibility of very long cable runs but at the cost of a rather large connector. The pin allocation is designed to facilitate cable termination and a clean PCB layout, while maintaining natural pairing in ribbon cables. This permits convenient assemblies of IDC connectors with twist-and-flat ribbon for internal use, test cables etc.

VSI-13. CORRCLOCK Port

The LVDS interface chips from **VSI-12** and the small format cable assemblies in **VSI-11a** and **11b** combine to provide a modern alternative to the high

energy drivers, transients and ground currents associated with TTL signals driven on 50Ω coaxes.

Spare pairs in the cable may be used to provide full duplex serial communications between CORR and DOB, ie. the Control function.

CORRCLOCK Ports based on **VSI-11b** and **VSI-11a**:

Correlator		**DOB**	**Corr**	**DOB**
Signal	**DB-15**	**DB-15**	**MDR-20**	**MDR-20**
RxP	1	8	1	10
Rx.GND	9	15	11,12	19,20
RxM	2	7	2	9
TxM	3	6	3	8
Tx.GND	11	13	13,14	17,18
TxP	4	5	4	7
CORRTICKP	5	4	5	6
CORRTICK.GND	13	11	15,16	15,16
CORRTICKM	6	3	6	5
CORRCLOCKM	7	2	7	4
CORRCLOCK.GND	15	9	17,18	13,14
CORRCLOCKP	8	1	8	3
sp0	10	14	9	2
sp.GND	12	12	19,20	11,12
sp1	14	10	10	1

Rx, Tx; serial comms lines. Either RS-422 (eg. use SN75179B) or LVDS (eg. use SN65LVDS179) format.
sp0, sp1 are spares t.b.a., eg. HPD and V+ respectively.

Internal Module Ports and Cables

The port connector which terminates an external VSI cable will not always terminate the signal path. For example in a highly modular constructions such as a DAS, signals may be conveyed from an external connector on the back of the bin/crate to an internal backplane, with blind-mate connectors to the module. The internal cable assembly must continue the external cable structure in order to maintain signal integrity. It is generally desirable that the internal/module connector format matches the external port, so the internal cable is wired straight-through from female to male connectors. Backplane connectors usually float to facilitate the mating process.

No suitable internal connector-cable combinations have been identified for the MDR series connectors, from the sources referenced in the proposals. The flange-mounted D-Sub series is well supported with a wide selection and representative parts are listed by

proposal below. nb. Only solid/machined pin plugs should be used in the backplane. Cable P/Ns as per the external cable assemblies except as noted.

IntVSI-10a

The BNC-coax proposal is served by divers sources, with the additional option of converting to semi-rigid and OSP connectors for a more compact internal assembly.

IntVSI-10b

{ Non-screwlock types for internal use: 745781-2; 747844-2; 745183-1, -3, -7; 748038-1 & 748047-1 (discard outer) [17].}

IntVSI-11b

{ Non-screwlock types for internal use: 745782-2; 747845-2; 745185-1, -5, -7; 748040-1 & 748041-1 [17].}

IntVSI-12b

{ Non-screwlock types for internal use: 745116-2; 747577-1 & 747578-1; or use 746789-1 & 646790-1 [17] with Amphenol TwistNFlat P/N 132-2801-050 28].}

Appendix

PID

Port IDentifier, a 16-bit binary number permanently allocated to each transmitting port and automatically transmitted across the Interface to the receiving port. Allows the destination equipment or its control software to verify the actual source of data arriving on each cable. If PIDs are unique globally, and DTS's record incoming PIDs along with other auxiliary data, a form of automatic identification is provided. Further, if each DOB appends the previous PID(s) to its own, a complete "path" for the data will build up through sundry network DTS's, tape copiers etc. This process would require each DTS to provide space for, say, four PIDs.

V+

A +5V auxiliary power rail provided by the source (Tx) port. eg. 5V+/-5%, 50mA min, 500mA max. Variously signals to destination that source is connected and active; supports a floating destination port converting from VSI back to bit streams as part of a converter to non-VSI formats; provides power to destination "EDID" logic so SDA/SDL (q.v.) can function even if the destination host is powered down.

HPD

Hot Plug Detect. Provides feedback from destination to source port if V+ is received and destination is active. Signals hosts that VSI is ready to go, may be used to enable interface hardware in both ports.

SDA, SDL
Serial DAta, Serial CLock. I^2C type signals [29] providing the source with destination detection, identification and configuration, after the manner of VESA's DDC and EDID standards [20]. See also V+ above.

Glossary

DIY Do It Yourself!

EL/OP ELectrical to OPtical (fibre)

LVDS Low Voltage Differential Signalling
LVDS is a high speed, low power, low RFI differential signal technology with major applications in back-plane extension, serial transmission and chip-chip links at >100MHz between CMOS ASICS. It is principally supported by TI [21] and Nat Semi [22] who have established substantial suites of devices [23] [5]. Hardware is typically HCMOS. Signals are ~4ma switched differentially into a balanced transmission line terminated by floating 100Ω resistor.
In comparison with traditional ECL (or PECL) interfaces, LVDS costs considerably less power, PCB real estate and $, generates less RFI and does not require a negative power supply.

MIA Media Interface Adaptor
A Fibre Channel [30] component, converting between electrical and optical formats.

SERDES SERialiser DESerialiser

SQ Shielded Quad cable

STP Shielded Twisted Pair cable

twinax
Contrasts with STP in that it is a wide bandwidth cable with parallel, not twisted, inner conductors.

References

[0] http://dopey.haystack.edu:80/vsi/ {VLBI Standard Interface: 3-Feb-99}
[1] http://www.hp.com/HP-COMP/io/hdmp1022.html
[2] http://www.em.avnet.com/cgi-bin/sc.cgi
[3] http://www.scruz.net/~gcreager/
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