A 2GHz Digital Filterbank Correlator

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Abstract

The combination of traditional polyphase filter architecture with a new multiplier-rich FPGA family provides the means to build wideband (GHz), flexible and high dynamic range filterbanks and FX correlators using a small number of commodity ICs. A 2GHz 4k-channel unit, serving as a prototype for next generation ATNF correlators and as an SKA demonstrator, is described.

Polyphase Digital Filterbanks

Whereas the 'F' in 'XF correlator' necessarily represents a Fourier transform, the 'F' in 'FX correlator' indicates a *filterbank* of which the ubiquitous FFT is but one, rather crude, example.

Conventional uniform filterbanks comprise an array of quadrature downconverters. For each one the LO frequency defines the centre of the passband, and identical lowpass filters in the I and Q outputs define its shape. Such structures are at the heart of familiar VLBI systems such as the analog VCs and BBCs in MkIV and VLBA DARs respectively, and the digital IFPs in the LBA DAS.

Direct implementation of large arrays of order 10^3 channels is expensive in any technology. Fortunately digital converters using FIR output filters can be described with simple algebra, thus providing an alternative form of 'circuit design'. Comparison of the set of expressions for a filterbank reveals many common, ie redundant, operations. With a judicious choice of parameters the whole can be factorised and rearranged as a single instantiation of the FIR filter in polyphase form, and a matrix of complex modulators $e^{-j\omega_k t}$ in the form of a DFT. The DFT is naturally evaluated as an FFT.

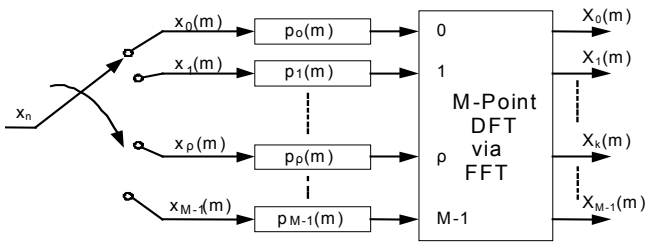

Figure 1 *M-Channel Filterbank in Polyphase Form*

Figure 1 shows the resulting structure. Taps of the original FIR filter are distributed amongst the short (length ~16) FIR sections p_ρ. All computation is at the output channel rate. Compared with direct implementation, the hardware clock rate is reduced by a factor of 2M and the number of filter evaluations is also reduced by 2M. Modulations are reduced by a factor of ~$M/\log_2 M$ thanks to the FFT. With M of order 10^3 these represent considerable savings in cost and complexity.

Arbitrary Passbands >> High Performance

The channel shape may be designed with standard filter tools to have a rectangular passband with steep transitions to deep stopbands, in contrast to the compromise of channel smearing and leakage which besets the simple FFT solution. Non-overlapped bands also permit simultaneous high resolution analysis *within* individual channels by small external processors, and high band efficiency offers maximum SNR in the integrated visibilities.

New Technology >> Reconfigurable Designs, High Dynamic Range

The recently released Xilinx Vertex II FPGAs are replete with 18*18 multipliers and 36-bit RAM blocks, ideal for FIR filter structures, FFTs and integrating correlators. For example at 128MHz the XC2V6000 can support a 16k-tap polyphase filter for a 1GHz wide 1k-channel filterbank. That such a structure can be built inside a single IC represents a massive reduction in size and construction costs.

An additional bonus is the ability to reconfigure the hardware as required to produce instruments with quite different characteristics. Sufficient I/O pins and internal resources are available to support data from high resolution ADCs, and provide a dynamic range of ~16 bits at the FFT output. These will be important factors in providing a system robust against strong interferers in both the local and SKA environments, and may also mean that IF/sampler gain servos are no longer required.

Free Interpolation ≫ Fractional Sample Delay

The combination of a digital filter with a technology capable of storing many sets of coefficients provides an easy method of inter-sample interpolation. Thus 'fractional sample delay' for delay tracking amounts to selecting the appropriate coefficient set, and is effectively a 'free' feature of the polyphase filter.

This feature also facilitates conversion of the input data from real to complex form. Interpolation of the imaginary part is additional to delay tracking, and other details are absorbed into the existing filter structure. The advantage gained is a doubling of the number of frequency channels for a given length of FFT.

Zoom Features ≫ Even Higher Resolution

When the outputs of the polyphase filter are summed directly the structure becomes a classic integer-band decimating filter. (This is exactly the bottom channel of the DFT.) Transforming the coefficients in the usual way to shift the band centre up from DC, gives a bandpass channel of the original shape, but centred at what was a band edge in the original scheme.

The total filter computation is independent of the decimation factor M, but the reduced bandwidth passed to the FFT hardware means its load is reduced to 1/Mth. It may now take on both polyphase and FFT roles to produce the same number of, or even more, channels across the reduced bandwidth. This bandwidth in turn can be varied with M. The reprogrammable FPGAs allow such reconfigurations at will.

2GHz 4k-Channel Correlator Project

The ATNF is developing an FX correlator based on a 2GHz wide 4096 channel filterbank with rectangular passbands and 50dB adjacent channel rejection. Input data up to 8-bit resolution is supported, delay tracking to T/16 is provided by interpolation, and SSB fringe stopping follows channelisation. Zoom factors of 8 and 64 are being considered. The ATNF's new 2-bit 4Gsps InP sampler will provide the wideband input. High dynamic range experiments will initially use 8-bit 128Msps LBA DAS data.

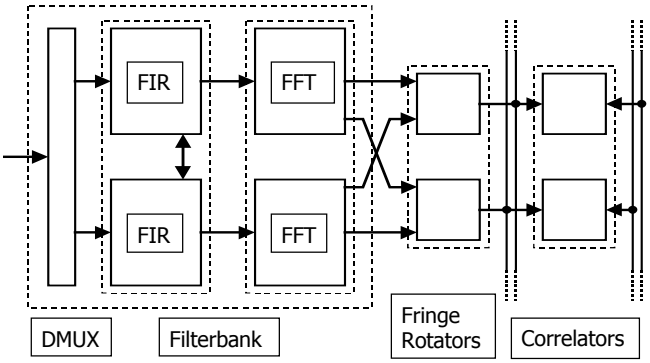

Figure 2 *Basic Filterbank Correlator Structure*

The structure shown above supports the 4k-channel complex input mode, the 2k-channel real input mode, and the zoom modes at a bandwidth of 2GHz. The data DMUX functions are absorbed into the wideband data bus while the rest of the system fits into a small number of FPGAs as indicated. The polyphase FIR and the FFT parts each use two large XC2V6000 ICs, while the fringe rotator and (per baseline) correlator parts each use two of the smaller XC2V1000 ICs. All chips are clocked at 128MHz.

The wide-input multipliers allow artefact-free fringe stopping in the rotator and high tolerance to noncoherent interference signals in the correlator, limited only by the maximum number of bits retained in the data streams before distribution to the correlator block. More resources are available in the FPGAs to provide scaling and requantisation if necessary.

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