MULTIBEAM CORRELATOR MODULE

ATNF Electronics Group

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Contents

1.0 General Description.

The Correlator Module provides a 1024 lag autocorrelator for the Multibeam project for the Australia Telescope National Facility Parkes Radio Telescope. It is designed to be a complete host for the ATNF Sampler also designed for the same project. The correlator uses the recently developed University of New Mexico Arecibo NASA SERC correlator chip.

Provision has been made for the installation of a second correlator IC. With this second correlator IC installed, an autocorrelation function of 2048 lags can be obtained, or with the connection of a second sampler to the Auxiliary Sampler Input, a crosscorrelation function of +/- 1024 lags may be generated.

The sampler signal is transmitted to the correlator over 2 X twisted pair cable at 128MHz using balanced ECL. One twisted pair is Magnitude and the other is Sign. Conversion from the sampler's 4 level mode to the 3 levels required by the correlator chip is done in the Correlator

Module by the Data Generator FPGA. The basic conversion algorithm is shown below. A variety of conversion algorithms may be programmed if required.

Sampler		**Correlator**	
Output	Value	Input	Value
01	+4	01	2
00	+1	00	1
10	-1	00	1
11	-4	10	0

An auxillary data input port exists to allow data from other external sources to be input to the correlator.

Configuration and monitoring of the sampler is done via a standard ATNF Dataset interface while dynamic or realtime control is via 2 X twisted pair balanced TTL signals. All these control signals are provided by the Correlator Module, but if required may be sourced elsewhere.

Configuration of the Correlator Module is done via a standard ATNF Block Control Computer Interface Bus, and dynamic or realtime control via an ATNF Event Generator Bus.
The ATNF Block Control Computer Interface Bus is a 15 bit address, 16 bit data read/write bus that allows configuration and status data to be transferred between the Correlator Module and an IBM PC based control computer using a standard ATNF BCC Interface card.
The ATNF Event Generator bus is a 16 bit data, 1 bit strobe unidirectional balanced TTL bus that allows precisely timed signals to be delivered to a remote point. These signals can come from any appropriate source or from an IBM PC or DEC Q-BUS ATNF Event Generator. The use of an ATNF Event Generator requires a time-frame generator such as the ATNF Time-frame Clock.

Data output is via a 32 bit wide data/address bus plus 8 control control signals (4 in and 4 out). The "standard" protocol on this bus is that used by the existing ATNF Correlator DMA bus which is connected to a DEC Alpha workstation. This is an asynchronous protocol that uses 2 outward control signals (REQuest and NEXT) and one return signal (ACKnowledge). Other protocols can programmed if required.
Data may also be retrieved via the BCC Interface Bus but at a considerably reduced rate. The use of the BCC Interface Bus to transfer data means that it is possible to collect and process data using an IBM PC.

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2.0 Memory Maps.

2.1 Global Memory Map.

Each Correlator board occupies a 64 byte (32 word (16 bit word)) segment on the Block Control Computer Interface Bus. The base address of each board is assigned by the position it occupies in the bin as well as the bin identity, assigned as per the 8 pole DIP switch located thereon. Only the first 7 switches have any meaning, translating to the top 7 BCC Interface address lines, and the next 3 address bits from the board position.

BCCAddr Line	Match Source	BCC IF value	DMA IF value
---	Block ID #7	-----	0x800000
A15	Block ID #6	0x4000	0x400000
A14	Block ID #5	0x2000	0x200000
A13	Block ID #4	0x1000	0x100000
A12	Block ID #3	0x0800	0x080000
A11	Block ID #2	0x0400	0x040000
A10	Block ID #1	0x0200	0x020000
A9	Block ID #0	0x0100	0x010000
A8	Unit ID #2	0x0080	0x008000
A7	Unit ID #1	0x0040	0x004000
A6	Unit ID #0	0x0020	0x002000

There are 24 X 16 bit non contiguous registers in the Multi Beam Correlator. The following section shows their mapping reference to the boards base address.

2.2 Register Memory Map.
The following is a list of the various registers on each Correlator Module.

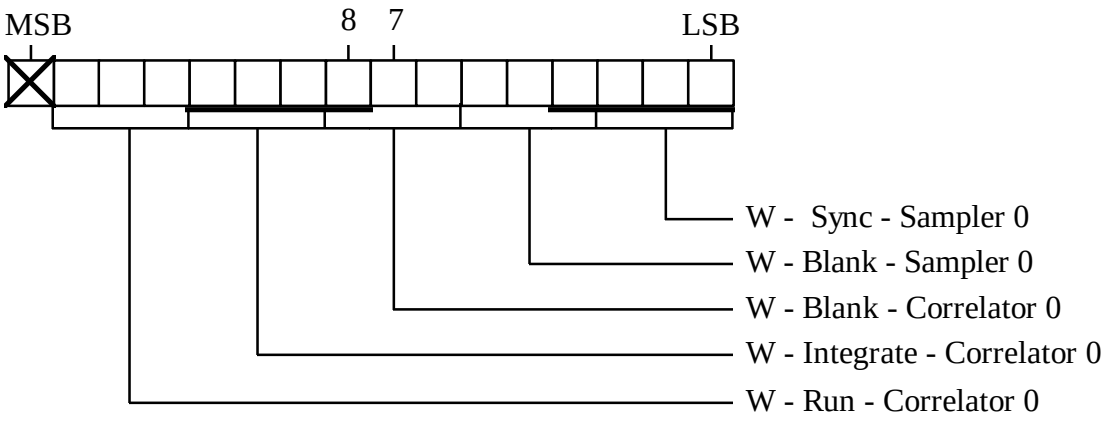
Address	Description
Base	Select EG lines correlator #1 (Write).
Base + 0x1	Select EG lines correlator #2 (Write).
Base + 0x2	Select EG lines and control correlator #1 (Write).
Base + 0x3	Select EG lines and control correlator #2 (Write).
Base + 0x4	DMA EG signal select, DataSet address offset, serial number and remote programming of DMA controller Xilinx. (Read/Write).
Base + 0x5	Reserved
Base + 0x6	Reserved
Base + 0x7	Reserved
Base + 0x8	DMA Controller (Read). LS word correlator
Base + 0x9	DMA Controller (Read). MS word correlator
Base + 0xA	DMA Controller (Read/Write). Control/status register
Base + 0xB	DMA Controller (Read). DMA address value
Base + 0xC	Clock Generator/Data Generator (Read/Write).
Base + 0xD	Clock Generator/Data Generator (Read/Write).
Base + 0xE	Clock Generator/Data Generator (Read/Write).
Base + 0xF	Clock Generator/Data Generator (Read/Write).
Base + 0x10	DataSet 0 Register 0 (Read/Write).
Base + 0x11	DataSet 0 Register 1 (Read/Write).
Base + 0x12	DataSet 0 Register 2 (Read/Write).
Base + 0x13	DataSet 0 Register 3 (Read/Write).
Base + 0x14	DataSet 1 Register 0 (Read/Write).
Base + 0x15	DataSet 1 Register 1 (Read/Write).
Base + 0x16	DataSet 1 Register 2 (Read/Write).
Base + 0x17	DataSet 1 Register 3 (Read/Write).
Base + 0x18	Reserved.
	.....
Base + 0x1F	Reserved.

The Clock Generator/Data Generator registers are divided such that the top eight bits belong to the Clock Generator and the bottom eight bits belong to the Data Generator.
The DataSet registers are mapped in groups of 8 contiguous locations. The DataSet auxillary bus has 6 address lines that (in conjunction with the HI/LO byte signal) gives an address range of 64 (16 bit) locations. The Samplers associated with each Correlator Module (each Sampler appears as 4 locations on this bus) should be set up to appear within this window. The wondow can be set to access any of the 8 other sets of address by setting the DataSet Address Offset bits in the Multibeam Correlator Register 4

3.0 Register descriptions.
This section describes the registers found on the Correlator Module. Those registers defined above as 'DataSet' are not described here as they are dependent on what is connected to the Correlator Module's emulation of a DataSet auxillary bus at that time.

3.1 Multibeam Correlator Register 0.

MULTIBEAM CORRELATOR REGISTER 0 (Offset 0x0)

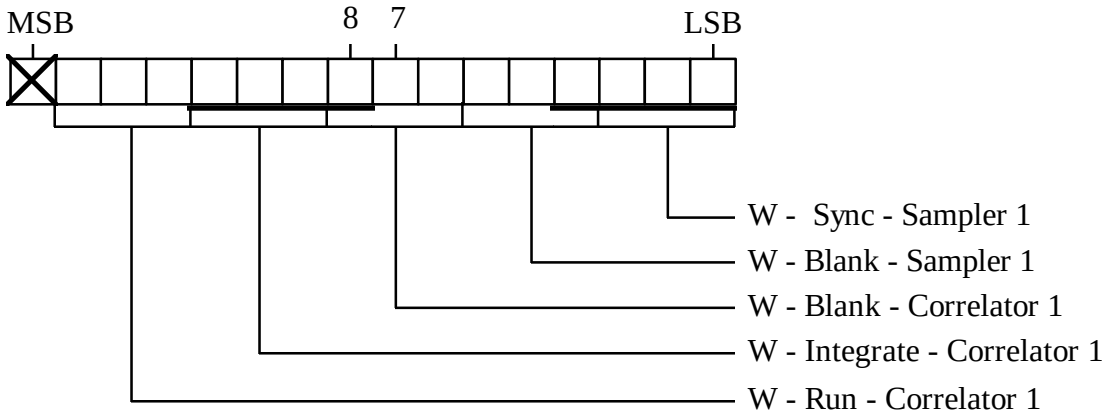


Multibeam Correlator Register 0. (offset 0x0)

Sync Sampler 0.	3 bits select the source for the Sampler Sync signal for Sampler 0 from the 8 available.
Blank Sampler 0.	3 bits select the source for the Sampler Blank signal for Sampler 0 from the 8 available.
Blank Correlator 0.	3 bits select the source for the Blank signal for Correlator 0 from the 8 available.
Integrate Correlator 0.	3 bits select the source for the Integrate signal for Correlator 0 from the 8 available.
Run Correlator 0.	3 bits select the source for the Run signal for Correlator 0 from the 8 available.

3.2 Multibeam Correlator Register 1.

MULTIBEAM CORRELATOR REGISTER 1 (Offset 0x1)

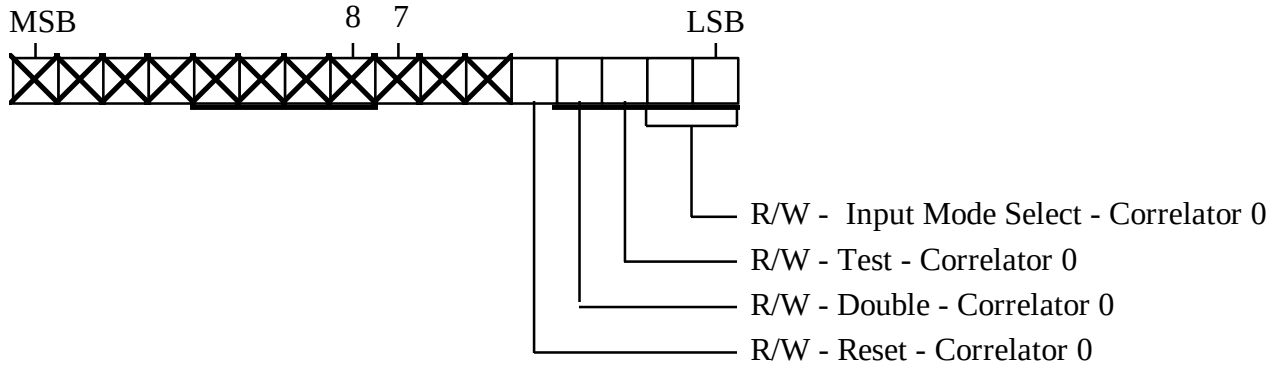


Multibeam Correlator Register 1. (offset 0x1)

Sync Sampler 1.	3 bits select the source for the Sampler Sync signal for Sampler 1 from the 8 available.
Blank Sampler 1.	3 bits select the source for the Sampler Blank signal for Sampler 1 from the 8 available.
Blank Correlator 1.	3 bits select the source for the Blank signal for Correlator 1 from the 8 available.
Integrate Correlator 1.	3 bits select the source for the Integrate signal for Correlator 1 from the 8 available.
Run Correlator 1.	3 bits select the source for the Run signal for Correlator 1 from the 8 available.

3.3 Multibeam Correlator Register 2.

MULTIBEAM CORRELATOR REGISTER 2 (Offset 0x2)

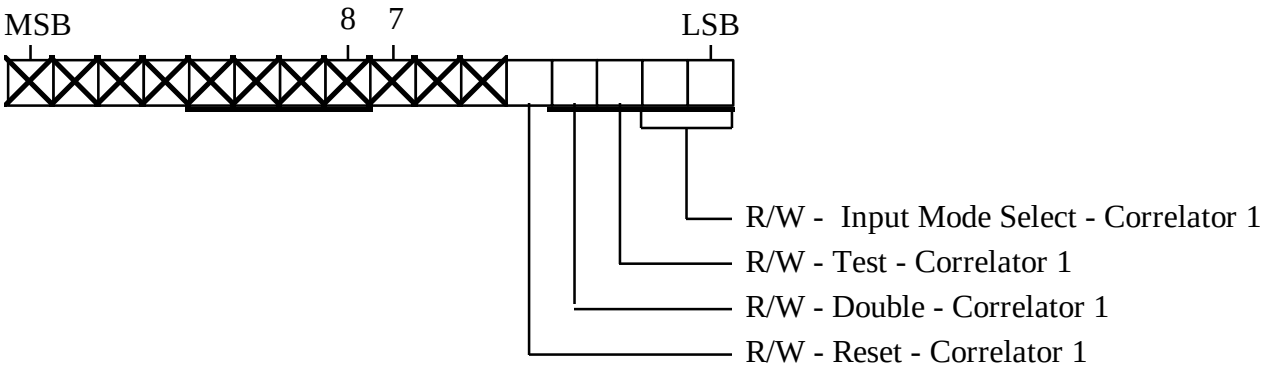


Multibeam Correlator Register 2. (offset 0x2)

Input Mode Select.	2 bits select the input mode for correlator 0. These two bits should always be zero for Correlator 0.
Test.	Writing a 1 to this bit sets Correlator 0 into internal test mode.
Double.	Writing a 1 to this bit sets Correlator 0 into double sampling rate mode.
Reset.	Writing a 1 to this bit forces a reset of correlator 0 accumulator. This signal must remain hi for at least the correlator clock period.

3.4 Multibeam Correlator Register 3.

MULTIBEAM CORRELATOR REGISTER 3 (Offset 0x3)

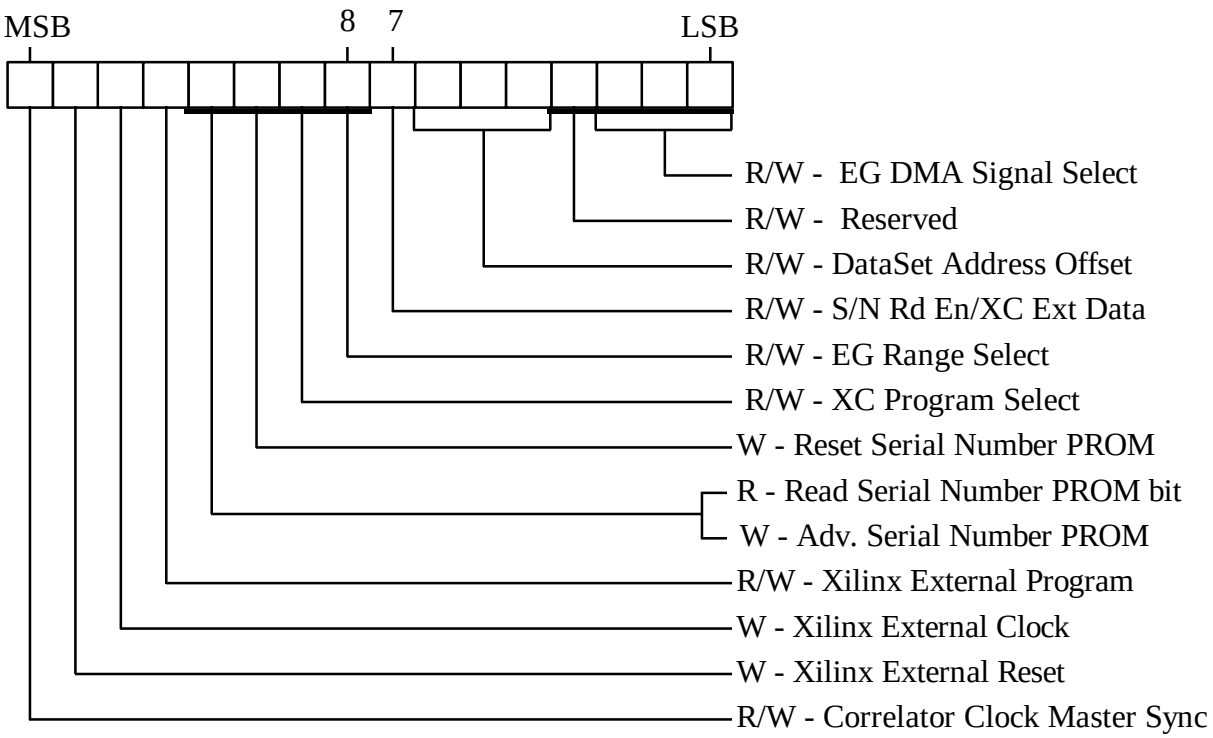


Multibeam Correlator Register 3. (offset 0x3)

Input Mode Select.	2 bits select the input mode for correlator 1. Bit 0 selects input source for X channel. Bit 1 selects input source for Y channel. A 0 selects the data source from the Data Generation Xilinx. A 1 selects the data source from the cascade output of Correlator 0. Setting both bits to 1 enables on board concatenation of Correlator 0 and Correlator 1.
Test.	Writing a 1 to this bit sets Correlator 1 into internal test mode.
Double.	Writing a 1 to this bit sets Correlator 1 into double sampling rate mode.
Reset.	Writing a 1 to this bit forces a reset of correlator 1 accumulator. This signal must remain hi for at least the correlator clock period.

3.5 Multibeam Correlator Register 4.

MULTIBEAM CORRELATOR REGISTER 4 (Offset 0x4)



Multibeam Correlator Register 4. (offset 0x4)

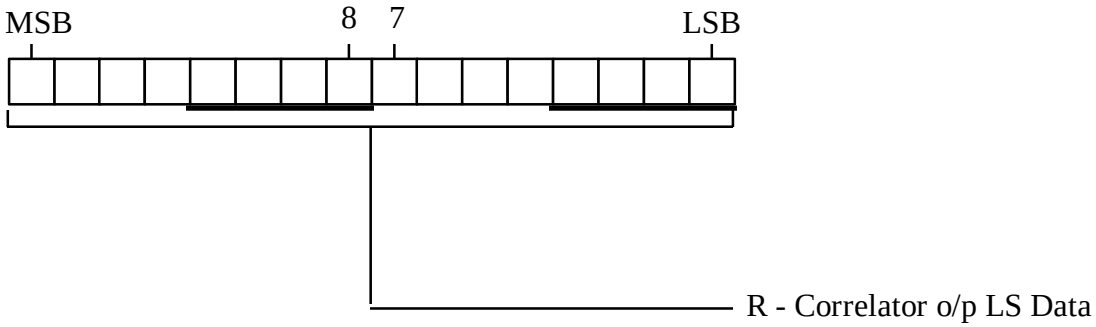
EG DMA Signal Select.	3 bits select the which of the eight Event Generator lines (set by the EG Range bit) will signal the DMA controller.
Reserved.	Reserved for future expansion from 3 to 4 bits for EG DMA Signal Select.
DataSet Address Offset	3 bits determine the 3 MSbits of the posted address on the DataSet address bus. This allows the BCC to directly access 8 contiguous DataSet addresses. See section 2.2.
S/N Rd En/XC Ext Data.	This is a dual function bit. When set the serial number can be read. The serial number reading operation uses the DataSet address lines to control the external serial number PROM, hence this bit must be reset before the DataSets bus can be used. To program the selected Xilinx chip, a data bit is written to this bit, then the Xilinx External Clock bit in this register must be written to. To be able to programme Xilinx chips through this register, it is necassary to set up the PCB jumpers accordingly.
EG Range Select.	When Lo the lower 8 bits of the event generator bus are used for Event Generator signals. When Hi the top 8 bits are used.
XC Program Select.	When Lo, the programming bits are set to connect to Xilinx chip #2 (DMA interface controller, and when set hi the programming bits are connected to Xinlinx chip #4 (Input Sampler data controller).
Reset Serial Number PROM.	Writing a 1 to this location resets the serial number PROM. This must be done before the Serial Number can be read. As the serial Number PROM uses some of the DataSet address bus lines, no Dataset activity must take place on this bus until the serial number reading has been completed. The Serial Number Read Enable bit must also be set.

Advance Serial Number Prom.	Writing a 1 to this bit will cause the next bit in the Serial Number serial PROM to be made available. This must be done before each new bit of the Serial Number can be read. When read, this bit is the current state of the Serial Prom Data bit. As the serial Number PROM uses some of the DataSet address bus lines, no Dataset activity must take place on this bus until the serial number reading has been completed. The Serial Number Read Enable bit must be set to perform any operations with the Serial Number PROM.
Xilinx External Program.	Writing a 1 to this bit pulses the DONE/PROG line on the DMA Xilinx chip to go Lo forcing that chip to enter the configuration state. The state of the DONE/PROG bit may be read by reading this bit. The destination of this bit is controlled by the XC Program Select bit above. To be able to programme Xilinx chips through this register, it is necassary to set up the PCB jumpers accordingly.
Xilinx External Clock	Writing a 1 to this bit sends a clock pulse to the selected Xilinx chip. The rising edge clocks the state of the S/N Rd En/XC Ext Data bit into the selected Xilinx chip. The destination of this bit is controlled by the XC Program Select bit above. To be able to programme Xilinx chips through this register, it is necassary to set up the PCB jumpers accordingly.
Xilinx External Clock	Writing a 1 to this bit sends a reset pulse to the selected Xilinx chip. The destination of this bit is controlled by the XC Program Select bit above. To be able to programme Xilinx chips through this register, it is necassary to set up the PCB jumpers accordingly.
Correlator Clock Master Sync	Setting this bit Hi enables this Correlator Module to be Master. This means that this Correlator Module sends its synchronizing signal out onto the Clock Sync Bus. When set Lo this Correlator Module is Slave. There can be only one Master. There is no interlocking of the Master Sync signal, so care should be taken to be sure only one Correlator Module is master. (Note: as the Clock Sync bus uses PECL, it is unlikely to cause any damage if more than one Correlator Module is set to be Master.)

To program a Xilinx chip through this register, perform the following operation.
1. Select the desired xilinx chip to program by setting the XC Program Select bit.
2. Force the Xilinx chip into the programme state by writting a 1 to the Xilinx External Program bit. Read this bit back to see if it went low. If not it may be necassary to force a full reset by writing a 1 to both Xilinx External Program bit and the Xilinx External Reset bit together.
3. Once the Xilinx External Program bit has gone Low, transfer the programming data one bit at a time by first writing that bit to the S/N Rd En/XC Ext Data, then as a seperate operation writing a 1 to the Xilinx External Clock bit. Repeat this operation until all bits are sent.
4. After all bits have been sent, read the Xilinx External Program bit to see if the Done/Program line has gone Hi. If not, the Xilinx chip has not programmed correctly. Repeat from point 2 if necassary.

3.6 Multibeam Correlator Output Register 1.

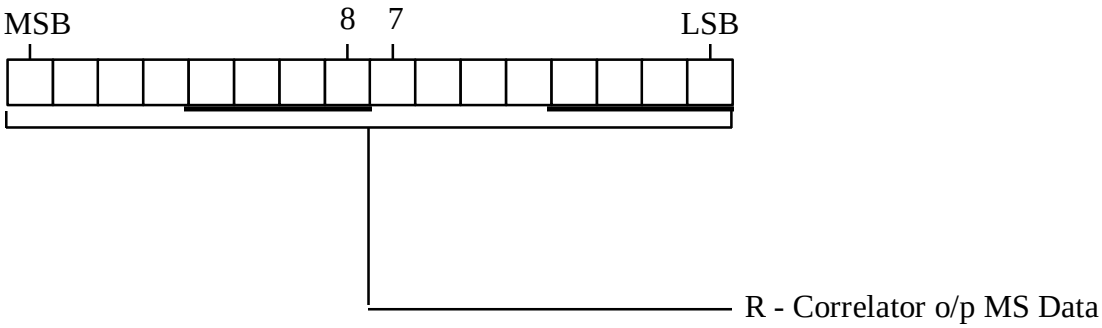
CORRELATOR OUTPUT LS DATA REGISTER 1 (Offset 0x8)



Correlator o/p LS Data	The LS 16 bits of the 32 bit output of the Correlator IC. When reading the Correlator IC this register must be read first, then the Correlator Output MS Data Register 2.

3.7 Multibeam Correlator Output Register 2.

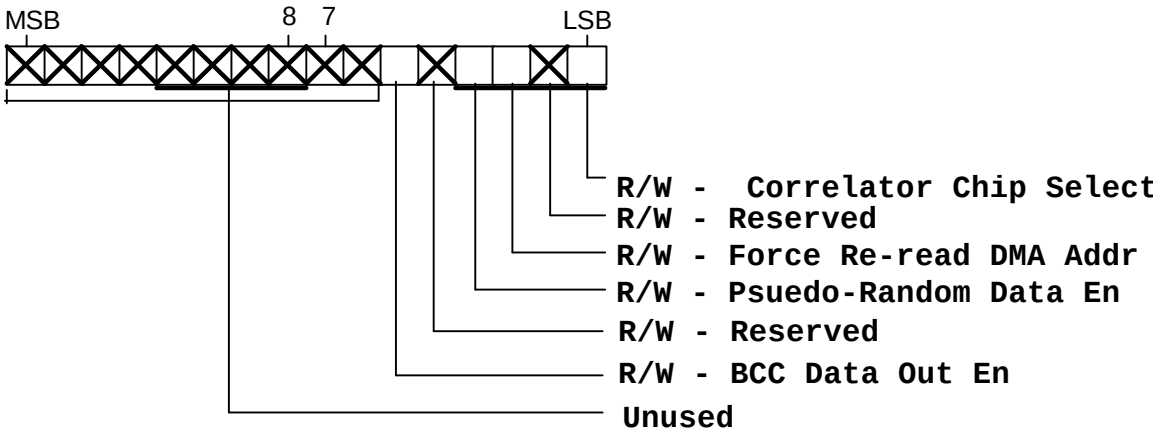
CORRELATOR OUTPUT MS DATA REGISTER 2 (Offset 0x9)



Correlator o/p MS Data	The MS 16 bits of the 32 bit output of the Correlator IC. When reading the Correlator IC this register must be read last, directly after the Correlator Output MS Data Register 1.

3.8 Multibeam Correlator Output Register 3.

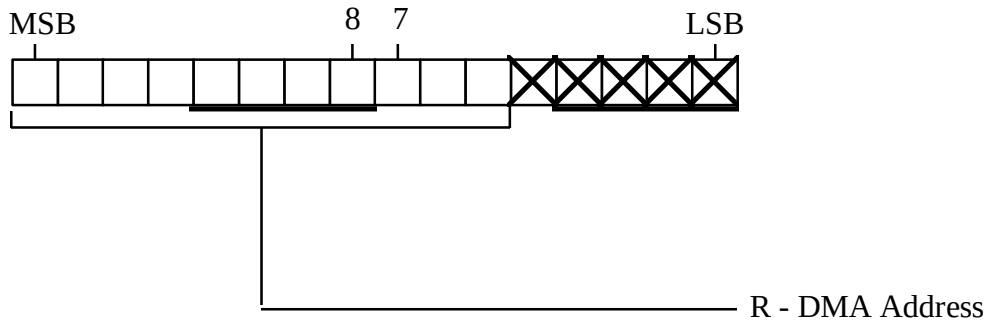
CORRELATOR OUTPUT CONTROL REGISTER (Offset 0xA)



Correlator Chip Select	Selects which correlator chip will be read when the BCC accesses Correlator Output registers 1 and 2. When set to 0 correlator chip 0 will be read and when set to 1 correlator chip 1 will be read.
Force Re-read DMA Address	Writing a 1 to this bit reloads the address of the DMA interface. The address is only loaded at power up or whenever this bit is set to 1. This operation should not be performed while a DMA transfer is in progress. When read, this bit has no meaning.
Psuedo-Random Data Enable	When set to 0 the data read out by either the DMA bus or the BCC will be that from the correlator chip. When set to 1 the data will be from a psuedo-random number generator. The psuedo-random number generator is reset to the start state when the LS 10 bits of the start address are all 0 for DMA bus transfers, or when the BCC Read Start bit has been set for BCC bus transfers.
BCC Data Out En	When set to 1 this bit allows correlated data to be read back by the BCC Interface. This is used for data retrieval over Ethernet. When set to 0 correlated data is read back by DMA transfer.
Unused	These bits do nothing. They can be used as general memory bits.

3.9 Multibeam Correlator Output Register 3.

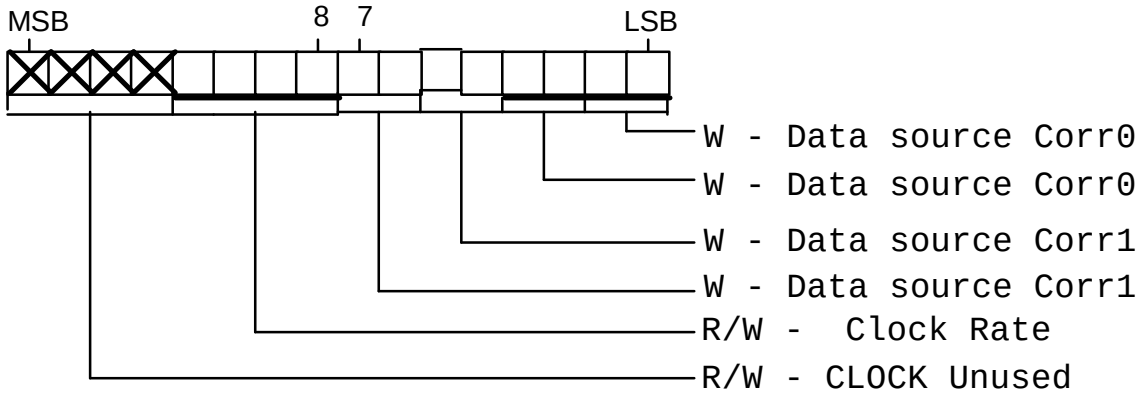
DMA ADDRESS REGISTER (Offset 0xB)



DMA Address. The address as seen by the Correlator Module from reading the Block Ident switch and the Module position. Bits 5, 6, and 7 is the Module position (1 of 8) and bits 8 to 15 is the Block Ident as per the DIP switch on the back of the Mother board.

3.10 Multibeam Correlator Data/Clock Register 1.

MULTI-BEAM DATA/CLOCK GENERATOR REGISTER 1 (Offset 0xC)



Data Source. 2 bits select the data source for the X and Y inputs of the two correlators according to (00 = Sampler 0, 01 = Sampler 1, 10 = Auxillary Input).

Clock Rate. 4 bits select the clock rate of the Correlators.
Clock rate = Input rate / 2 **N
where 0 <= N <= 15
For 128MHz
0 - 128MHz.
1 - 64MHz.
2 - 32MHz.
.....
F - ~1.953KHz.

CLOCK Unused. 4 bits currently not used in the Clock Generator Register. May be written to or read from.

3.11 Multibeam Correlator Data/Clock Register 2.
No register currently available.
3.12 Multibeam Correlator Data/Clock Register 3.
No register currently available.
3.13 Multibeam Correlator Data/Clock Register 4.
No register currently available.

4.0 Pin Description.

This section deal with the pin outs of the two I/O connectors on the Correlator board. The first section is the 256 pin SEIDECON connector to the backplane, and the second is the 20 pin T & B connector on the front edge.

4.1 Backplane Connector.

This is the main connector for the Correlator. All necessary signals for the correlators operation use this connector, as well as Power and Ground.

Type: SIEMENS SIEDECON 256 P/N V23532-A1010-B200.

4.1.1 Pin Name Description.

The names used in this section are those found on the schematic drawing.

Signal direction is as follows:

Input -- from Backplane to Correlator Module,

Output -- from Correlator Module to Backplane,

Input/Output -- may be either Input or Output.

NAME	DESCRIPTION
GND	Ground.
+5V	+5 volt supply.
-5.2V	-5.2 volt supply.
S1_SIGN	Sampler 1 sign signal, positive signal of complementary pair. Input.
~S1_SIGN	Sampler 1 sign signal, negative signal of complementary pair. Input.
S1_MAGNITUDE	Sampler 1 magnitude signal, positive signal of complementary pair. Input.
~S1_MAGNITUDE	Sampler 1 magnitude signal, negative signal of complementary pair. Input.
S2_SIGN	Sampler 2 sign signal, positive signal of complementary pair. Input.
~S2_SIGN	Sampler 2 sign signal, negative signal of complementary pair. Input.
S2_MAGNITUDE	Sampler 2 magnitude signal, positive signal of complementary pair. Input.
~S2_MAGNITUDE	Sampler 2 magnitude signal, negative signal of complementary pair. Input.
BP_SYNC_SIGNAL	Synchronizing signal for correlator when multiple correlators need to be synchronized, positive signal of complementary pair. PECL. Input/Output.
~BP_SYNC_SIGNAL	Synchronizing signal for correlator when multiple correlators need to be synchronized, negative signal of complementary pair. PECL. Input/Output.
BP_DS_A0.....	
BP_DS_A5.	DataSet address bus. Allows sampler to be controlled from correlator in lieu of a serperate DataSet. Single ended TTL. Output.
BP_DS_D0.....	
BP_DS_D7.	DataSet data bus. Allows sampler to be controlled from correlator in lieu of a serperate DataSet. Single ended TTL. Input/Output.
BP_DS_R/W.	DataSet bus Read/Write line. Single ended TTL. Output.
BP_DS_HB/LB.	DataSet bus High byte/Low byte control line. Single ended TTL. Output.
~BP_DS_STRB.	DataSet bus Strobe line, active Lo Single ended TTL. Output.
BP_BCC_A1.....	
BP_BCC_A15.	BCC address bus. Single ended TTL. Input.
BP_BCC_D0.....	
BP_BCC_D15.	BCC Data bus. Single ended TTL. Input/Output.
~BP_BCC_STRB.	BCC bus Strobe signal. Single ended TTL, Active Lo. Input.

~BP_BCC_WR.	BCC bus Read/Write signal. Single ended TTL. Lo = Write, Hi = Read. Input.
~BP_BCC_ACK.	BCC bus Acknowledge signal. Single ended TTL. Output.
BP_RIGHT_CHAN_0..... BP_RIGHT_CHAN_3	4 bit high speed data bus connecting to adjacent module BP_LEFT_CHAN_xx Bus. Positive signal of complementary pair. PECL. Input/Output.
~BP_RIGHT_CHAN_0..... ~BP_RIGHT_CHAN_3	4 bit high speed data bus connecting to adjacent module ~BP_LEFT_CHAN_xx Bus. Negative signal of complementary pair. PECL. Input/Output.
BP_LEFT_CHAN_0..... BP_LEFT_CHAN_3	4 bit high speed data bus connecting to ajdacent module BP_RIGHT_CHAN_xx Bus. Positive signal of complementary pair. PECL. Input/Output.
~BP_LEFT_CHAN_0..... ~BP_LEFT_CHAN_3	4 bit high speed data bus connecting to adjacent module BP_ROGHT_CHAN_xx Bus. Positive signal of complementary pair. PECL. Input/Output.
BP_SAM_BLANK	Sampler Blanking signal. Positive signal of complementary pair. Output.
~BP_SAM_BLANK	Sampler Blanking signal. Negative signal of complementary pair. Output.
BP_SAM_SYNC	Sampler Sync signal. Positive signal of complementary pair. Output.
~BP_SAM_SYNC	Sampler Sync signal. Negative signal of complementary pair. Output.
BP_SPARE_0, BP_SPARE_1	Spare signal for sampler control. May be used for seperate control of second sampler Positive signal of complementary pair. Output.
~BP_SPARE_0, ~BP_SPARE_1	Spare signal for sampler control. May be used for seperate control of second sampler Negative signal of complementary pair. Output.
BP_DMA_0..... BP_DMA_31	DMA I/O data lines. Positive signal of complementary pair. Standard logic TTL, but may be made PECL if alternate bus drivers installed. Input/Output.
~BP_DMA_0..... ~BP_DMA_31	DMA I/O data lines. Negative signal of complementary pair. Standard logic TTL, but may be made PECL if alternate bus drivers installed. Input/Output.
BP_DMAC_0..... BP_DMAC_3	DMA control lines. Positive signal of complementary pair. Standard logic TTL, but may be made PECL if alternate bus drivers installed. Input.*****
~BP_DMAC_0..... ~BP_DMAC_3	DMA I/O data lines. Negative signal of complementary pair. Standard logic TTL, but may be made PECL if alternate bus drivers installed. Input.*****
BP_DMAC_4..... BP_DMAC_7	DMA control lines. Positive signal of complementary pair. Standard logic TTL, but may be made PECL if alternate bus drivers installed. Output.*****
~BP_DMAC_4..... ~BP_DMAC_7	DMA I/O data lines. Negative signal of complementary pair. Standard logic TTL, but may be made PECL if alternate bus drivers installed. Output.*****
BP_EG_0.....	

BP_EG_15	Event Generator signal lines. Positive signal of complementary pair. Input.
~BP_EG_0.....	
~BP_EG_15	Event Generator signal lines. Negative signal of complementary pair. Input.
BP_EG_STROBE	Event Generator Strobe signal. Positive signal of complementary pair. Input.
~BP_EG_STROBE	Event Generator Strobe signal. Negative signal of complementary pair. Input.
BP_BLKID_0.....	
BP_BLKID_7.....	Block Ident. 8 bit code for block number. Single ended TTL. Input.
UNIT_ID_0.....	
UNIT_ID_7.....	Module Ident. 3 bit code for module number within each Block. Single ended TTL. Input.

* NOTE: Signal sets BP_DMAC_xx.
BP_DMAC_2, and BP_DMAC_3 require jumpering to drive DMA control Xilinx.
BP_DMAC_6, and BP_DMAC_7 require jumpering to be driven from DMA control Xilinx.
In all cases total number of control lines cannot exceed 6.

4.1.2 Bus Timings.
The main connector consists of several seperate bus sub-systems. These are:
i) BCC I/O Bus.
ii) DataSet I/O Bus.
iii) DMA Bus.
iv) Event Generator Bus.
This section provides a brief overview of each of these buses.

4.1.2.1 BCC External Bus.
The BCC External Bus is a self contained bus to transfer data between the BCC (host) and the Multibeam Correlator Module (target). For timing details consult Appendix A of this manual or for full information consult the BCC External Bus manual.
Signals in this bus are:
BP_BCC_A1 - BP_BCC_A15, BP_BCC_D0 - BP_BCC_D15, ~BP_BCC_STRB, ~BP_BCC_WR, ~BP_BCC_ACK.

4.1.2.2 DataSet I/O Bus.
The DataSet I/O Bus is a self contained bus to transfer data between the Multibeam Correlator Module (host) and the Samplers (target). For timing details consult Appendix B of this manual.
Signals in this bus are:
BP_DS_A0 - BP_DS_A5, BP_DS_D0 - BP_DS_D7, BP_DS_R/W, BP_DS_HB/LB, ~BP_DS_STRB.

4.1.2.3 DMA Bus.
The DMA I/O Bus is a self contained bus to transfer data from the Multibeam Correlator Module (target) to the main data processing Computer (host). For the default timing information consult Appendix C of this manual.
Signals in this bus are:
BP_DMA_0 - BP_DMA_31, BP_DMAC_0 - BP_DMAC_7.

4.1.2.4 Event Generator Bus.
The Event Generator Bus is a self contained bus to transfer data (events) from an Event generator to the between the Multibeam Correlator Module. For the timing information consult the Event Generator Manual.
Signals in this bus are:
BP_EG_0 - BP_EG_15, BP_EG_STROBE.

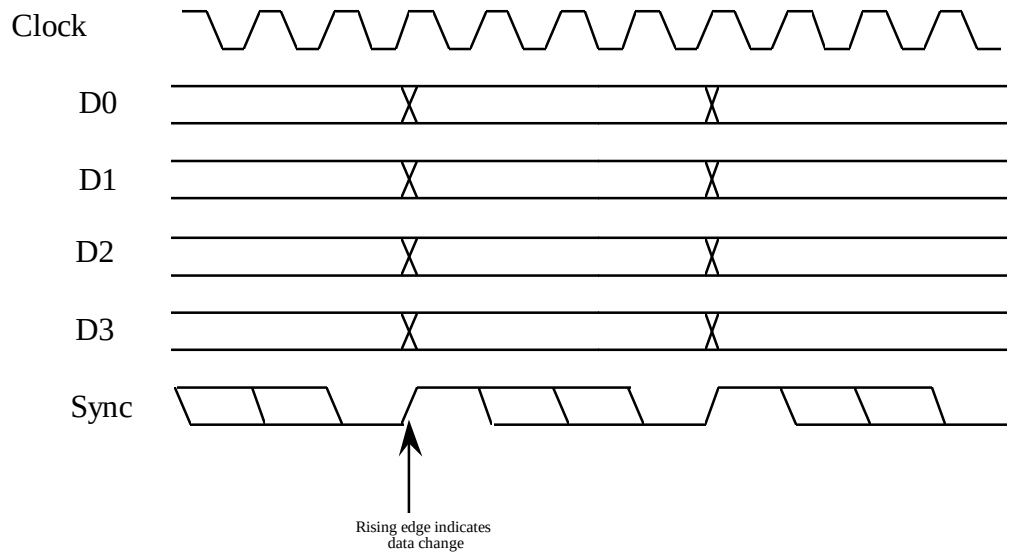
4.2 Front Connector.

This is the auxillary connector for the Correlator. This is to allow alternate sampler signals to be feed to the correlator.

TYPE: T & B Ainsley 609-2007 or equivalent.

EXT_AUX_SIGN_0.....	
EXT_AUX_SIGN_4	External Sign signal. Positive signal of complementary pair. ECL. Input.
~EXT_AUX_SIGN_0.....	
~EXT_AUX_SIGN_4	External Sign signal. Negtive signal of complementary pair. ECL. Input.
EXT_AUX_MAGN_0.....	
EXT_AUX_MAGN_4	External Magnitude signal. Positive signal of complementary pair. ECL. Input.
~EXT_AUX_MAGN_0.....	
~EXT_AUX_MAGN_4	External Magnitude signal. Negative signal of complementary pair. ECL. Input.

Note:
Signal set EXT_AUX_SIGN_4 allocated for synchronizing signal, and signal set EXT_AUX_MAGN_4 unused.



AUXILLARY INPUT SIGNAL TIMING

5.0 Hardware Configuration.
This section deal with the hardware configuration.

5.1 Jumper Links.
This section deal with the setting of the various links on the board to activate the various options. States shown in **BOLD** face are the default.

Link	State	Function
LK10	**OPEN**	Xilinx Configuration Mode - Serial Slave XC4.
	CLOSED	Xilinx Configuration Mode - Serial Master XC4. Xilinx prom must be installed in U5. See also LK42 and LK43.
LK12	OPEN	Xilinx Configuration Mode - Serial Slave XC5.
	CLOSED	Xilinx Configuration Mode - Serial Master XC5. Xilinx prom must be installed in U16.

LK30	OPEN	Xilinx Configuration Mode - Serial Slave XC2.
	CLOSED	Xilinx Configuration Mode - Serial Master XC2. Xilinx prom must be installed in U14. See also LK11 and LK31.
LK40	OPEN	Xilinx Configuration Mode - Serial Slave XC1.
	CLOSED	Xilinx Configuration Mode - Serial Master XC1. Xilinx prom must be installed in U20.
LK50	OPEN	Xilinx Configuration Mode - Serial Slave XC3.
	CLOSED	Xilinx Configuration Mode - Serial Master XC3. Xilinx prom must be installed in U80.
LK41	**OPEN**	PCB Clock rate - FAST.
	CLOSED	PCB Clock rate - SLOW.
LK41	**OPEN**	XC3 uses XC3020, XC3030, or XC3042.
	CLOSED	XC3 uses XC3064, XC3090, or XC3095.
LK11	**ALL OPEN**	For XC2 Configuration Mode - Serial Master.
	1 - 2)	Connects appropriate control lines to XC2 for
	3 - 4)	external Xilinx configuration. See also LK30
	5 - 6).	and LK31.
LK31	**1 - 2**	XC2 reset from system reset. PCB comes with this link hard wired. Cut PCB track between pins 1 and 2 on rear side of PCB to remove this default. See also LK11 and LK30.
	2 - 3)	XC2 reset from external download source. See also LK11 and LK30.
LK43	**ALL CLOSED**	For XC4 Configuration Mode - Serial Master.
	1 - 2)	Connects appropriate control lines to XC4 for
	3 - 4)	external Xilinx configuration. See also LK10
	5 - 6).	and LK42.
LK42	1 - 2	XC4 reset from system reset. PCB comes with this link hard wired. Cut PCB track between pins 1 and 2 on rear side of PCB to remove this default. See also LK10 and LK43.
	2 - 3)	XC2 reset from external download source. See also LK10 and LK43.

5.2 Wire Wrap Links.

In general the DMA Control Bus consists of 4 input signals (from external source) and 4 output signals (to external source). Due to the limited number of I/O pins on the 84 pin Xilinx chip, 2 input control lines and 2 output control lines are hard wired and the remaining 4 control lines made optional. This would allow those unsed Xilinx pins to be used for any as yet unforseen purpose.

WW1/WW8	Input from DMA Control Bus line #2 to XC2.
WW2/WW6	Input from DMA Control Bus line #3 to XC2.
WW3/WW7	Output to DMA Control Bus line #6 from XC2.
WW4/WW5	Output to DMA Control Bus line #7 from XC2.

5.3 On board Oscillator.

The on board oscillator is the clock by which all the control logic is stepped. This includes BCC interface, DMA interface, DataSet interface emulation and Display interface. It does not have any effect on the Correlator data flow or clocking (other than data path or clock rate enabling), or the Event Generator Strobe.

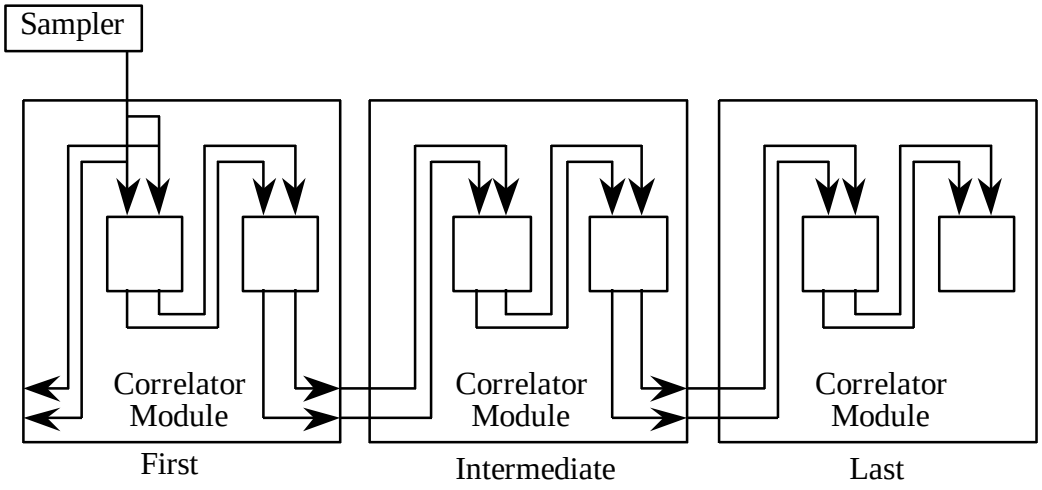
The recomended frequency for the oscillator is 10 - 20MHz, with 16MHz being preferred. Frequencies up to 40 MHz are supported, however the speed link (LK41) should be installed for clock rates above 20MHz. This is to give proper timing values in the hand shake protocol for the BCC. Performance of the DataSet emulation bus at speeds above 20MHz will also need to be evaluated.

Since the DMA interface requires interaction with the far end (host) changing the clock rate from say 16MHz to 40 MHz will produce only a small increase in data rate as there is large delays in the handshake turnaround at the far end.
For the DataSet emulation interface, as the protocol is only controlled by the host (the correlator board), there is a 1:1 linear relationship with clock speed and data rate. If this bus is being used to communicate with devices other than the ATNF Multibeam Samplers, be sure that the setup and hold time comply with that required.

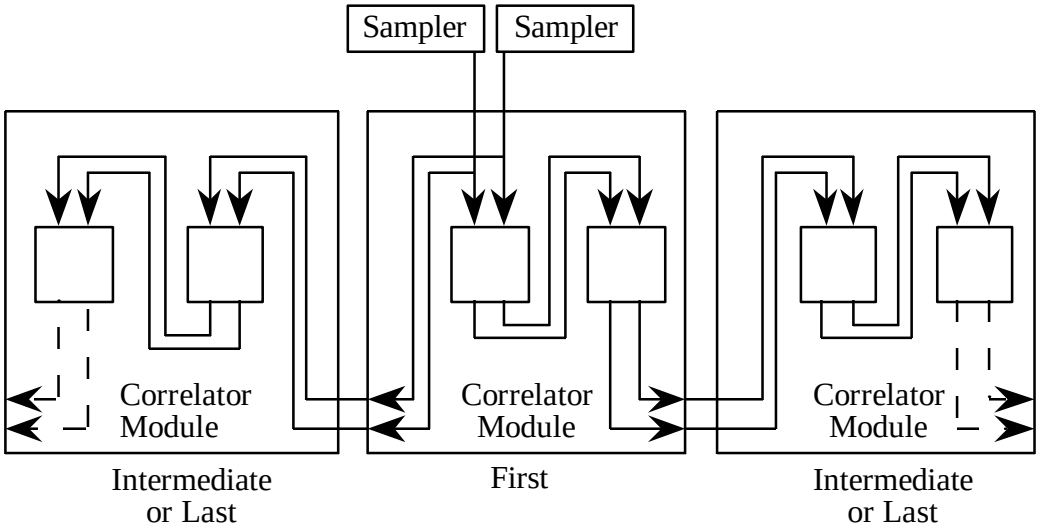
5.3 Concatenation Chain (NOT CURRENTLY IMPLEMENTED 10/3/97)
Logic exists to concatenate one Correlator Module with another, both within a Block and beyond. In all cases both delayed and undelayed data is passed along the concatenation bus. This precludes the need to connect the output from the particular sampler with all Modules that require the signal. Terminology used here is that used for the standard ATNF CA Correlator.

The board has been layed out to support 3 different modes of concatenation. These are:
i) Concatenation of both correlator ICs with subsequent Correlator Modules. Useful for maximum resolution from each Correlator Module. Can be for autocorrelation or crosscorrelation. When used for crosscorrelation there must be a matched lag set.
ii) Seperate concatenation of each correlator IC with subsequent Correlator Modules. Useful for autocorrelating 2 samplers when connected to the same Correlator Module. One concatenation chain can concatenate to the left while the other concatenates to the right. With crosscorrelation, all positive lags can be concatenated to one side, while the negative lags can concat to the other. Subsequent Correlator Modules can devote one or both correlator ICs to the concatenation chain.
iii) Concatenation of one correlator IC only with subsequent Correlator Modules. A subset of ii). Useful for autocorrelation only.

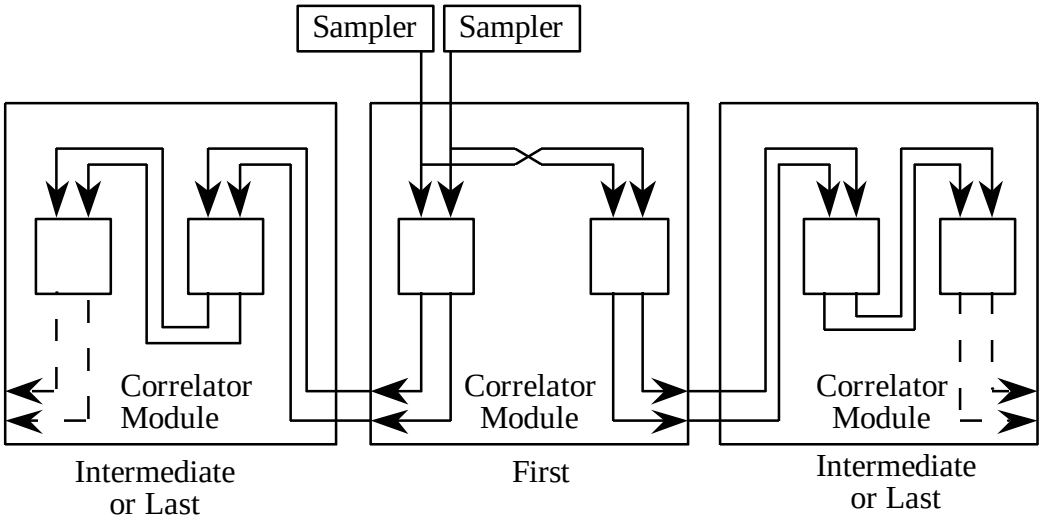
When Correlator Modules are concatenated, they must take on one of 4 possible positions; None, First, Intermediate or Last.
None is when no concatenation takes place. The concatenation buses are all disabled.
First is when one or both concatenation buses are exporting data and the input signal to the Correlator Module is from the Sampler (or Auxillary input).
Intermediate is when the Correlator Module is receiving from one concatenation bus and exporting the data through the other concatenation bus.
Last is when the Correlator Module is receiving from one or both concatenation bus and not exporting that data.



CONCATENATION - BOTH CORRELATOR ICs
AND SUSEQUENT MODULES

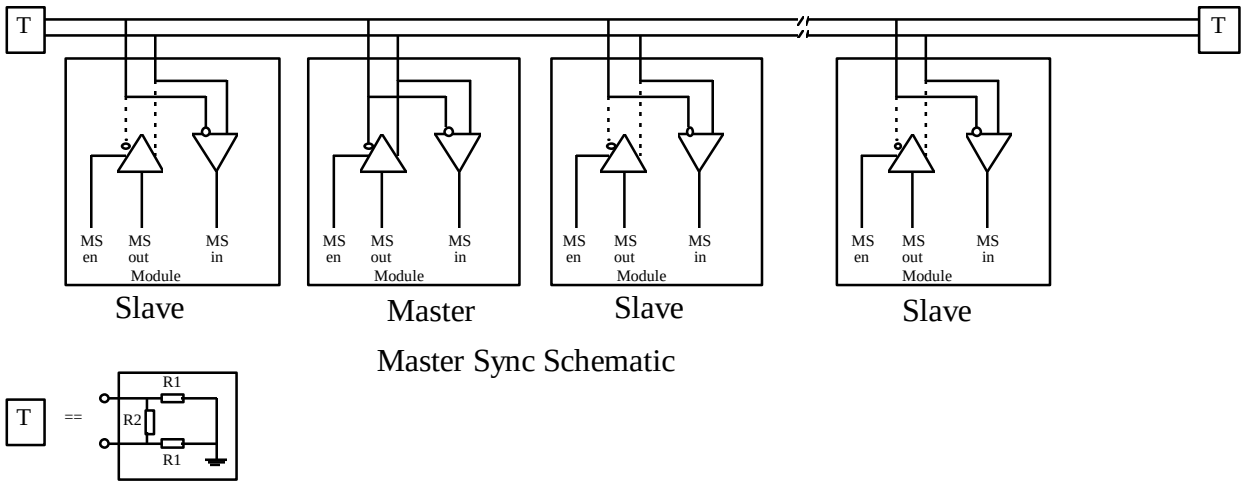


CONCATENATION - BOTH CORRELATOR ICs
AND SUBSEQUENT MODULES



CONCATENATION - EACH CORRELATOR IC
AND SUBSEQUENT MODULES

5.4 Master Sync (NOT CURRENTLY IMPLEMENTED 10/3/97)
Logic exists to allow Correlator Modules to be Clock synchronized. Each Correlator Module has a tri-statable balanced PECL driver and receiver to allow a synchronizing signal to be exported and/or imported. The synchronizing signal must be the slowest signal in the system. There can be only one Master. It is intended that the Master's Correlator clock would synchronize itself from the signal off this bus. If so desired the synchronizing signal can come from an external source.
There must be a termination at both end of the bus. This should be a TT (pi) to ground with a Z_0 of 100 ohms.



Master Sync Schematic

6.0 Programming.
There are many ways to programme the correlator. This section deals with the steps needed to get the correlator up and running in a fairly basic mode. It also includes a section listing other possible options.

6.1 Full bandwidth, autocorrelation.
This is the most simple configuration. To run this mode it is necassary to perform the following tasks:
1. Setup the Event Generator lines.
2. Enable the data paths and select the full correlator clock rate.
3. Enable the Correlator.
These tasks setup all the static control of the correlator. The dynamic control is performed by the (external) Event Generator.
1.Setup the Event Generator lines.
This operation connects the dynamic control signals to the desired Event Generator lines. The selection is limited to either the lower 8 bits or the upper 8 bits of the Event Generator Bus. To select which half, set the EG Range Select bit in the Correlator Register 4 by writing a 1 or 0 to that bit:
To set: CorrelatorRegister4 | 0x100 -> CorrelatorRegister4
To reset: CorrelatorRegister4 & ~0x100 -> CorrelatorRegister4

There are three dynamic control lines that must be set: Correlator Blank, Integrate and Run, and two others that are optional: Sampler Sync, and Sampler Blank. These can be found in Correlator Register 0, for Correlator IC 0, and in Correlator Register 1 for Correlator IC 1. The actual values will depend on which bit of the Event Generator Bus will be assigned for the task. The optional signals should be set to an unused Event Generator line. Load the appropriate field in these registers with the number of the Event Generator line to use. As an example, if bit 2, 3, 4 of the Event Generator Bus are to control Correlator Blank, Integrate and Run respectively, with Sampler Sync, and Sampler Blank connecting to 0, then to set these for correlator IC 0:
(2 << 12) | (3 << 9) | (4 << 6) | (0 << 3) | 0 -> CorrelatorRegister0.

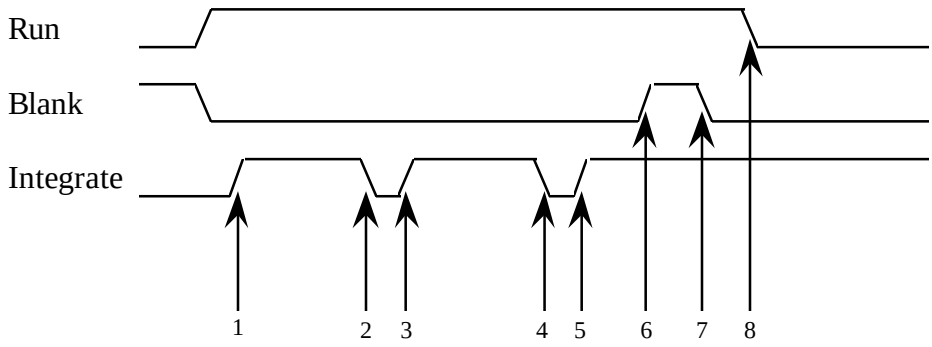
2. Enable the data paths and Select the full correlator clock rate.

This operation connects the Correlator IC data inputs to the desired data signals and selects the clock divider ratio. The usual case is Correlator IC 0 taking data from Sampler 0 and Correlator IC 1 taking data from Sampler 1. For full bandwidth the divider ratio is 0:
(0 << 8) | (1 << 6) | (1 << 4) | (0 << 2) | 0 -> CorrelatorRegister 0xC

3. Enable the Correlator.
This operation enables the internal workings of the correlator IC. For Correlator IC 0 this is through Correlator Register 2 and for Correlator IC 1 this is through Correlator Register 3. There are 5 bits that must be set. These are: Input Mode, Test, Double and Reset. The default state is that Correlator IC 0 connects to Sampler 0 and Correlator IC 1 connects to Sampler 1, with the remaining signals set for no Test, no Double and no Reset (ie ready to run normally). If in doubt (to be sure, to be sure, to be sure) load this register with all zeros:

0x0000 -> CorrelatorRegister2.

6.2 Correlating.
The Event Generator can now be run to control the correlator so as to correlate. The 3 main dynamic control signals Correlator Blank, Integrate and Run, need to be switched at the appropriate times for each integration period. As an example:



Integration Cycle Control

1. With Run Hi and Blank Lo, Integrate is bought Hi. The accumulators accumulate the results of the multipliers.
2. Integrate bought Lo. This completes the integration process started at 1. Data for this period is now available from the output data registers. The accumulators are reset.
3. Integrate bought Hi. A new integration period is started.
4. Integrate bought Lo. This completes the second integration cycle. Data for this period is now available from the output data registers. The accumulators are reset.
5. Integrate bought Hi. A new integration period is started.
6. Blank bought Hi. Accumulation stops. Contents of accumulators remains unchanged. Input data is still being shifted through the Correlator IC.
6. Blank bought Lo. Accumulation resumes.
7. Run bought Lo. Input data ceases to be shifted through the correlator IC. Accumulation continues on last data presented to each multiplier. Possibly not a good state to be in.

6.3 Correlated Data Transfer.
After each integration period the correlator data can be transferred from the internal accumulators of the Correlator ICs to the data proceessing computer, This can be done though 2 channels: the high speed DMA port or the BCC data port.
The Correlator ICs appear as a FIFO to both these data ports. Consequently each lag can only be read once. Data comes out from lag 0 through to lag 1023, plus the Total Count (1025 reads in all).
To read via the BCC port it is necessary to:
1. Enable BCC data retrieval.

2. Setup which Correlator IC to read.
3. Read the LS word (16 bits).
4. Read the MS word (16 bits).
5. repeat 2 and 3 till all data has been read. It is not necassary to read all lags if so desired.
The read operation must be completed before the end of the next integration period as the data held in the readout registers will be over written.
1. Enable BCC data retrieval. To allow data to be retrieved by the BCC Interface set the BCC Data Out En bit in Correlator Output Register 3 (offset 0xA). Thus

0x0020 -> CorrelatorOutputRegister3.

2. Select which correlator IC to read. To set which correlator IC to read set the Correlator Chip Select bit in Correlator Output Register 3 (offset 0xA). For Correlator IC 0 set this bit to 0 and for Correlator IC 1 set this bit to 1. . Thus to read Correlator IC 1:

0x0001 | CorrelatorOutputRegister3 -> CorrelatorOutputRegister3.

3. Read the LS word (16 bits). The LS word must be read first for each 32 bit transfers. This is done by reading the Correlator Output Register 0 (offset 0x8):

CorrelatorOutputRegister0 -> BCC.

4. Read the MS word (16 bits). After reading the LS word the MS word must be read for each 32 bit transfer. This is done by reading the Correlator Output Register 1 (offset 0x9):

CorrelatorOutputRegister1 -> BCC.

By combining the values from 2, and 3 shifted left 16 bits, the 32 bit accumulator result is obtained.

5. Repeat 2 and 3 till all data has been read. After the MS word has been read the next 32 bit word can be recovered from the Correlators accumulators. It is not necessary to recover all the lags if so desired, as the contents of the accumulator will be over written at the end of the next integration cycle.

6.4 Other Option.

There are many ways to configure the correlator. This is a list of some of them. It is based on what is available with the PCB layout. In some instances it may require further development of the associated Xilinx FPGAs.

Correlators.
1. Two seperate autocorrelators.
2. A single autocorrelator using both Correlator ICs to correlate.
3. A single crosscorrelator using both Correlator ICs to correlate.

Data sources.
1. One or two Samplers.
2. Auxillary input.
3. Concatenation bus, Left and/or Right.

Concatenation. (Use of concatenation will require further development of the FPGA's)
1. Data from one Correlator IC out both Left and Right Concatenation Bus.
2. Data from one Correlator IC out the Left Concatenation Bus and data from the other Correlator IC out the Right Concatenation Bus.
3. Data in from one Concatenation Bus, into one or both Correlator ICs.
4. Data in from one Concatenation Bus, through one or both Correlator ICs and out the other Concatenation Bus.
5. Data in from one Concatenation Bus, into one Correlator IC and data in from the other Concatenation Bus, into the other Correlator IC.

7.0 Notes on the Xilinx devices.
This section deals with the design aspects of the various Xilinx FPGAs used on the board. There are 5 such devices each layed out to perform distinct functions. These are:
i) BCC interface (XC1).
ii) DMA interface (XC2).
iii) Display (XC3).
v) Clock Generation (XC4).
iv) Data generation (XC5).

Currently, all Xilinx designs are done using PROTEL schematic capture, and a flat schematic model (as opposed to a heirachic model). To build a Xilinx netlist, run the netlist generator within PROTEL, making sure to select the Xilinx netlist format. With the flat model, the netlister produces a set of files; one for each sheet of the drawings. It is necessary to merge these into one file for the XACT software. To do this, from a DOS prompt run the MERGE program. This will ask for the name of the top netlist file, and ask for an output file. After this MERGE will open the top netlist file, and the merge all files referenced in the designated output file. This output file should then be used in the XACT software to generate the Xilinx layout.

7.1 BCC interface Xilinx.
The BCC interface Xilinx FPGA handles both the BCC data interfacing as well as the Event Generator interface and the DataSet emulation interface.
7.1 1 BCC interface Key functions.
Key functions are:
i) Map all registers on the board (including registers in other Xilinx FPGAs).
ii) Selection of Event Generation lines to Event Generator input signals.
iii) Distribution of Event Lines.
iv) Control of some Correlator control lines.
v) DataSet auxillary bus emulation.
vi) Gateway for the remote downloading of the Data Generation Xilinx FPGA and the DMA interface Xilinx FPGA.

7.1 2 Display output.
Display information is transmitted serially to the Display Xilinx FPGA (XC3) using the PCB clock and 2 signal lines. One signal line contains the data and the other signal lines is the Sync. Data is clocked into the Display Xilinx FPGA on the rising edge of the PCB clock. When all bits have been sent, the Sync signal goes Hi for one clock period. When the Display Xilinx FPGA sees the Sync bit hi and on the rising edge of the PCB clock, the preceeding bits are loaded internally in the Display Xilinx FPGA. See Display Xilinx section for more information. As the onboard clock is a fundemental clock of this Xilinx FPGA, normal shift register logic is used to send the data out.

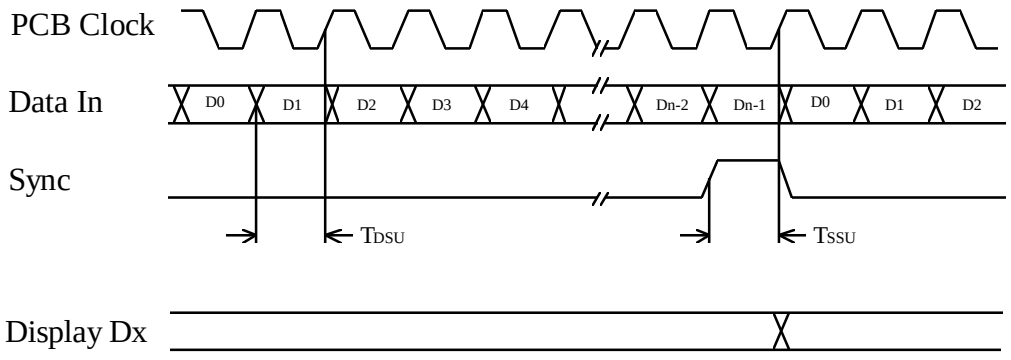
7.2 DMA Interface Xilinx.
The DMA Interface Xilinx FPGA handles both the DMA interfacing between the Correlator ICs and the External DMA bus. The default protocol is that used by the CA ATNF correlator, modified for 32 bit wide data transfers (but maintaining 24 bit addressing).
7.2.1 DMA Interface Key functions.
Key functions are:
i) Address request recognition.
ii) Data transfer out.
iii) Psuedo-random data output for DMA bus testing.
This Xilinx FPGA may be setup for remote configuration loading via the BCC.

7.2.2 Display output.
Display information is transmitted serially to the Display Xilinx FPGA (XC3) using the PCB clock and 2 signal lines. One signal line contains the data and the other signal lines is the Sync. Data is clocked into the Display Xilinx FPGA on the rising edge of the PCB clock. When all bits have been sent, the Sync signal goes Hi for one clock period. When the Display Xilinx FPGA sees the Sync bit hi and on the rising edge of the PCB clock, the preceeding bits are loaded internally in the Display Xilinx FPGA. See Display Xilinx section for more information. As the PCB clock is a fundemental clock of this Xilinx FPGA, normal shift register logic is used to send the data out.

7.2 Display Xilinx.
The Display Xilinx FPGA handles the displaying of various pieces of information on the 16 LEDs grouped together on the front edge of the PCB.

7.3.1 Display Key Functions.
Key functions are:
i) On initialization display the board address for several seconds.
ii) Display selected bits, including Event Generator strobe, DataSet strobe, from the other Xilinx FPGA in the board.

7.3.2 Display Input.
Some display information is transmitted serially from the various Xilinx FPGA on the board to this Xilinx FPGA using the PCB clock and 2 signal lines. One signal line contains the data and the other signal lines is the Sync. Data is clocked into the Display Xilinx FPGA on the rising edge of the PCB clock. On the last data bit, the Sync signal is set Hi for one clock period. When the Display Xilinx FPGA sees the Sync bit hi and on the rising edge of the PCB clock, the preceeding bits are loaded into the display registers and displayed.



DISPLAY DATA INPUT SIGNAL TIMING

TDSU (Data SetUp) and TSSU (Sync SetUp) are for the selected Xilinx used for the Display controller.

7.3.3 LED Display Definition.
The following are displayed on the correlator LED display:
LD10 - Unit ID0
LD11 - Unit ID1
LD12 - Unit ID2
LD18 - Local Clock Presence
LD20 - PSR Enable
LD21 - Correlator Select
LD22 - DMA Request
LD23 - DMA Next
LD24 - Event Generator Strobe
LD25 - Dataset Strobe

7.4 Clock Generation Xilinx.
The Clock Generation Xilinx FPGA generates the clock for the Correlator chips and the Data Generation Xilinx FPGA. The Clock Generation Xilinx FPGA uses "-2" speed grade devices. The use of (just released) "-1" or "-09" devices may alleviate the timing problem. The main problem designers will encounter is having the right data setup times for the Correlator chip (and to a lesser extent the Data Generation Xilinx chip) for the fastest clock rate. As slower clock rates decrease by a power of 2, data setup times should not be a problem for these.

7.4.1 Clock Generation Key Functions.

Key functions are:

i) To provide clock signal to correlator ICs, Data Generation FPGA, and to the Samplers.

ii) To provide a synchronizing clock when choosen as the Master. (Not currently implemented 10/3/97)

ii) To provide synchronizing logic. (Not currently implemented 10/3/97)

7.4.2 Pin assignment.

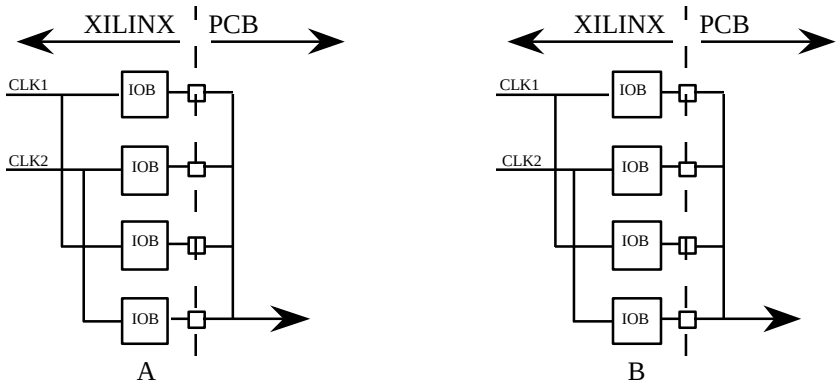
The pin assignments were setup to allow for maximum flexibility with both output drive and timing. This was achieved by allocating 4 pins to each of the 5 major users: the correlator chips, the samplers, and the Data Generation Xilinx chip.

This configuration allows the following 3 possible alternatives:

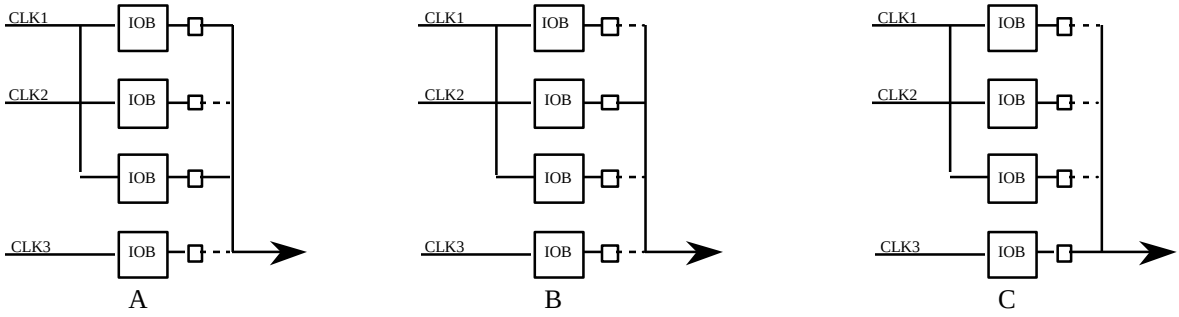
i) 2 X 2 identical types of output,

ii) 2 X 1 and 1 X 2 outputs (total 3 types).

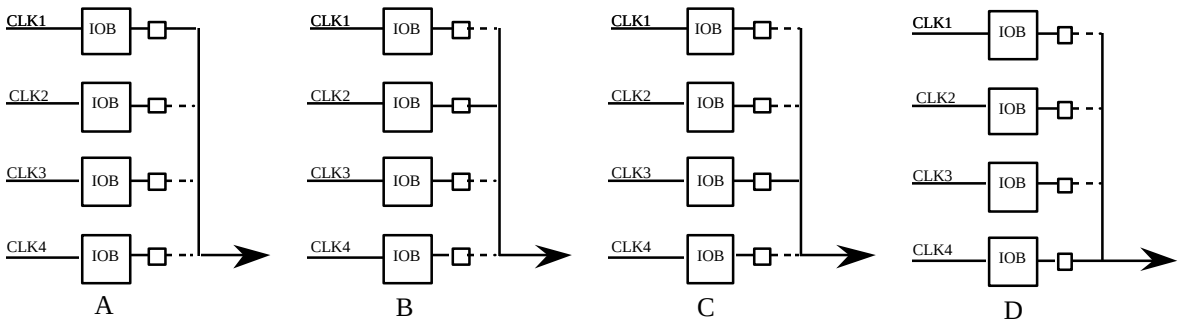
iii) 4 X 1 type outputs.



2 X 2 outputs



2 X 1 & 1 X 2 outputs



4 X 1 outputs

Configuration (i) allows two outputs to be paralled together to increase the drive capability if needed. Care must be exercised when pairing the outputs off; they should have pretty much the same propagation times. The unused outputs are tri-stated.
Configuration (ii) allows one output to be paralled together to increase the drive capability if needed (as in (i) above) and two single pin outputs for alternate clock timing. Care must be exercised when pairing the outputs off; they should have pretty much the same propagation times. The unused outputs are tri-stated.
Configuration (iii) allows four single pin outputs for alternate clock timing.

Pin Pairs

Group	Pair 1	Pair 2	Destination
1	35/37	36/38	Correlator 0 clock.
2	44/46	45/47	Correlator 1 clock.
3	80/82	81/83	Sampler 0 clock.
4	76/78	77/79	Sampler 1 clock.
5	5/7	4/6	Data Generation clock.

Note: Pair 1 offer the fastest connection directly to the internal clock signal.

For both configurations (i. and ii), the outputs must operate in a different mode between the maximum speed (where the board clock equals the correlator clock) and for all speeds slower (1/2**n of the board clock). As an example, for the Correlator 0 clock, at maximum clock rate (MCR), pair 1 would be active with pair 2 tri-stated, and for all lesser rates (MCR/2, MCR/4....), pair 1 would be tri-stated with pair 2 active. If the added drive was not required, only one pin in each pair need be active.
The pair used for slower clock rates should be setup to be "clocked output", where the IOB clock is the Xilinx clock, and the data is the slower clock rate. This technique produces the most predictable timing regime.

7.4.3 Implementing the design.
To implement the design it may be necessary to manually route the critical nets first. Using a blank or new design, edit the LCA design using the netnames in the schematic, by placing the nets, and enabling the IOB accordingly. Once completed, use this design as a *GUIDE DESIGN* and let the XACT PPR process route the remaining logic.
The clock divider has implemented as serial divider; for a given output rate, Terminal Count (TC) outputs of all previous stages are forced into the Terminal Count state.

7.4.4 Display output.
Display information is transmitted serially to the Display Xilinx FPGA (XC3) using the PCB clock and 2 signal lines. One signal line contains the data and the other signal lines is the Sync. Data is clocked into the Display Xilinx FPGA on the rising edge of the PCB clock. When all bits have been sent, the Sync signal goes Hi for one clock period. When the Display Xilinx FPGA sees the Sync bit hi and on the rising edge of the PCB clock, the preceeding bits are loaded internally in the Display Xilinx FPGA. See Display Xilinx section for more information. As the PCB clock is not a fundemental clock of this Xilinx FPGA, normal shift register logic is not used to send the data out.

7.5 Data Generation Xilinx.
The Data Generation Xilinx transfers data from the input and drives it to the selected output. The Data Generation Xilinx FPGA uses "-2" speed grade devices. The use of (soon to be released) "-1" or "-09" devices may alliviate the timing problem. The main problem designers will encounter is having the right data setup times for the Correlator chip and concatination path for the fastest clock rate. As slower clock rates decrease by a power of 2, data setup times should not be a problem.
7.5.1 Data Generation Key Functions.
Key functions are:
i) To transfer data from any input to the appropriate Correlator IC.
ii) To convert input data format to that required by the Correlator ICs where necessary.
ii) To transfer data from appropriate inputs to Concatenation outputs.

7.5.2 Pin assignment.

The pin assignments were allocated to the following signal to allow for maximum flexibility with input timing for input only signals, and input and output timing for bi-directional signals. This was achieved by allocating 2 pins to each of these signals.

Signal	Xilinx Pins	Type
RIGHT_CHAN_0	81,82	Input/output
RIGHT_CHAN_1	79,80	Input/output
RIGHT_CHAN_2	77,78	Input/output
RIGHT_CHAN_3	75,76	Input/output
LEFT_CHAN_0	62,63	Input/output
LEFT_CHAN_1	66,67	Input/output
LEFT_CHAN_2	68,69	Input/output
LEFT_CHAN_3	70,71	Input/output
CASCADE_10_0	50,52	Input
CASCADE_10_1	46,48	Input
CASCADE_01_0	35,37	Input
CASCADE_01_1	39,41	Input

For RIGHT_CHAN_* and LEFT_CHAN_* signals, the timing will depend on the propagation delay of the balanced drivers on both the sending and receiving logic, as well as the logic delays in both the sending and receiving Xilinx chip. For CASCADE_* signals, the timing will depend on the propagation delay of the Correlator chips and the logic delays in the receiving Xilinx chip.
With each signal routed to 2 pins it is possible to have two different software selectable input timing regimes which may be altered according to the clock rate, eg input 1 could be clocked on the positive edge, and input 2 on the negative edge. With slower clock speeds (say < 100MHz), such race conditions may not be a problem.

7.5.3 Display output.

Display information is transmitted serially to the Display Xilinx FPGA (XC3) using the PCB clock and 2 signal lines. One signal line contains the data and the other signal lines is the Sync. Data is clocked into the Display Xilinx FPGA on the rising edge of the PCB clock. When all bits have been sent, the Sync signal goes Hi for one clock period. When the Display Xilinx FPGA sees the Sync bit hi and on the rising edge of the PCB clock, the preceeding bits are loaded internally in the Display Xilinx FPGA. See Display Xilinx section for more information. As the PCB clock is not a fundemental clock of this Xilinx FPGA, normal shift register logic is not used to send the data out. See circuits used in the Clock Generator Xilinx.

8.0 Transfering data using the DMA Bus.

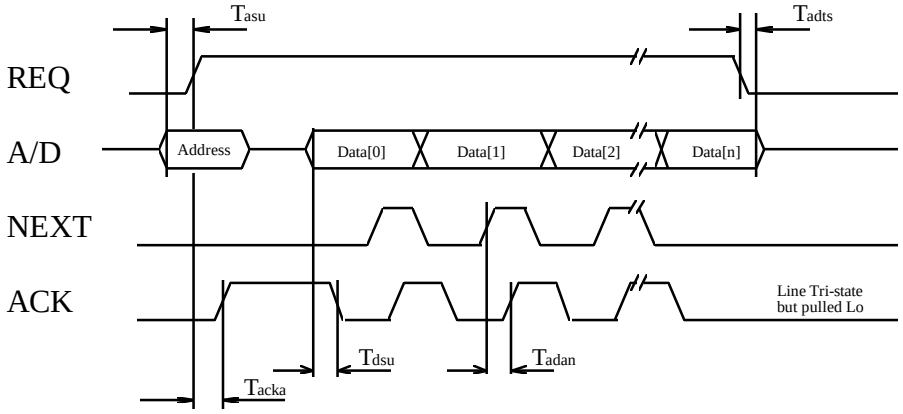
This sections deals with the transfer of data from the Correlator Module to the external computer via the DMA bus. This bus allows 32 bit data transfers using the same protocol as with the correlators on the ATNF Compact Array. At the Correlator Module end, the protocol is handled by a Xilinx FPGA. Provision has be made to allow this FPGA to be externally configured.
The protocol consists of 3 control lines, and 32 address/data lines. The 3 control lines are:

Name	Source
REQuest	Master
NEXT	Master
ACKnowledge	Correlator

The Address/Data lines are bidirectional.

To transfer data, the Master places the start address of where to get data from onto the Address/Data lines. After a short period to settle, the Master asserts the REQuest line. The target seeing REQuest go Hi, loads the address on the Address/Data lines into its holding / comparator registers, and checks the address to see if it is it that is being addressed. If not, no further action occurs. If so, the target places a Hi on the ACKnowlege line and enables that driver. On seeing ACKnowlege go Hi, the Master tri-states the Address/Data lines in readiness for data to be sent back from the target. Meanwhile, the target has accessed the first address and after a short while

(to allow the Address/Data bus to go tri-state), loads this data onto the Address/Data. After this has had time to settle, the target sets the ACKnowledge Lo. This tells the Master that data on the Address/Data bus is valid. The Master loads this data and sets the NEXT line Hi. The target on seeing the NEXT line Hi, immediately sets the ACKnowledge Hi, and proceeds to get the next data word and places it on the Address/Data bus. The Master on seeing ACKnowledge go Hi sets NEXT Lo. After the data lines have had sufficient time to settle, the target sets ACKnowledge Lo, and the cycle is repeated. The transfer continues until the Master de-asserts the REQuest line.



DMA Bus transfer

Parameter	Description	Min	Typ	Max	Units
Tasu	Address Setup time	20			nS
Tacka	ACK asserted time	6			T
Tdsu	Data Setup time	2			T
Tadan	ACK de-asserted after NEXT	1			T
Tadts	Address/Data tri-state time			1	T

T == On board oscillator period.

9.0 Hardware faults.

This sections deals with known hardware faults and their fixes.

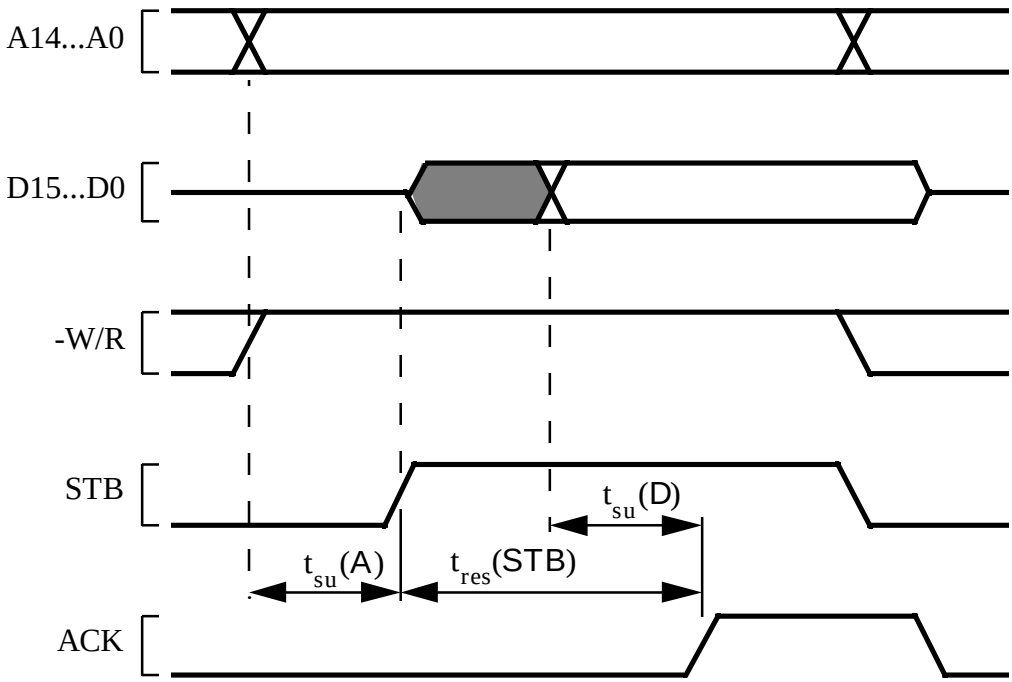
1. Signal BCC_D2 conflict on LDC pin on Data Generation Xilinx IC XC4.

Problem: When Data Generation Xilinx IC XC4 is not configured the LDC pin is an active output set Lo. This conflicts with the BCC data line D2. If the Data Generation Xilinx IC XC4 is configured from the onboard prom, then this would not be a problem. If however the option of external configuration is used, then this problen may render BCC data line D2 useless.

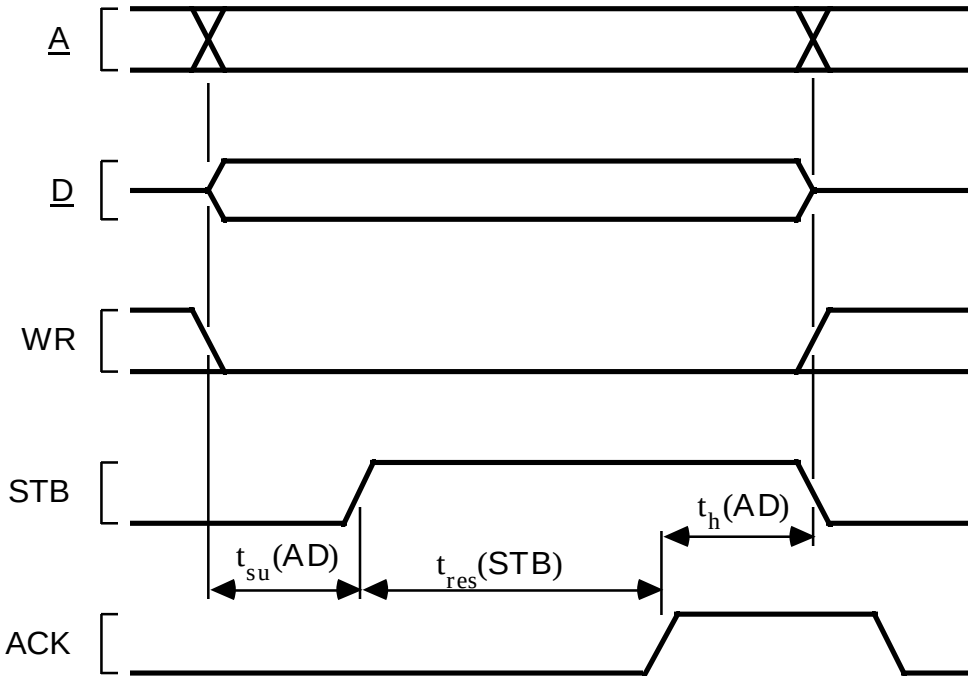
Fix: On the rear side, cut track leading from pin 36 of Data Generation Xilinx IC XC4, just near the via adjacent to that pin . Scratch the Solder resist from the track leading to the next via, at about the length of a surface mount resistor from the first via. Solder a 5K6 ohm resistor across the cut, with one end on the first via, and the other end on the track now clear of solder resist. For a permanent fix, on the PCB layout, place a surface mount resistor at about this spot.

Appendix A - BCC External Bus Timing.

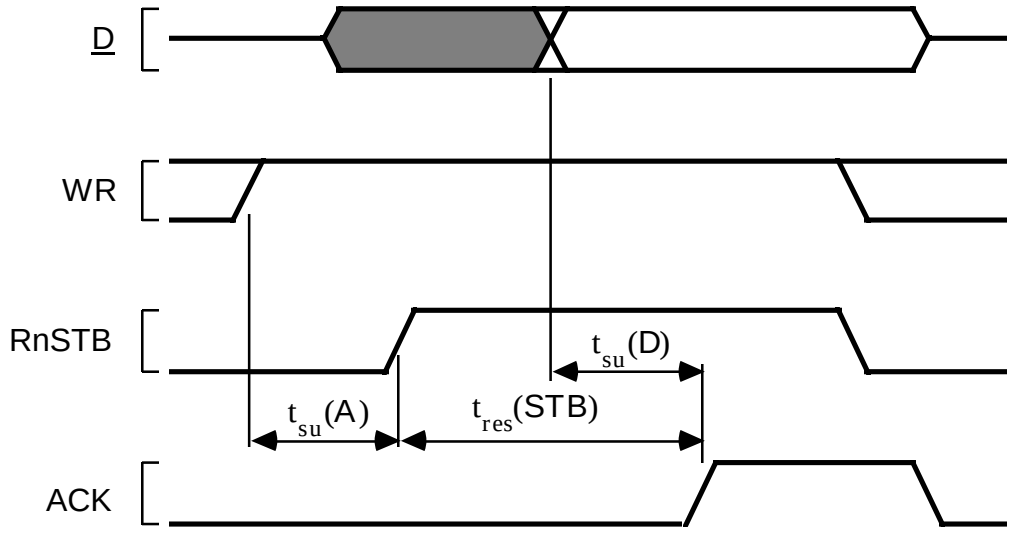
The information in this section was taken from BCC External Interface manual.



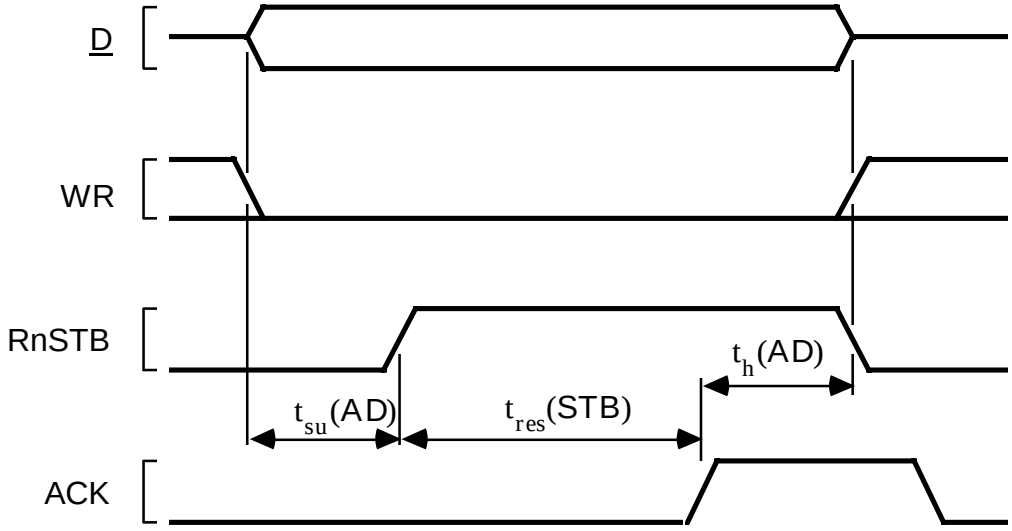
Fig(2): Addressable Read Transaction



Fig(3): Addressable Write Transaction.



Fig(4): Register Read Transaction.



Fig(5): Register Write Transaction

Quantity		**Min**	**Max**
t_{su}(A)	Address setup.	60nS	
t_{su}(D)	Data hold.	5nS	
t_{su}(AD)	Address/Data setup.	60nS	
t_h(AD)	Address/Data hold.	5nS	
t_{res}(STB)	Strobe response.		2µS

Table(2): External Bus timing constraints.

Appendix B - DataSet I/O Bus Timing.

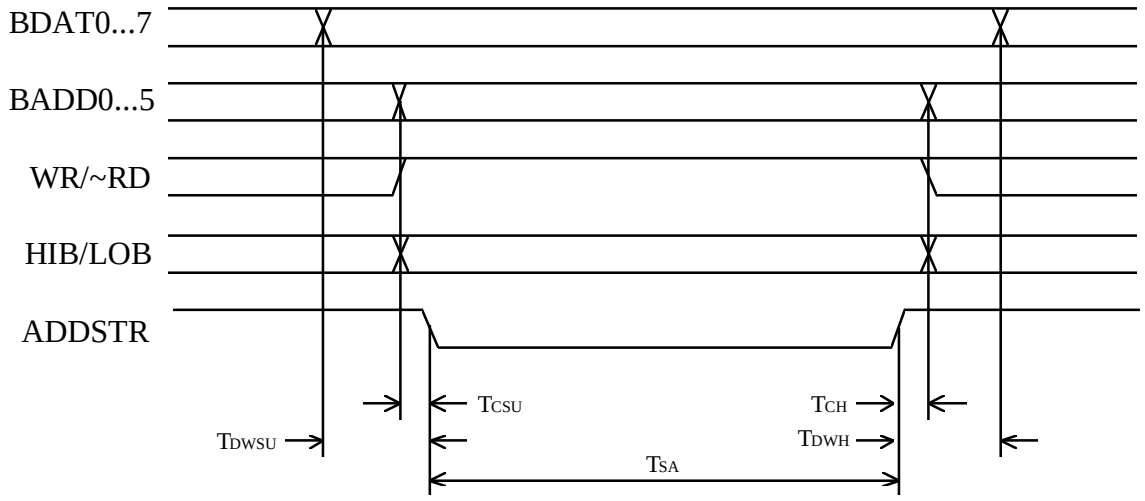
Note this is the Multibeam Correlator Module implementation of this famous bus.

Dataset timing values:

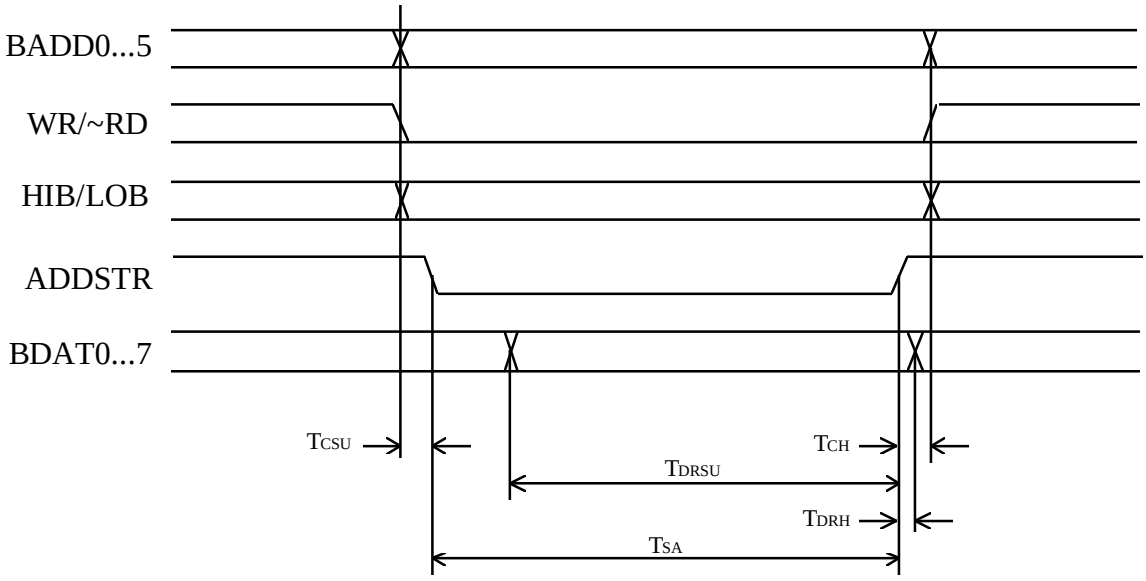
Symbol	Description	Min	Typ	Max	Units
TDWSU	Data write setup	3			T
TCSU	Control signal setup	3			T
TSA	Strobe active	4			T
TSHO	Strobe holdoff	4			T
TCH	Control Hold	1			T
TDWH	Data write hold	1			T
TDRSU	Data read setup	50			nS
TDRH	Data read hold	0			uS

T == On board clock period, eg T = 50ns for 20MHz clock

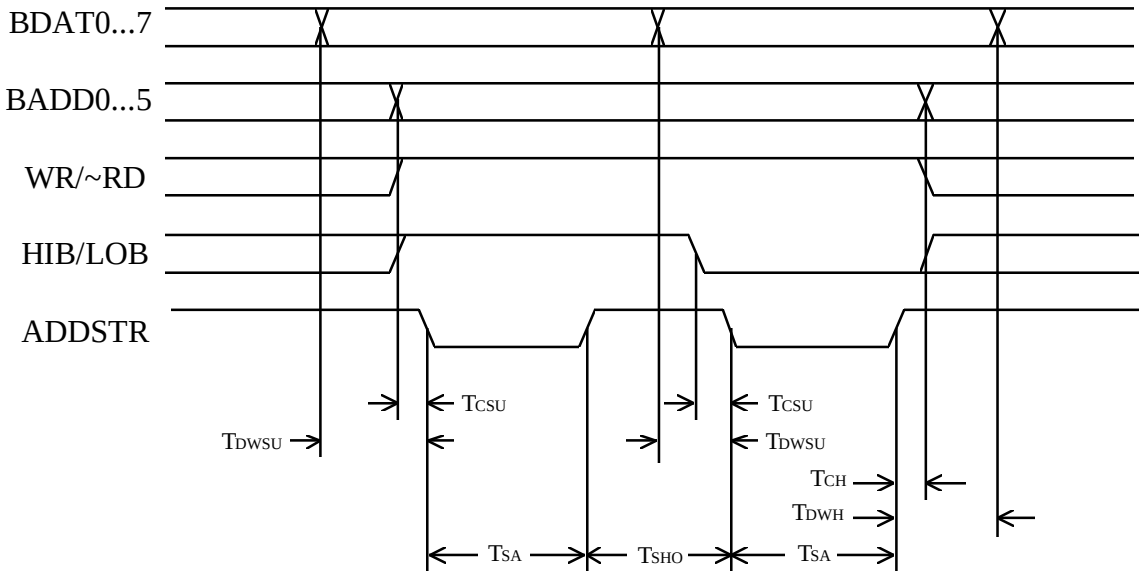
Note: HIB/LOB - when hi access high byte, when LO access low byte.



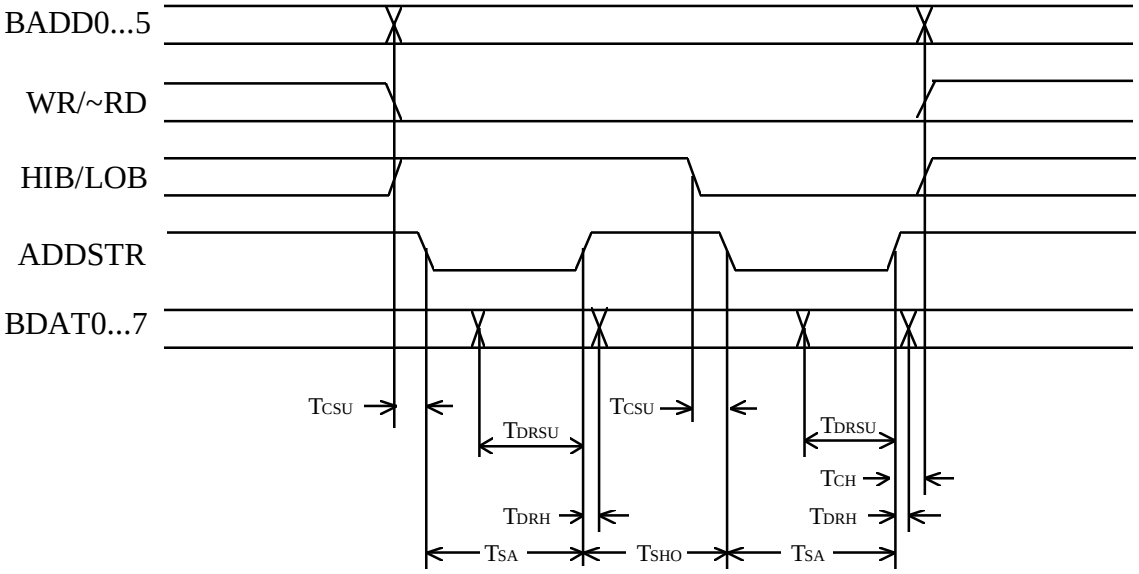
DATASET ADDRESSED 8 BIT WRITE



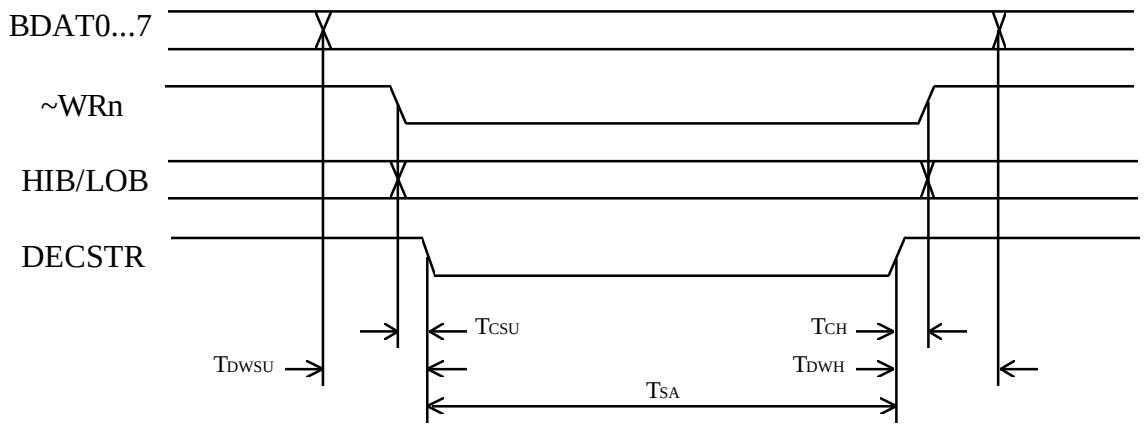
DATASET ADDRESSED 8 BIT READ



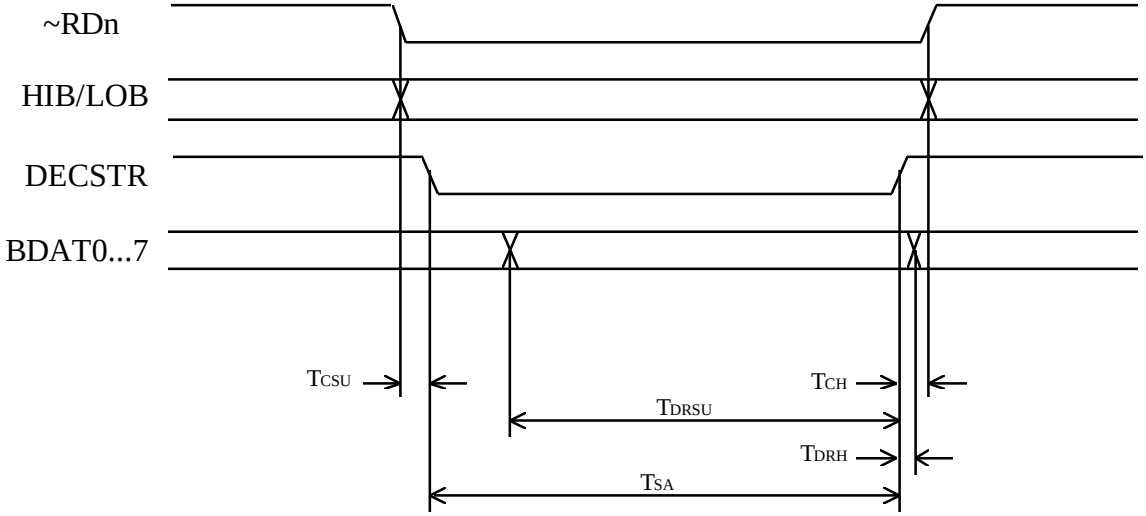
DATASET ADDRESSED 16 BIT WRITE



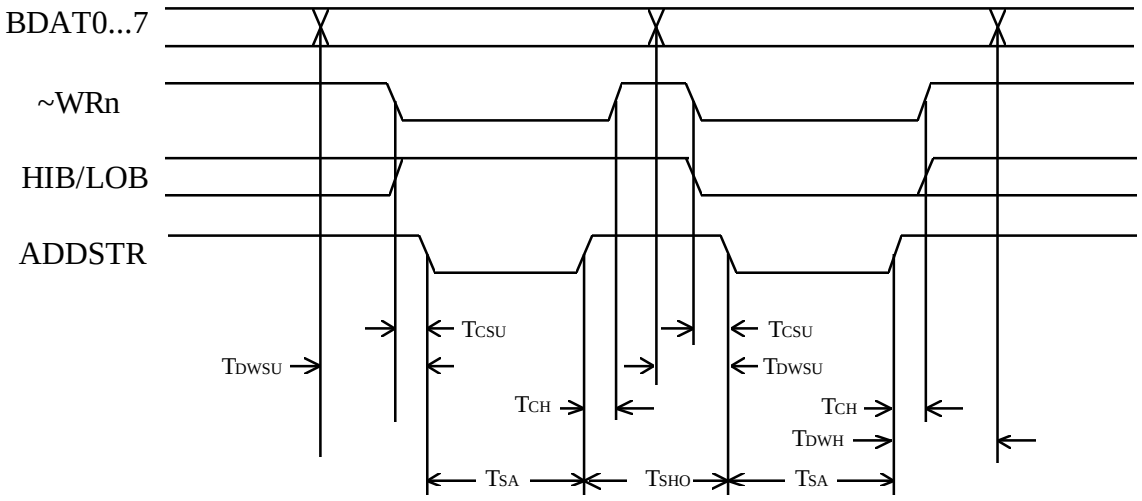
DATASET ADDRESSED 16 BIT READ



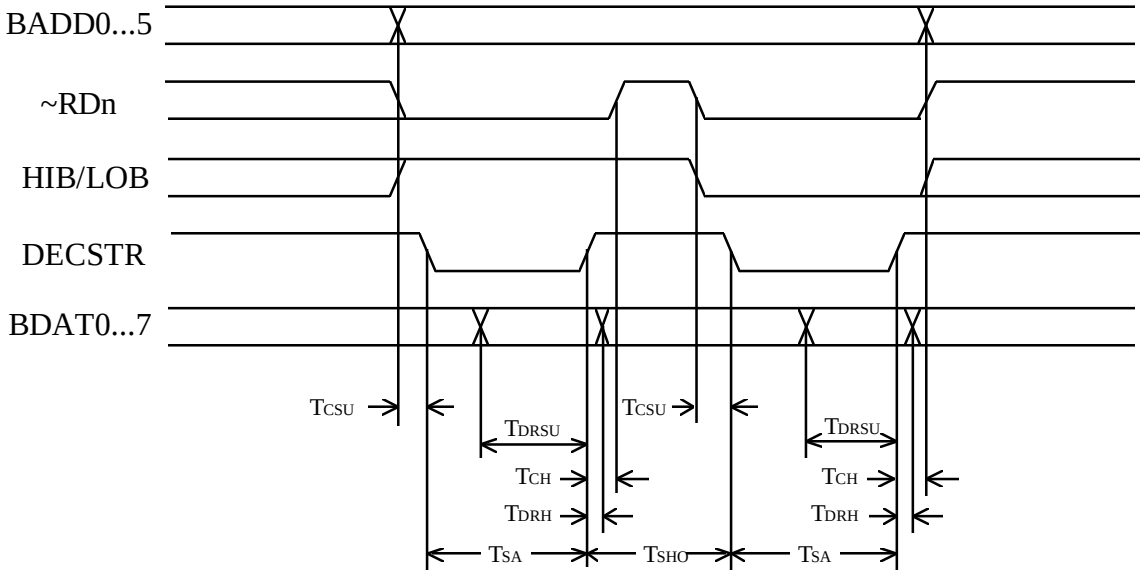
DATASET DECODED 8 BIT WRITE



DATASET DECODED 8 BIT READ



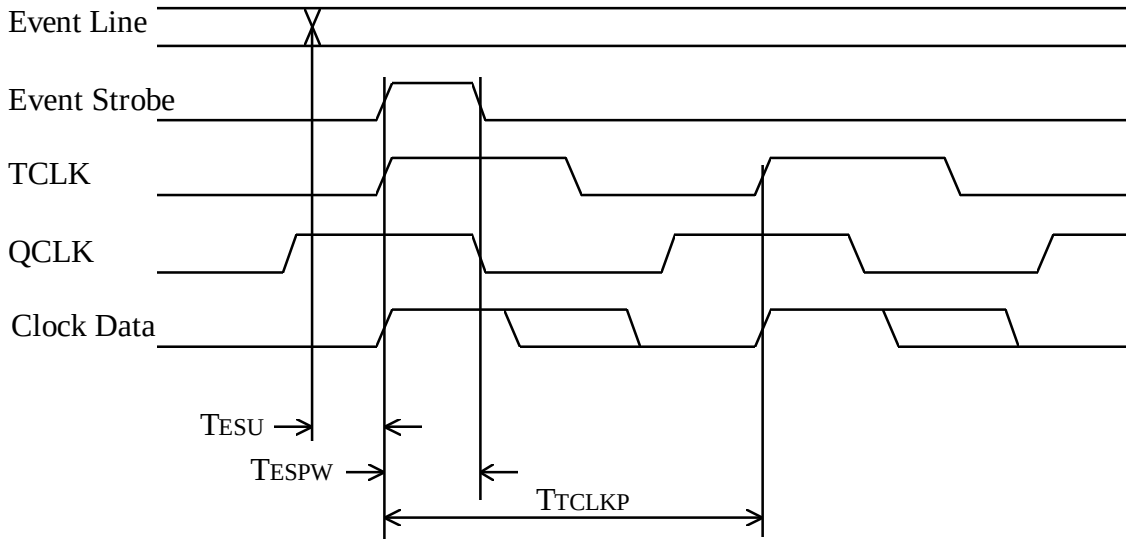
DATASET DECODED 16 BIT WRITE



DATASET DECODED 16 BIT READ

Appendix C - Event Generator Bus Timing.

The information in this section was taken from PC Event Generator manual.



EVENT TIMING

Time	Description	Value	Units
TESU	Event Setup	192	nS
TESPW	Event Strobe Pulse Width	250	nS
TTCLKP	TCLK Period	1000	nS

Appendix D - Power Supply Requirements.

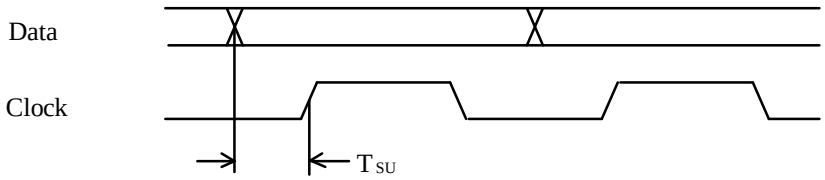
The module power supply current was measured at 3A(+5V) and 0.3A(-5.2V) with all chips installed and the module running at a 128 MHz clock rate.

Suggested +5V power supply = 4.0A / module.

Suggested -5.2V power supply = 0.4A / module.

Appendix E - Data Manipulation Xilinx Timing
(and adjustment of data cables feeding the Correlator).

A guide to the data setup requirements for data signals into the Data Manipulation Xilinx IC with respect to its clock input measured at the IC pin. Device used was a XC3130A-2.



Data Manipulation Xilinx IC - Data Setup Timing

Time	Min	Max	Units
T_{su}	2.6	8.5	nS.

Adjustment of data signal phase with respect to the correlator clock, may be done by changing the length of either. Generally it has been found that it is easier to set the clock signal cable length, and alter the data cable length. When using Spectra-strip Twist ‘n’ Flat #28 guage a propagation delay of around 200mm / nS can be expected. With a nominal cable length, measure the timing of the data signal at the Data Manipulation Xilinx IC, then alter the data cable length to bring the setup time at the IC pins within the desired range.

End