The NRAL Multibeam Correlator System

ATNF Electronics Group

Paul Roberts

1 Introduction

The purpose of this document is to describe at a fairly global level the Multibeam Correlator system as supplied to the Nuffield Radio Astronomy Laboratory. Detailed technical information on each of the systems component parts can be found in the following documents: Multibeam Correlator Module Manual; Multibeam Sampler Manual; Multibeam Block Control Computer Manual.

2 System Architecture

Figure 1 below is a diagram of the major system components and interconnections of the Multibeam correlator.

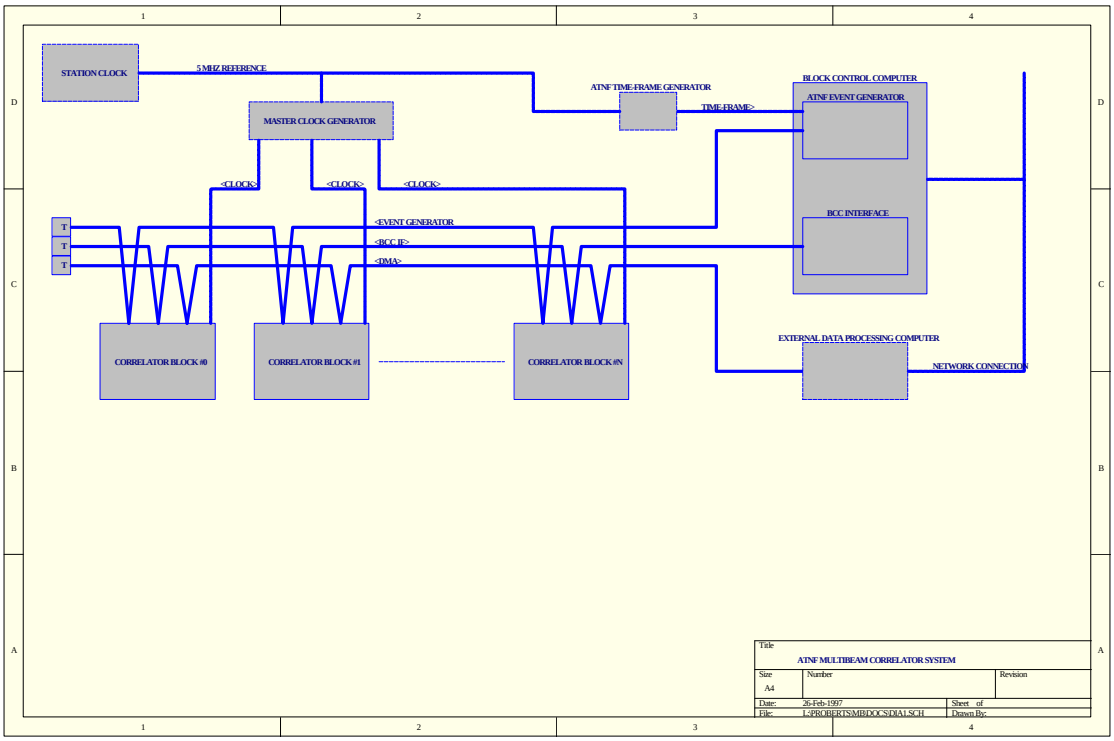


Figure 1. Multibeam System Components

2.1 Station Clock

The station clock is the observatory's fundamental time reference, usually some form of maser standard. The station clock is supplied by NRAL. A 5 MHz signal locked to the station clock is used as a reference for the ATNF time frame generator. Another signal locked to the station clock is required as a reference for the Master Clock Generator.

2.2 ATNF Time Frame Generator

The ATNF Time Frame Generator is a PC based clock which sends serial encoded Binary Atomic Time (BAT), UTC, LMST, MJDC etc out on a RS-422 clock bus (a single twisted pair). The purpose of the Time Frame Generator is to distribute time signals to time dependent equipment within the observatory. In the multibeam system the Time Frame is used by the correlator to precisely control the correlator sequencing to 1µs accuracy. The current generation of the ATNF Time Frame Generator is a set of PC boards which are plugged into a standard 80x86 based computer (80286 or better). This design was produced by the University of Tasmania based on the PDP-11/23 design previously used in the ATNF. The Time Frame Generator requires a 5MHz reference locked to the station clock. An optional 1 Hz tick can also be used for precise phasing of the clock to a known time-of-day tick, e.g. a GPS output. The clock display requires a VT100 compatible serial terminal. ATNF will supply the special purpose PC boards and software. **NRAL will need to supply the PC and serial terminal**.

2.3 Master Clock Generator

The Master Clock Generator provides the fundamental system clock for the correlator modules, nominally 128 MHz , phased locked to the station clock. Each module requires a separate clock connection from the Master Clock Generator. **The Master Clock Generator will be supplied by NRAL**. At its simplest a synthesiser followed by a four way splitter would be sufficient.

2.4 Multibeam Correlator Block

The Multibeam Correlator Block consists of a backplane into which up to 8 correlator module daughterboards may be slotted and 16 sampler modules attached by data cables (two per module). A diagram of the Block connections is illustrated in Figure 2.

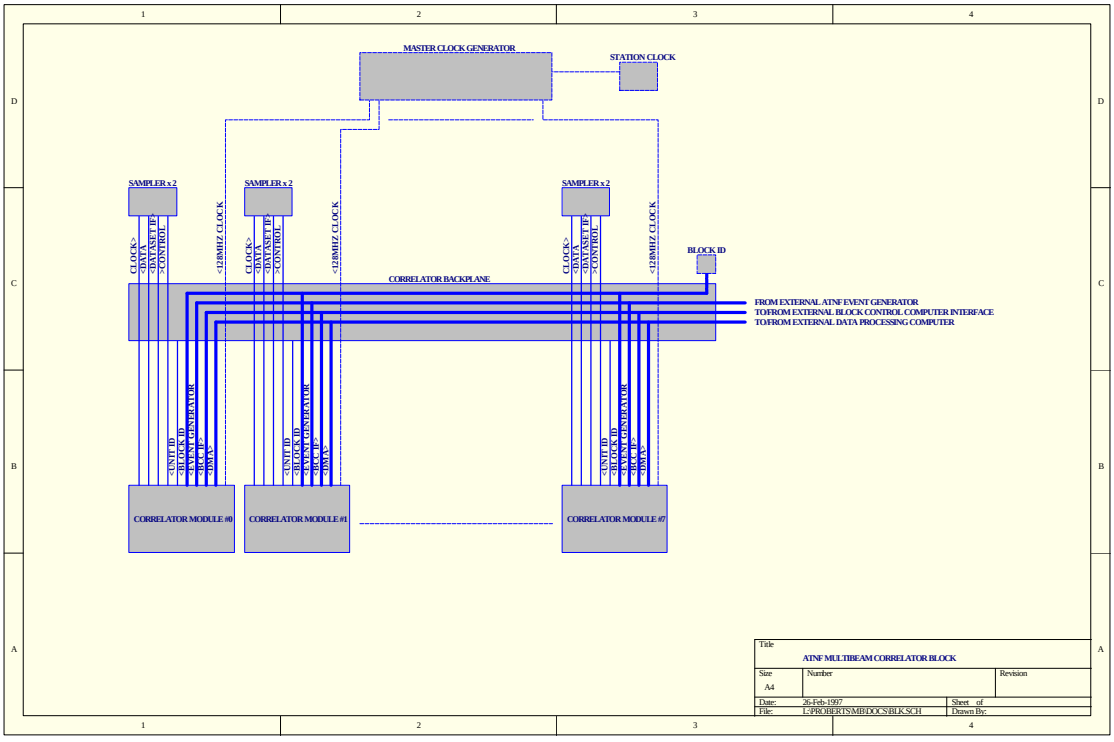


Figure 2. Multibeam Correlator Block.

There are various connections from the backplane to other parts of the system. The 34 pin header labelled “EVENT GENERATOR” is the input for the Event Generator signals. There is a 50 pin header labelled “BCC IF” to which the Multibeam Block Control Computer (MBCC) external bus

interface is connected. The external bus interface is a 16 bit data - 14 bit address parallel data bus used for control of the correlator modules. The 60 pin header and pair of 40 pin headers labelled "DMA I/F" are used for retrieving the correlation data by 32 bit DMA interface from an external control computer. Directly adjacent to each module slot is a 34 pin header labelled "SAMPLER CONTROL" and a 15 pin D connector labelled "SAMPLER DATA". The D connector is where data from two samplers is fed to the module (the 15 pin D connector splits off to two 9 pin D connectors, one for each sampler). The 34 pin header is a simple parallel data bus to the samplers for setting up sampler registers and retrieving total power counts, called the "DATASET" bus after an (in)famous piece of ATNF equipment. Connected by feedthroughs to each correlator module are three RG174 coaxial cables. The uppermost cable supplies the system clock to the module and the two other cables provide the sample clock to each of the attached samplers.

Each Correlator block has an ID, which is the base address of the first module in the block. This is set by a DIP switch on the backplane. The NRAL system will be supplied with a base address of 2000_{16}. Each subsequent module has an address offset by 20_{16}.

2.4.1 Multibeam Sampler

The Multibeam Sampler contains a 2-bit high speed sampler and single channel total power detector. The 2 bit sampler is capable of sampling at up to 256 Msamples/s with 128 Msamples/s the maximum Multibeam rate. The input frequency response extends to 300 MHz allowing any band within this range to be digitised. The threshold levels are maintained by a PLL technique and set at the optimum for a 3 level correlator. The nominal input power requirement is -27dBm @ 64 MHz bandwidth.

The total power detector portion of the sampler uses a back-diode square law detector followed by a V/F converter to give an output frequency proportional to the total power. Two on-board counters count the number of counts during the low and high periods of an external signal called SYNC. In normal operation a noise diode is switched into the receiver path synchronously with the SYNC signal. Comparison of the two counts and a knowledge of the diode noise power allows the system temperature to be found.

The sampler sample clock arrives on a coaxial input from the correlator. The IF arrives on another coaxial input and the total power counts are retrieved over the 34 pin dataset interface. The SYNC and
BLANK dynamic control signals also enter on the dataset interface cable. Sampled data returns to the correlator on the 9 pin D connector.

For detailed information see the Multibeam Sampler Manual.

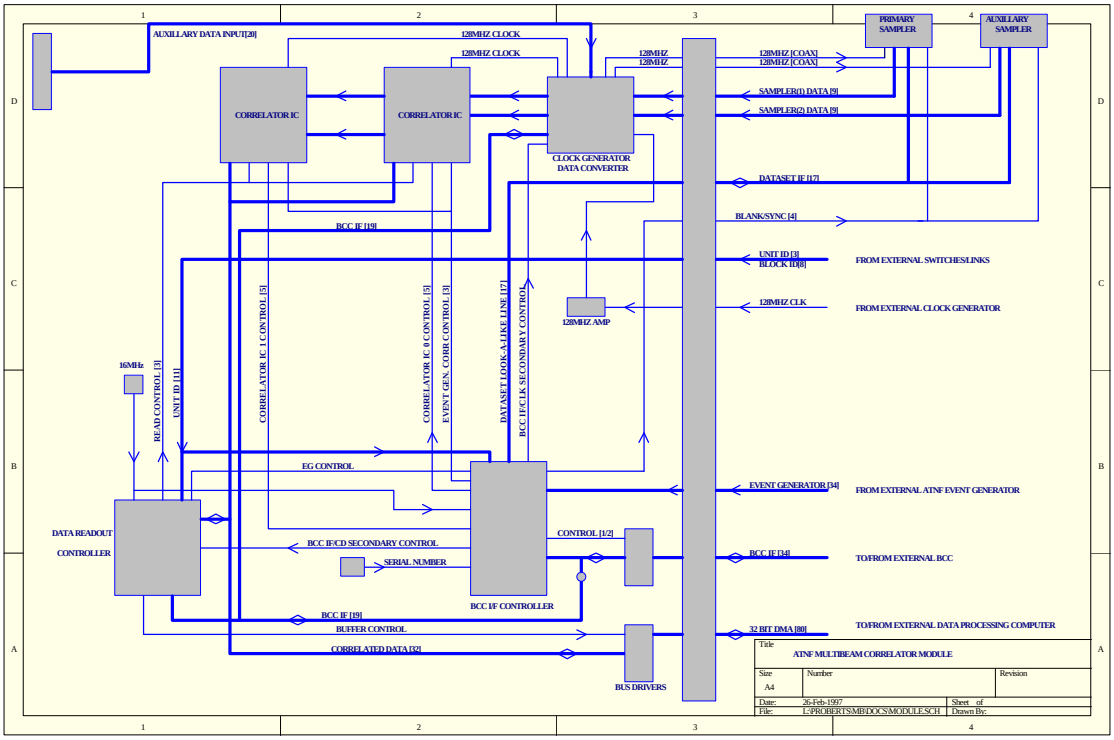
2.4.2 Multibeam Correlator Module

The Multibeam Correlator Module is based around 2 NASA SERC 1024 lag correlator chips. The maximum clock rate of the module is 128 MHz (64 MHz signal bandwidth). The module can be configured in three modes: 1) Two independent 1024 lag autocorrelators 2) One 2048 lag autocorrelator or 3) One 2048 lag (-1024 .. 1024) cross correlator. The usual data source for the module is two multibeam samplers. There is also an auxiliary data input port on the front of the module where data from other sources (e.g. the LBA-DAS under development at the ATNF) can be introduced to the module. Figure 3 gives a diagram of the Multibeam Correlator Module.

The module has a maximum integration time of 16.77 seconds at 128 Ms/s, doubling with each halving of the sampler rate. The result of the correlation is available as 1025 32-bit numbers, comprising the 1024 lag values and one sample count. The correlation result can be retrieved by DMA transfer or by the BCC bus. The output data rate is approximately one 32 bit word / 100ns by DMA or 2x16bit words/1us via the BCC.

All dynamic control of the module is provided by an ATNF Event Generator which produces events to start and stop the correlation cycles and a host of other activities.

For detailed information see the Multibeam Correlator Module Manual.



2.5 Multibeam Block Control Computer

The Multibeam Block Control Computer (MBCC) is an 80486 based computer running special purpose software written by the ATNF, under the pSOS real-time operating system. It provides for control, configuration and data retrieval for the correlator modules and the samplers. The MBCC can be considered the application programmers interface (API) to the correlator system. Once the necessary hardware connections have been made the correlator system is run and data retrieved solely by sending
appropriate commands to the MBCC. Communication with the MBCC is generally by network connections utilising the socket paradigm. A limited amount of control and monitoring is also possible using a serial connection. For full details see the Multibeam Block Control Computer Manual.

2.5.1 MBCC Hardware

The MBCC consists of the following PC boards which are inserted in a five slot 16-bit ISA bus passive backplane: 1) 80486 CPU Card 2) SMC8013 Ethernet card 3) ATNF Event Generator 4) ATNF External Bus Interface. An ATNF IDENT board is also attached to the External bus.

2.5.1.1 ATNF Event Generator

The Event Generator is a custom hardware device designed and built at the ATNF. It can generate up to 16 timing signals and a clocking signal. It includes a frame grabber used to obtain information from the ATNF Time Frame Generator. To control the event generator's timing signals an Event Timing Description (ETD) is used. An ETD is a recursive data structure which defines a stream of events for the event generator. An ETD acts like a program which is followed to generate

the data (time and events) to send to the event generator. It consists of the ETD commands listed in the Multibeam Block Control Computer Manual.

2.5.1.2 ATNF External Bus Interface

The External Bus Interface is a custom hardware device designed and built at the ATNF. It provides three 16 data bit - 14 address bit external parallel buses. It addresses 32K by 16 bit words and six specific purpose external registers on each bus.

2.5.1.3 ATNF Ident Board

The ATNF Ident board allows the MBCC to assign itself an IP address. On boot-up the MBCC reads the value of the DIP switch on the Ident board and uses this as an index into an internal table in the software to assign itself an IP address. The correct setting for the DIP switch for the NRAL system is $E0_{16}$. This comprises a site ID of 7 for Jodrell and a block number of 0. See the Block Control Computer Identity Board documentation for details.

2.5.2 MBCC Software

The ATNF has developed special purpose software, for the control and configuration of AT correlator hardware, which runs on the MBCC. The MBCC software is capable of controlling all types of AT correlators not just the Multibeam. The subset of the full Block Control Computer command language as used in the Multibeam has been compiled in the document Multibeam Block Control Computer Manual and should be consulted for reference. MBCC commands consist of the character '.' followed by a two letter command code and a variable number of command arguments. For instance the command -
.pm 6100 10202 a0000 ,
programs registers 1 and a on the multibeam module located at address 6100 with the values 0202 and 0000 respectively.

3 Data Retrieval

The Multibeam Correlator supports two methods for retrieving the correlated data from the correlator modules, namely by external DMA transfer or over the network connection.

3.1 DMA Transfer

The normal mode of data retrieval with ATNF correlators is by DMA transfer. The DMA bus is an external 32 bit data bus which connects from the correlator modules as slaves to a special purpose ATNF interface board as master. The interface board plugs into the Turbo Channel interface on a DEC Alpha (or an older version connects to the Qbus on a MicroVax). An event produced by the MBCC Event Generator triggers the master (the Alpha) to initiate a DMA transfer of the correlated data. Data transfer is at the rate of approximately one 32 bit word per 100ns.

3.2 Network Transfer

As external users of the Multibeam Correlator are unlikely to have an Alpha with Turbo Channel interface available an alternative method has been provided whereby the correlated data is

read from the modules by the MBCC and sent to the control computer in response to a **.gc** command. The data is read from the modules at a rate of approximately one 16 bit word per us. Transmission time from the MBCC to the control computer depends on network traffic and availability of buffers at the sending and receiving ends. 4100 bytes of data must be transferred for each correlator chip.

3.3 Other Options

The controller which handles DMA transfers on the correlator module is implemented in a Xilinx FPGA design which is downloadable from the control computer. Thus the option exists of using a commercial plug-in parallel interface card in the control computer and redesigning the DMA controller for a new protocol.

It may also be convenient to buy a second hand Alpha with Turbo Channel interface. This would have the added advantage of allowing use of the Correlator Control Computer software developed at the ATNF over many years saving a lot of control computer software development time.

4 Running the Correlator

This section describes what is necessary to setup and run the Multibeam Correlator. The tasks described are the responsibility of the Correlator Control Computer (CCC). The CCC is a workstation (PC, Sun, Alpha etc) which sends the appropriate sequence of commands to setup, cycle and collect data from the correlator. The CCC then does Fourier transforming, archiving, displaying etc. **NRAL will provide their own CCC to control the Multibeam**. ATNF will supply a simple CCC program called “Simple CCC” which will run the correlator, display the correlations and amplitudes and save the data to file. Simple CCC is a C program compiled using Borland C++ 4.5 and runs under Windows NT on a PC. This program has been written as an example of what is required to run the correlator and to test the correlator following installation.

To run the correlator the following steps are needed:
1) Load an Event Timing Description.
2) Download on-board reconfigurable logic (Xilinx chip).
3) Program the Multibeam Correlator Module registers.
4) Initialise the total power acquisition task.
5) Cycle the correlator.

4.1 Load Event Timing Description

The correlator needs several events to run. The description of these events - when they should occur, for how long and on which signal line - is contained in a text file called an Event Timing Description (ETD) as explained in section 2.5.1.1. For example the following is an ETD for a 5 second integration period with the Multibeam.

```
O 6bd
A 7ffd
E 3e8 $0
A fff7
E 438 $0
S 3e8 2 3df 1388
X 84
E 1388 $0
O a
A fdde
X 80
```

```
E 4bb2e8 $0
X 4
E 4bb2ed $0
O 20
X 4
E 4bb2f2 $0
S 4bb2f2 2 2 5
X 4
E 5 $0
O 8200
E 4bbf04 $0
A 7fff
E 4bbf18 $0
S 4bb2e8 2 7 1388
X 80
E 1388 $0
```

ATNF will supply NRAL with ETDs for common modes of the correlator. If NRAL requires additional modes they can either contact us to generate new ETDs to their requirements or write their own. The definition of events and the lines on which they occur are given below in Table 1. If users intend to write new ETDs they should maintain the same definitions and bit allocations.

Event Generator Name, Bit and Sense Allocation.
File Name: mbtp (1 of 2)

interrupt	C0	8001 (hex)	(MSB 1000000000000001 LSB)	S0 +
marker	C1	0800 (hex)	(MSB 0000100000000000 LSB)	S1 +
blank	C2	0008 (hex)	(MSB 0000000000001000 LSB)	S2 +
shift	C3	0010 (hex)	(MSB 0000000000010000 LSB)	S3 +
integrate	C4	0020 (hex)	(MSB 0000000000100000 LSB)	S4 +
ncal	C5	0080 (hex)	(MSB 0000000010000000 LSB)	S5 +
sam_blank	C6	0002 (hex)	(MSB 0000000000000010 LSB)	S6 +
sam_sync	C7	0004 (hex)	(MSB 0000000000000100 LSB)	S7 +
sam_data_ready	C8	0200 (hex)	(MSB 0000001000000000 LSB)	S8 +
sam_cycle_end	C9	0400 (hex)	(MSB 0000010000000000 LSB)	S9 +
-- No Entry --				
-- No Entry --				
-- No Entry --				
-- No Entry --				
-- No Entry --				
-- No Entry --				

Keywords: help
Type two letter code, space then desired value then <RET>
When through <RET>

Table 1. Multibeam event names and bit allocations. Taken from config event menu.

4.1.1 Event Description

Interrupt. This is the event which signals the DMA controller to start transferring the correlation data over the DMA bus. This signal is not used in the NRAL system where data retrieval is via the network connection.

Marker. This is a visual debugging signal which marks the beginning of an integration cycle. It is not required for correlator operation.

Blank. This is the correlator chip BLANK signal (see NASA SERC correlator chip documentation). When BLANK is high the correlator chip ignores input data.

Shift. This is the correlator chip SE signal. When SE is high data is shifted through the internal delay line.

Integrate. This is the correlator chip INT signal. INT is the integration period framing signal. On bringing INT low the integrated data is dumped into the output registers and a new integration can begin by bringing INT high.

Ncal. This is the noise diode switching signal.

Sam_blank. This is the sampler BLANK signal. The leading edge of BLANK clears the total power counters and the current contents of the counters are transferred to the output registers. Further counting is inhibited whilst BLANK is high.

Sam_sync. This is the sampler SYNC signal. When SYNC is high the on counter is incremented. When SYNC is low the off counter is incremented. The leading edge of SYNC is also used to clock data through the sampler logic during the BLANK period.

Sam_data_ready. This event marks the end of a total power acquisition cycle. The accumulated total power counts are transferred to an output buffer ready to be retrieved with a .gp command.

Detailed constraints regarding the timing relationships between events, their duration and sequence etc can be provided if needed.

4.2 Download On-board Configurable Logic

For maximum flexibility the data distributor/formatter FPGA and the DMA controller FPGA have been made downloadable. The NRAL multibeam has been shipped with the DMA controller programmed from on-board PROM so only the data distributor/formatter FPGA need be downloaded. This is accomplished with the .dx command. The correct file to download is ddd64.xil. This design allows autocorrelations and crosscorrelations up to 64MHz bandwidth with the data source being the two attached samplers. If users wish to create their own additional designs a utility, rbt2xil.exe, is available which takes the .rbt file produced by the Xilinx software and compresses it into the .xil format required by the .dx command.

4.3 Program Multibeam Registers

There are several registers on the Multibeam module that have to be set for correct operation. See the Multibeam Module Manual and the example software for details. Programming the registers is accomplished with the .pm command.

4.4 Initialise Total Power Task

In order for total power results to be read the total power acquisition task must be initialised and told from which samplers to collect total power readings. This is accomplished with the .mi command.

4.5 Cycle the Correlator

The correlator is cycled by issuing a .ee command. The specified ETD will be executed at the specified start time. One execution of the ETD generally corresponds to one integration period. For a continuous uninterrupted sequence of integration periods the control computer needs to issue a new .ee command before the previous ETD has completed and with a start time equal to the time at which the previous ETD completes. Somewhere within the integration cycle the control computer has to retrieve the correlation data and total power counts collected during the previous integration, with the .gc and .gp commands respectively.