C.S.I.R.O Australia Telescope National Facility

Australia Telescope Electronics Group

S6 Multi Beam Sampler

Manual

Contents

Drawing List

Mechanical Drawings

Drawing Number	Name	Drawn By	Date
S06/014/01	Multi Beam Sampler Box	W Preston	8/8/94
	Mod C	P Sharp	5/9/96
S06/014/02	Multi Beam Cover & Base Plate Detail	W Preston	17/8/94

Electrical Drawings

Protel Schematic Capture Files

File Name	Description	Drawn By
Ateg2:\usr2\users\mwilling\pfw-sch\multisam\samecl.sch	ECL p.c.b schematic	M Willing
Ateg2:\usr2\users\mwilling\pfw-sch\multisam\samlin.sch	Linear p.c.b schematic	M Willing
Ateg2:\usr2\users\mwilling\pfw-sch\multisam\sampwr.sch	Total Power p.c.b schematic	M Willing

Protel PCB Files

File Name	Description	Drawn By
Ateg2:\usr2\users\mwilling\pfw-pcb\multisam \samecl\ecl.pcb	ECL pcb file	M Willing
Ateg2:\usr2\users\mwilling\pfw-pcb\multisam \samlin\samlin.pcb	Linear pcb file	M Willing
Ateg2:\usr2\users\mwilling\pfw-pcb\multisam \sampwr\sampwr.pcb	Total Power pcb file	M Willing

Xilinx Protel Schematic Capture Files

Parkes Muli Beam Sampler Prom “3lev1212.mcs”

File Name	Description	Drawn By
Ateg2:\usr2\users\mbeam\s6\elec\xilinx\3levParkes\sch \multisam.sch	Schematic Sh 1 of 13	M Leach
\decode	Schematic Sh 2 of 13	M Leach
\Tp-div	Schematic Sh 3 of 13	M Leach
\Divide00	Schematic Sh 4 of 13	M Leach
\Divide01	Schematic Sh 5 of 13	M Leach
\Reg0	Schematic Sh 6 of 13	M Leach
\Reg1	Schematic Sh 7 of 13	M Leach
\Phase	Schematic Sh 8 of 13	M Leach
\Phasdiv	Schematic Sh 9 of 13	M Leach
\Ph-comp0	Schematic Sh 10 of 13	M Leach
\Ph-comp1	Schematic Sh 11 of 13	M Leach
\Ph-comp2	Schematic Sh 12 of 13	M Leach
\Monitor	Schematic Sh 13 of 13	M Leach

Xilinx File

Ateg2:\usr2\users\mbeam\s6\elec\xilinx\3levParkes\lca\3levsam.lca	LCA file
Ateg2:\usr2\users\ mbeam\s6\elec\xilinx\3levParkes\bit\3lv1212b.mcs	Program file.

Muli Beam Sampler Prom with Programmable clock“3lechclk.mcs”

File Name	Description	Drawn By
Ateg2:\usr2\users\mbeam\s6\elec\xilinx\3levprog\DRAW		
\multisam.sch	Schematic Sh 1 of 13	M Leach
\decode	Schematic Sh 2 of 13	M Leach
\Tp-div	Schematic Sh 3 of 13	M Leach
\Divide00	Schematic Sh 4 of 13	M Leach
\Divide01	Schematic Sh 5 of 13	M Leach
\Reg0	Schematic Sh 6 of 13	M Leach
\Reg1	Schematic Sh 7 of 13	M Leach
\Phase	Schematic Sh 8 of 13	M Leach
\Phasdiv	Schematic Sh 9 of 13	M Leach
\Ph-comp0	Schematic Sh 10 of 13	M Leach
\Ph-comp1	Schematic Sh 11 of 13	M Leach
\Ph-comp2	Schematic Sh 12 of 13	M Leach
\Monitor	Schematic Sh 13 of 13	M Leach

Xilinx File

Ateg2:\usr2\users\mbeam\s6\elec\xilinx\3levprog\xnf\3levsam.lca	LCA file
Ateg2:\usr2\users\ mbeam\s6\elec\xilinx\3levprog\xnf\3levhclk.mcs	Program file.

This docuement: MSWord application

Ateg2:\usr2\users\mbeam\s6\doc\msamdoc.doc

Sampler Overview

Each Sampler module contains a 2 Bit high speed Sampler and a single channel Total Power Detector.

The 2 Bit Sampler is capable of a 128 to 8MSample/Sec[1] range of sampling rate. The Parkes Multi Beam correlator uses a 128MSample/sec rate. The frequency response of the input amplifiers and comparators extends beyond 300MHz, allowing use of upper and lower IF side bands. The side band used for the Parkes Multi Beam project extends from 128MHz to 192MHz.

Threshold levels for the 2 Bit Sampler are automatically determined by a phase lock loop technique. Threshold levels are set for optimal 3 level sampling signal to noise performance. The sampler can be optimised for four level sampling by replacing the programming prom.

The Total Power Detector uses a digital synchronous detection scheme. An external noise source coupled into the RF provides reference level calibration.

The Multi Beam Sampler is mounted in an RF shielded enclosure, the sample clock and IF input connections are made by SMA connectors on the front of the module. DC power, BLANK and SYNC connections are made via a 15 pin male D connector. The Data set interface connection is a 25 pin male D and the Sampled IF output is a 9 pin male D connector.

Module electronics are mounted on three separate printed circuit boards.

The Total Power pcb process the incoming IF signal and outputs a frequency proportional to input power level. The Total Power pcb also produces an out amplified IF output which is normally used to drive the ECL pcb.

The E.C.L pcb contains IF amplification, the 2 bit Sampler and phase lock loop statistic prescalers.

The Linear pcb implements three phase lock loop filters and power supply regulators. A Xilinx device on this pcb contains second stage statistic dividers, phase comparators and the total power detector accumulators. The Xilinx device is controlled by the data set interface.

2 Bit Sampler

[1] Sample rate programming is available with the programming prom ‘3levhclk’. Other Proms require the use of a 128MSample/sec sample clock.

An RF amplifier on the Total Power pcb provides 12 dB of gain on the IF input. A 10dB coupler and 3dB pad isolate the detector diode. The direct path of the coupler is attenuated by 3dB and taken off the pcb. This output is generally used to drive the ECL pcb.

The input IF is amplified by MP1 on the ECL pcb. This device has a -1dB compression power level of +27dBm, maximum noise power at the IF input should not exceed +3dBm.

The nominal input noise power level to the ECL pcb is -15dBm. When the Total Power pcb IF output is used to drive the ECL pcb nominal input total noise power should be -27dBm.

Table 1: Noise Input Power Levels

Noise BW	4MHz	8MHz	16MHz	32MHz	64MHz
Total Power dBm	-27	-27	-27	-27	-27
Power/Hz dBm/Hz	-93	-96	-99	-102	-105

The Sampler uses fast dual comparators, AD96687, to convert the IF into 2 bit four level balanced ECL signals. The multi beam correlator which is a “3 level correlator”, encodes the sampler signal to a three level.

The ‘sign’ or ‘offset’ comparator, U1B has threshold level near ground. Comparator output is low for all IF samples greater than ground. Samples are synchronised to the sample clock by internal latches.

Comparator U1A, is the positive level comparator. The output of this comparator is high for the 26.95% of samples above the U1A threshold level. Similarly the negative comparator, U2A output is high for 26.95% of samples with amplitude less than the negative level threshold. The output of the positive and negative comparators are ORed together to give the ‘Magnitude’ bit. Sampler levels, are optimised for maximum signal noise ratio.

Table 2: Truth table for Sampler and “Three Level” Data Bits.

Input Level	**Sampler Sign Bit**	**Sampler Mag. Bit**	**3 Level Sign Bit**	**3 Level Mag. Bit**
Above + Level	**0**	**1**	**0**	**1**
Above 0 below + Level	**0**	**0**	**0**	**0**
Below 0 below - Level	**1**	**0**	**0**	**0**
Below 0 below - Level	**1**	**1**	**1**	**1**

The sample clock input is converted to an ECL signal by a fourth comparator, U2B. The ecl level sample clock is distributed by buffers in U3. The comparator outputs are

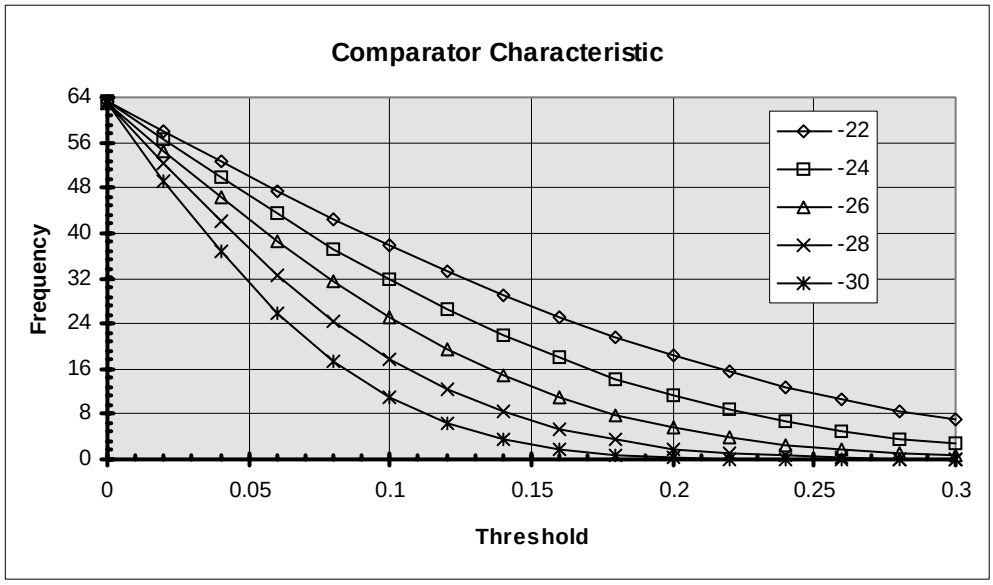
latched internally by the sample clock and then are re-synchronised to the clock by three D latches in U4.

Comparator outputs are synchronised to the sample clock and divided by two in U4 data latches. The sample clock and comparator outputs are further prescaled by a divide by 16 counters, U6,U7,U8 and U9. The signals are converted to single ended TTL by U10 and passed via feed throughs to the linear pcb.

Each comparator threshold level is controlled by a separate phase locked loop. The comparators behave in a similar fashion to a VCO. With a threshold hold of 0 volts, half of all samples will be high, corresponding to an output frequency half the sample clock. With increasing threshold level the comparator output frequency decreases.

Fig 1 shows a typical comparator characteristic. The characteristic was measured with a 128MHz sample clock. A 64MHz bandpass filter, centre frequency 96MHz, was used to limit noise bandwidth. Noise power level was adjusted for each curve by a variable attenuator. The threshold voltage was adjusted by a linear supply.

Fig 1:



The Xilinx device contains four dividers and three phase detectors[2]. The output of each divider is connected to a test point on the Linear pcb. The clock frequency is used as the reference frequency for each phase detector. The division ratios for each statistic and frequencies at relevant test points are set out in the table 2 below. Division ratios are selected to ensure that the optimal signal to noise ratio is maintained.

Lower noise input bandwidths can be selected by using programmable statistic dividers in the Xilinx device and changing sample clock frequency. The

[2] The Xilinx phase detector is based on the Motorola MC4044. The phase detector locks the VCO in phase with the reference frequency. There are two output ports from this phase detector, each drive a dual pole low pass filter. See attached data sheets.

programmable dividers are capable of a 1 to 16 division ratio. Division rates and sample statistics are set out in table 3.

Table 3: PLL Test point Data when Locked With 128MHz Clock

Signal	**Test Point**	**Frequency**	**Division Ratio**	**% of Samples**
Sample Clock	CLK Out	8MHz	32	100%
Sample Clock	DIV-CK	976Hz	32*8192	100%
O/S Statistic	OSTAT	64MHz	1	50%
O/S Statistic	O/S OUT	4MHz	16	50%
O/S Statistic	DIV-0	976Hz	16*4096	50%
POS Statistic	POSTAT	34.496MHz	1	26.95%
POS Statistic	POS OUT	2.156MHz	16	26.95%
POS Statistic	DIV-P	976Hz	16*2208	26.95%
NEG Statistic	NEGTAT	34.496MHz	1	26.95%
NEG Statistic	NEG OUT	2.156MHz	16	26.95%
NEG Statistic	DIV-N	976Hz	16*2208	26.95%

Table 4: Sampler Programmable P.L.L divisor ratios and Sampler Statistics.

Sample Clock	Noise BW	Mag Division	Sign Divisor	Statistics
128MHz	64MHz	16 * 2208	16 * 4096	53.906%
64MHz	32MHz	16 * 1104	16 * 2048	53.906%
32MHz	16MHz	16 * 560	16 * 1024	54.688%
16MHz	8MHz	16 * 272	16 * 512	53.125%
8MHz	4MHz	16 * 144	16 * 256	56.250%

Outputs from each phase detector drive a balanced, dual pole low pass filter. Each phase detector acts to lock the reference and VCO signal in phase. The output of the positive and negative loop filters each drive an unity inverting amplifier. A resistive divider by 12 is used to reduce VCO gain. The unity gain buffer saturates when input levels approach -20dBm, resulting in statistic lock failure.

Two loop lock indicators are implemented in the Xilinx device. An out of lock indication occurs when the divided ‘VCO’ output is out of phase with the reference. The indicator are latched into a register if phase lock is lost on any reference cycle. The latches are cleared every BLANK. There is an indicator for the Sign and the Ored output of the Magnitude Loops.

The Zero loop output filter drives an inverting buffer amplifier. A resistive divide by 24 is used to reduce VCO gain.

With the nominal input noise power, the positive threshold should be approximately +100mV. The negative threshold level should be around -100mV and the zero threshold level should be approximately 0 Volts.

Total Power Detector

Overview

The total power detector uses a synchronous detection scheme to measure noise power of the IF signal.

A calibrated noise signal is coupled into the RF input of the receiver. The noise signal is switched ON and OFF by a synchronising signal called SYNC.

IF noise power is detected by a back diode, and amplified on the Total Power PCB. The amplifier DC output drives a voltage to frequency converter, which has a 1V/1MHz characteristic.

When SYNC is OFF, frequency output from the Total Power pcb increments the Off counter. When SYNC is ON, the On counter is incremented. Since the excess noise power is well known the difference between the ON and OFF counts allows the IF total power to be determined. The BLANK signal is used to reset counters and load counter registers and determines the length of the integration time.

Implementation

The incoming IF is amplified by A1 passed through a 10dB coupler and a 3dB pad and routed to the ECL pcb. The coupled output is attenuated by 3dB, the RF level is converted to a d.c voltage by back diode D1. Two stages of DC gain with approximately 30dB each follow.

With a -27dBm noise power input the output of the d.c amp should be about one volt. D.C amplifier output drives U1, a voltage to frequency converter with a 1V/MHz characteristic. If the d.c level is too large (around 3V) to U1, the device output saturates at a logic high level. NOTE The V to F characteristic is increasingly non linear for d.c inputs greater than one volt.

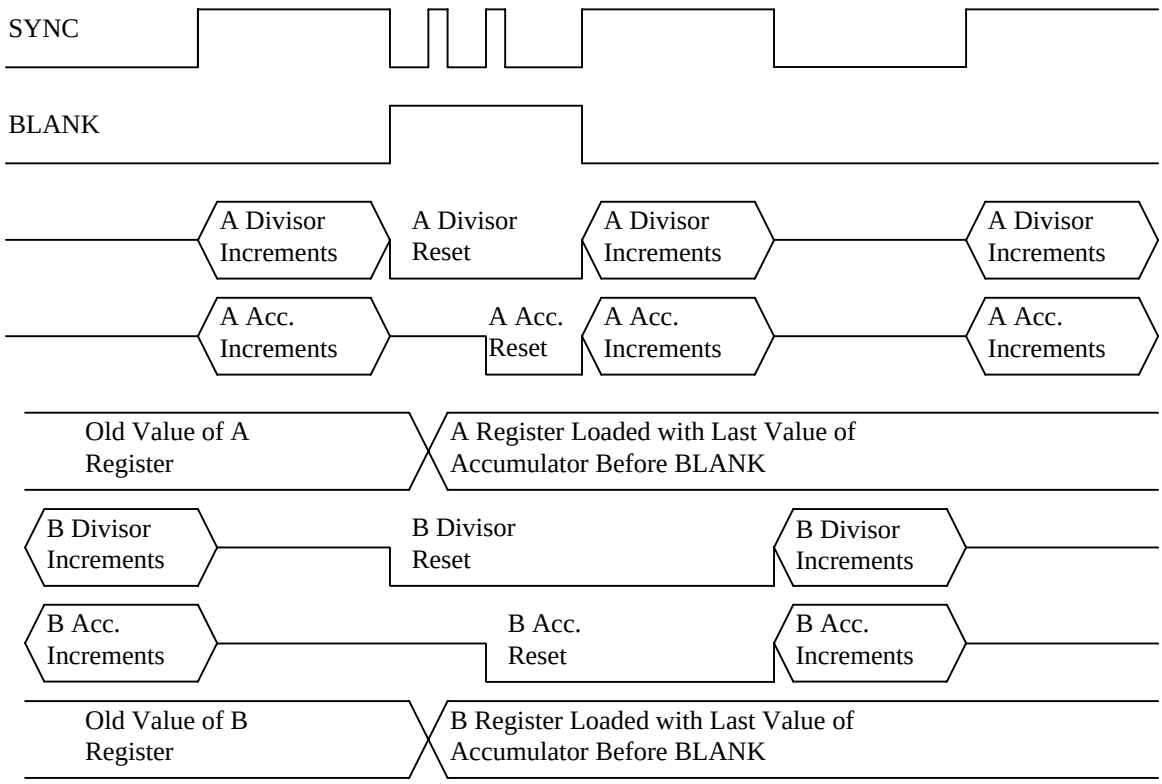
Output from U1 is input to the Xilinx device on the linear pcb.

Two programmable dividers are implemented in the Xilinx device. Each divider is programmed by the 6LSBs of base register of the Dataset interface. The 5 LSBs are used to set the division ratio to a value equal to 5 LSBs + 1. The 6th bit if set multiplies the divisor ratio by 2. Each divisor is only enabled by the appropriate state of SYNC.

Terminal count output from each programmable counter is accumulated in a 16 bit counter. Each accumulator is limited to a maximum count of 61441. Output from each 16 bit counter is stored in a 16 bit register.

The dividers stop counting when BLANK is set. A sequence of two SYNC pulses are required to properly load and clear the accumulators. The first SYNC pulse loads the old count into the registers. The second SYNC pulse clears the accumulators.

Figure 2: Total Power Timing Diagram



Data Set Interface

The Data Set Interface is based on the A.T standard Dataset Interface and is used to control and monitor the Total Power Detector.

Base addressing for each module is set by 4 bit DIP (Q5-Q2) switch on the back of the Sampler module backplane. One Data Set interface can control up to control 16 sampler modules.

There are two loop lock bits. The magnitude and sign lock bits indicate whether the sampler statistics are locked. A high indicates lock, low output indicates the not

locked condition. A lock in indication on the sign bit and unlock on magnitude indicates low input power.

The 6LSBs of the total power register are used to set the programmable dividers. The 6th bit controls the divide by 2 prescaler.

The 6 LSBs of the total power register can be read back. The MSB is the Sampler Statistic Sign Lock Indicator the next MSB is the Sampler Statistic Mag Lock Indicator. The magnitude and sign lock bits indicate whether the sampler statistics are locked. A high indicates lock, low output indicates the not locked condition. A lock in indication on the sign bit and unlock on magnitude indicates low input power.

The sample rate is controlled by writing to the clock control register. Sample clock rates of 128,64,32,16 and 8 MSamples/sec are possible.

Table 5: Data Set Offset Addresses

Base Address	Function	Word Length	Type
Q5-Q2 + 0	Set Total Power Divisor	6 Bits (LSB)	8 Bit Write
Q5-Q2 + 1	Set Sample rate	8 Bits	8 Bit Write
Q5-Q2 + 0	Read A Register	16 Bits	16 Bit Read
Q5-Q2 + 1	Read B Register	16 Bits	16 Bit Read
Q5-Q2 + 2	Read T. P Divisor	6 bits (6 LSBs)	8 Bit Read
Q5-Q2 + 2	Loop Lock	Bits 7 and 6	8 Bit Read
Q5-Q2 + 3	Serial Number	8 Bits	8 Bit Read

Table 6: Total Power Divder Ratios

Programmed Divisor	A Reg Divisor	B Reg Divisor	Max Integration Range (V/F @ 1MHz)
0-63	1-64	1-64	0.12 - 7.86 seconds
64-127	2-128 (Steps of Two)	2-128 (Steps of Two)	0.24 - 16 seconds

Maximum integration time is estimated by

$$t = n * 61440 / k$$

t is the maximum integration time
n is the register divisor
k is the frequency of the V to F convertor divided by 2, typically 500k.

Table 7: Clock Divider Register Data Words

Sample Clock MHz	Input Band Width	Register Data Word

128	64	0
64	32	8
32	16	12
16	8	14
8	4	15

Connector Pinouts

Table 8: 25 Way D Male Connector

Signal	Number	Type
Ground	1	Power
Ground	2	Power
Wr/Rd	3	D/S Interface Control
Add4	4	D/S Interface Address
Add2	5	D/S Interface Address
Add0	6	D/S Interface Address
Dat6	7	D/S Interface Data
Dat4	8	D/S Interface Data
Dat2	9	D/S Interface Data
Dat0	10	D/S Interface Data
Q5	11	Address Decode
Q3	12	Address Decode
Ground	13	Power
Addstr	14	D/S Interface Control
Hi/Lo	15	D/S Interface Control
Add5	16	D/S Interface Address
Add3	17	D/S Interface Address
Add1	18	D/S Interface Address
Dat7	19	D/S Interface Data
Dat5	20	D/S Interface Data
Dat3	21	D/S Interface Data
Dat1	22	D/S Interface Data
Ground	23	Power
Q4	24	Address Decode
Q2	25	Address Decode

Table 9: 15 Pin D Male Connector

Signal	Number	Type
SYNC +	1	Balanced TTL

BLANK +	2	Balanced TTL
Not Connected	3	
+9 Volts	4	Power
Ground	5	Power
-9 Volts	6	Power
Ground	7	Power
Ground	8	Power
SYNC -	9	Balanced TTL
BLANK -	10	Balanced TTL
+9 Volts	11	Power
Ground	12	Power
-9 Volts	13	Power
Ground	14	Power
+20 Volts	15	Power

Table 10: 9 Pin D Male Connector

Signal	Number	Type
Ground	1	Power
Sign +	2	Balanced ECL Data
Ground	3	Power
Mag +	4	Balanced ECL Data
Ground	5	Power
Ground	6	Power
Sign -	7	Balanced ECL Data
Ground	8	Power
Mag -	9	Balanced ECL Data

Parts List

ECL Printed Circuit Board

PART NAME	DESCRIPTION	PCB PART #	# PER PCB
RF Amplifier	QBH 115	A1	1
0.01UF capacitor	VJ1206Y103MXA-AB	C1-C31,C35,C36	33
0.1UF capacitor	VJ1210Y104KXB	C32-C34	3
75ohm resistor	MMA0204-50HF-75R	R3-R25	22
51ohm resistor	MMA0204-50HF-51R	R1,R2	2
220ohm resistor	MMA-0204-50HF-220R	R26-29	4
110ohm resistor	MMA-0204-50-110R	R30-32	3
Dual Comparator	AD96687BP	U1-U2	2
QUAD OR GATE	MC100E101	U3,U5	2
TRIPLE D FLIP FLOP	MC100E131	U4	1
COUNTER	MC10H136FN	U6-U9	4
HEX BUFFER	MC10H125FN	U10	1
9 PIN D MALE	HIROSE DB9-M	P1	1
SAMECL PCB	Prec Circ #1034		1

Linear Pcb

PART NAME	DESCRIPTION	PCB PART #	# PER PCB
27nF capacitor	VJ1206Y273KXB-AB	C1,C2,C5,C6,C9,C10	6
0.1uF capacitor	VJ1210Y104KXB	C24-30, R7,18&30	9
0.47uF capacitor	T491A474M020AS	C3,C4,C7,C8,C11,C12	6
15uF capacitor	T491156M025AS	C13-C20	8
82 Ohm resistor	MMA0204-50-82R	R51	1
120 Ohm resistor	MMA0204-50-120R	R50	1
120 Ohm resistor	MMA0204-50-120R	R36,R37	2
510 Ohm Resitor	MMA0204-50-510R	R1,R2,R12,R13,R24,R25	6
750 Ohm resistor	MMA0204-50-750R	R10,22,34	3
1k5 Ohm resistor	MMA0204-50-1k5	R9,11,20,23,32,35	6
56kOhm resistor	MMA0204-50-56k	R7,R8,R18,R19,R30,R31	6
120kOhm resistor	MMA0204-50-120k	R3-6,R14-17,R26-29	12
CONNECTOR 25 PIN	HIROSE DB25-M	P1	1
CONNECTOR 15 PIN	HIROSE DB15-M	P2	1
6 PIN SIP HEADER		P3	1
16 PIN HEADER 8 PIN DIP SOCKET		P4 J2	1 1
PFGA	XC3042A-6	U1	1
SERIAL PROM	XC1736DP	U2	1
DIFF. RECEIVER	DS26LS32CM	U3	1

PART NAME	DESCRIPTION	PCB PART #	# PER PCB
TRI OP AMP	LM837M	A1,A2	2
VOLT REG	LM7805CT	VR1	1
VOLT REG	LM7905CT	VR2	1
VOLT REG	LM337T	VR3	1
VOLT REG	LM7815CT	VR4	1
SAMLIN PCB			1

Total Power Pcb

PART NAME	DESCRIPTION	PCB PART #	# PER PCB
RF AMPLIFIER	QBH 102	A1	1
68ohm resistor	MMA0204-50-680	R1	1
130ohm resistor	MMA0204-50-131	R2,R6	2
47kohm resistor	MMA0204-50-473	R4,R5	2
3k9ohm resistor	MMA0204-50-392	R3,R7,R8,R9	4
470ohm resistor	MMA0204-50-471	R10	1
68pF capacitor	VJ1206A680JXB-AB	C4	1
270pF capacitor	VJ1206A271GXB-AB	C3	1
100pF capacitor	VJ1206A101JXB-AB	C2	2
0.01uF Capacitor	VJ1206Y103KXB	C1	
0.1uF capacitor	VJ1206Y104KXB	C5-10	6
OP AMP	OPA177GS	A2,A3	2
V TO F CONVERTOR	VFC121BP	U1	1
3dB Attenuator	MAT 3	ATT1,ATT2	2
10dB COUPLER	PDC-10-1	CPL1	1
TRW BACK DIODE	A1X-618	D1	1
20K POT		RT1	1
1k pot.	4290W-102 CITEC	RT2	1
TOTPOWER PCB	Prec. Cir #1197		1

Construction Notes

Total Power Printed Circuit Board

The Total Power PCB has a fault associated with RT1. The +15V power rail should connect to the wiper of the potentiometer. In order to rectify this problem the following procedure should be followed.

1: Cut trace from R5 to RT1.
2: Drill hole through pcb, near R5 taking care to miss power rail.
3: Cut existing trace on +15V rail to end of potentiometer.
4: Assemble rest of pcb, except for detector diode D1.
5: Link wiper of RT1 to +15V rail, with “wire wrap” wire.
6: Link R5 to the unconnected end of RT1 with “wire wrap” wire.
7: Insert D1.
8: Break pads on A1 component legs, on component side as they will short to component case.
9: Change C1 to 0.01uF to lower -3dB point

ECL Printed Circuit Board

The ECL printed circuit board has one modification. Pin 17 of U2 is to be connected to GND. Follow this procedure to correct problem.

1: Assemble p.c.b.
2: Identify U2 and note that pin 18 is connected to a near by feed-through.
3: Link pin 17 to the feed-through below the feed-through connected to pin 18.
4: On A1 break pads on component legs, on component side, as they will short to case.

Linear Printed Circuit Board

There are two modifications required here. The RESET pin of the Xilinx FPGA is unconnected and connections to the LM337 regulator are wrong. Follow these steps:

1: Assemble the p.c.b. but do not load components.
2: Identify the RESET pin on U1.
3: Solder one end of a 10kOhm resistor to the RESET pin.
4: Connect the other end of the resistor to the VCC end of C24.
5: Assemble board in chassis and mount I.C. regulators.
6: Cut track between R50 and pin 2 of the LM337 I.C.
7: Cut tracks to pins 2 and 3 of the LM337 on the solder side.
8: Swap connections of pins 2 & 3. ie connect pin 2 to VEE, and connect pin 3 to VTT.
9: Connect pin 3 to the free end of R50 on the component side.
10: Break via on track from pin 3 A2, away from solder side ground plane.
11: Feed throughs to POSLV,NEGLV, and O/SLV should be connected to linear board with 100, 0.125W resistors.
12: Check polarity of C3 on the linear pcb, it is shown incorrectly on silk screen overlay. It must be inserted correctly for positive statistic loop to work correctly.

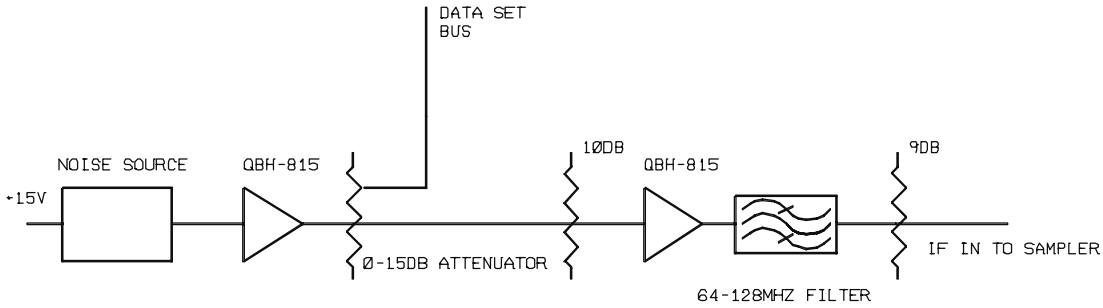
Testing

Prepare the module for test by removing all power supply links from the E.C.L pcb and the Total Power pcb. If the FEI AIX618 back diode is not soldered into position it should be inserted now..***Note static precautions are required***.

Remove power supply links to ECL and Total Power pcbs.

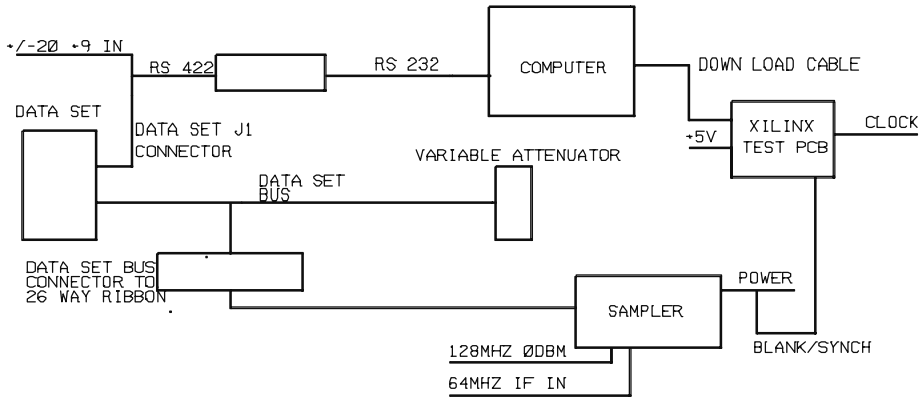
Check for power supply shorts on all p.c.bs. Apply power and check regulator voltages. If all is well power down and reconnect links to the E.C.L and Total Power p.c.bs. Check power supply voltages again, power down if all is well.

Connect test IF signal as shown in figure below.



The digitally controlled attenuator uses a Samsung SMP1103 device. This attenuator is controlled by the Data Set Bus. The address of the attenuator is set to 16. The 10dB attenuator is a variable 0-120dB step attenuator. The bandpass filter is a K&L 8MC10-95/52-0/0. The 7dB attenuator is a 0-12dB step attenuator. The IF power level to the sampler should be -23dBm.

Connect Data Set and Xilinx test pcb as shown below.



The Xilinx test pcb should be programmed with the bit file “test2.bit”. A TTL clock of 10kHz will give a 6 second blank signal. The Synch and Blank differential pairs

should be connected to single ended to differential drivers mounted on the Test pcb. A 128MHz 0dBm clock should be connected to the sampler clock input.

Sampler Statistics Check Out

Check that links SEL01, SEL2 ,SEL3 and SEL4 are set to divide by 16.

Check that the DIV CK test point on the linear p.c.b is a TTL waveform with frequency of 976 Hz. Check that TTL signals at DIV POS, DIV-O and DIV-NEG are in phase with DIV-CK

IF DIV-CK is not correct check signals outlined in Table 1 page 6.

Total Power PCB Checkout

Adjust variable attenuator to 120dB connect a voltmeter to TP2. Use RT1 to set DC amplifier offset to 0.00V. Check V/F output with an oscilloscope, with no input the output frequency should be less than 10Hz with the offset correctly adjusted.

Reset variable attenuator to 10dB. Measure the voltage at TP2 with a voltmeter adjust the input power to give a voltage near one volt at TP2. The V/F Cal pot is adjusted such that the output frequency at V/F OUT has a 1MHz/V characteristic, ie. if TP2 = 1.00V V/FOUT = 1MHz.

The data set interface to the Total Power Detector should be checked by running MULTIRMS.EXE.

Check that the serial number of module is correct. This should be updated when the Preload is programmed into the module. Data bus can be checked by varying serial number.

After Preload is loaded, run the GO option.

Check that the statistics are locked. Check that total power counts are active.

After a number of integrations check that the rms of difference between the two counts is around 10.

If all is well run the A option. When prompted for the number of integrations enter 30. This option will measure the count output for 30 integrations. The program then changes attenuator, until all attenuator values are recorded. The program writes to a file called “test.dat”.