ASKAP Commissioning Update, September 2017

In this issue, we report on recent changes that have been made to ASKAP's digital firmware in response to issues uncovered during commissioning. Several low-level problems have been identified and solved, leading to updates that will increase the stability of the telescope's data acquisition systems.

Understanding the Redback platform

ASKAP's digital signal processing system makes use of a custom platform that we call the Redback. Each Redback chassis hosts six Field Programmable Gate Array (FPGA) devices designed for high-speed digital signal processing, along with communications interfaces and control logic. The signal processing FPGAs need to buffer large amounts of data, so each FPGA is also connected to a Random-Access Memory (RAM) module.

Both the beamformers and correlator are made up of many interconnected Redback chassis which can transmit raw data to each other over high-speed optical interconnects and receive instructions from the telescope operating system software over 1Gb Ethernet.

Communications to and from every Redback are managed by a secondary module called the Bullant. This consists of another FPGA which manages the Ethernet interface, gathers output from the signal processing FPGAs and passes on instructions from the software via a register system.

Improving correlator stability

Correlator problems reported in the July issue of this update have been shown to have several causes, related to low-level signal integrity and logic. Investigation and testing has led to the solutions described below.

Correlator download stalling

One of the main problems we encountered during early science observations was a tendency for chassis within correlator blocks (groups of 12 Redback cards handling a total of 48 MHz bandwidth) to stop sending data to the ingest pipeline. CASS engineers identified two unrelated issues causing this problem:

1. Data corruption on the links between some Bullants and their associated processing FPGAs
2. Correlator inputs drifting out of alignment after initial setup, causing buffer overflows

Although the symptoms of both problems were similar, the two causes are very different.

Inter-FPGA communications

In the first case, data packets transmitted over short distances within each chassis were shown to have a high error rate. This would cause packets to fail their Cyclic Redundancy Check (CRC), excluding them from the final output. In some cases, control bits were also susceptible to corruption, causing more serious state-machine problems than payload errors alone.

The cause of these CRC errors was traced all the way back to the internal Serialiser/Deserialiser (SerDes) modules that drive high-speed Input/Output ports on the FPGAs.

After initially suspecting the internal calibration algorithms that tune these links on power-up, we discovered that the error rates were more closely related to the amount of signal processing load than the initial conditions. This pointed to the quality of the clock signal being used to drive the SerDes modules.

After investigating several approaches, a combination of reducing the clock rate by 20%, forwarding the clock signal over the same physical interface as the data and switching to regional buffering caused the CRC errors to vanish completely. The updated system has been run continuously for several days without a single error.

The decrease in clock rate still provides more than enough capacity to support full ASKAP operation as the bottleneck is the 1 Gb Ethernet interface used to send data to the ingest pipeline, not the inter-FPGA link itself.

Correlator input alignment errors

The signal from each antenna must be time-aligned before it can be correlated. This is done by issuing a sync pulse that is detected at the correlator input during initialisation of the array. It was found that the synchronisation process would sometimes fail on the first attempt (leading to an array that would not come online) and that alignment errors could also arise mid-stream (leading to data loss from the associated input). These alignment errors became more frequent as the number of antennas connected to the correlator increased.

To solve the initialisation problem, the size of the window used to search for the sync pulse was doubled, allowing for larger natural variance between inputs.

Alignment errors occurring post-initialisation were traced to several sources, including unexpected signals from antennas connected to the correlator but excluded from the astronomical data stream.

It was also found that the alignment mechanism could be triggered spuriously after initialisation, leading to undesired re-calibration. These issues were solved with some additional control logic.

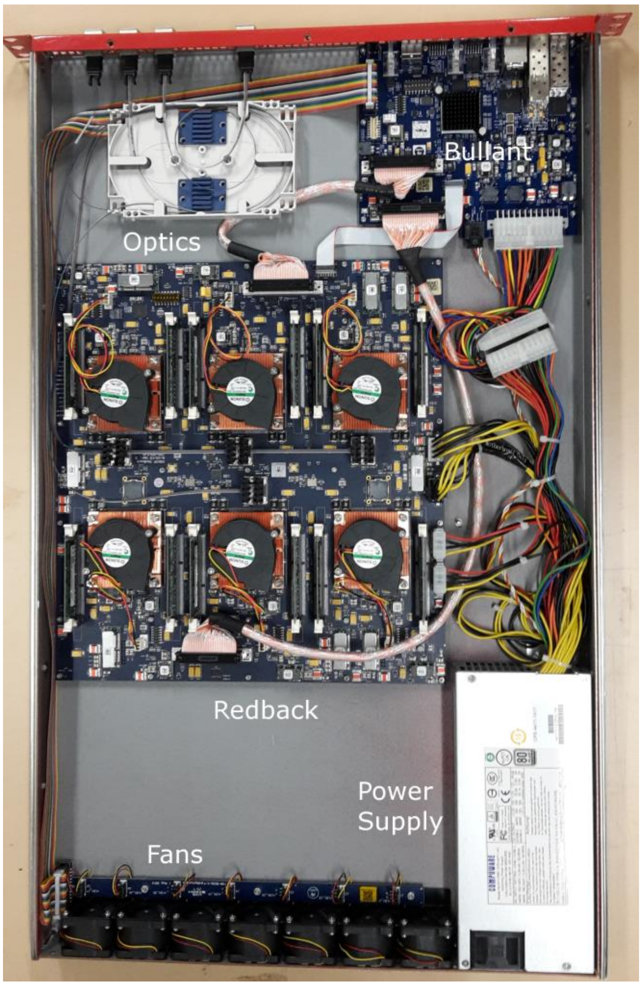

Image: Top-down view of a beamformer chassis with the cover removed to show the components described above.

Removing correlator spectral artefacts

In July, we also reported seeing narrow spikes (not associated with known RFI) and groups of channels with unexplained level shifts in the correlated spectrum. Some of these were indeed related to memory access issues, but several other problems have been solved during of the resulting investigation.

Corner-turn data integrity

A key part of the correlator's logic is the so-called corner turn required to change the indexing of the underlying data when moving from frequency-ordered beamformer output to the time-ordered data required for correlation. This is done in RAM on each Redback.

Passing an artificial uniform input level through the corner-turn logic was shown to produce unexpected non-uniform output. This led to investigation of the memory calibration logic, data pipeline logic and numerical scaling logic, each of which have been improved through updates to the firmware itself, or changes to the way it is driven from the software layer.

On-sky validation and testing

ASKAP's Telescope Operating System version 2.13 was released on the 24th of August, including updated firmware. Extensive testing is now underway and some additional issues have already been identified and solved.

Considering the delays experienced, we will endeavour to obtain key data sets for several of the science teams as part of the validation process. This will allow development of software pipelines and algorithms to continue.

However, before embarking on a lengthy observing campaign, we intend to finish the commissioning of several other key subsystems. This includes enabling parallel multi-file output from the ingest pipeline and moving to a centralised fringe rotator control scheme. Both are required to grow the array in bandwidth and number of antennas. The fringe rotator changes will also reduce the amount of flagging on long baselines.

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