# Data Transmission Synchronisation

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**At the Antenna:**

The signal BLANK controls the sync generation at the antenna. BLANK is set active by an event generator signal, marking the end of the current integration. As long as BLANK is active, zero's are transmitted on the data line. This occurs during the time between integration periods. At the instant when BLANK goes inactive, the SYNC code of 1101 is sent, followed by the first data sample of the new integration.

**At the Central Site:**

The sync detector is armed by the WINDOW signal, provided by an event generator. Whilst WINDOW is active, the sync detector searches for the occurrence of the SYNC code, 1101, which must be preceeded by either 16 zeros ***or*** 15 zeros and one "don't care" bit, depending on the current state of the sync detector. When the required sequence is detected, the next 1,2 or 4 bits are accepted as the first sample. If the SYNC pattern is not detected during the period that WINDOW is active, then an error flag is raised, indicating that the data is invalid in that particular channel. The WINDOW signal should remain active for only a short period so as to aid in the detection of clock errors at the antenna and to reduce the probability of an extraneous SYNC pattern being accepted.

The WINDOW signal also plays a role in the resolution of the ambiguity inherent to the Manchester decoding. It is assumed that during a period of a few microseconds before WINDOW goes active, the data is fixed on zero, corresponding to being blanked at the antenna. Obviously this requires that the BLANK signal at the antenna and the WINDOW signal at the central site are suitably synchronised.

**In the Sampler:**

The time at which BLANK goes inactive determines the start of an integration period and is controlled by the "integration" clock. This is a programmable pulse generator, whose period and phase can be set at intervals of 16 nanoseconds. The maximum period is 32 seconds. It is driven by a fixed phase 128MHz clock from the L.O. reference generators and is intended to provide a precise start time for each integration period, accurate to a fraction of a sampling period over a number of days operation.

Once the phase and period of the integration clock have been set and calibrated, the start time of each ensuing integration can be calculated and thence the starting phase of the sampling clock required to cause the first sample to be taken at the correct time. Note (see Fig. 1) that the sampler clock phase is set by locking the 128MHz (4Bit) sampler clock to a variable phase 128MHz reference frequency. The 512MHz (1Bit) and the 256MHz (2Bit) sampler clocks have a fixed relationship to the 128MHz (4Bit) sampler clock.

Within the sampler, the BLANK signal is "latched" by the 128MHz (4Bit) sampler clock. The first 128MHz sampler clock pulse which latches an inactive BLANK signal, starts the integration. With this method, a problem can arise when the sampler clock phase is such as to cause a 128MHz sampler clock pulse to occur at the same instant as, or very close to, the BLANK active to inactive transition. In this case, the performance of the latch circuit can not be predicted, and an error of 1,2 or 4 samples may result, depending on whether the sampler is operating in 4,2 or 1Bit mode respectively. The sampler clock phase at which this occurs, measured relative to the integration clock, is easily determined by taking a series of integrations with different start phases, and noting the point at which the measured correlation function jumps by the appropriate number of samples. During observations, whenever the required sampler start phase approaches this predetermined value, the BLANK active to inactive transition is advanced by 4 nanoseconds (180° at 128HHz), thus avoiding any problems within the latch circuit.

Note:
In 1 and 2Bit modes the "early" version of BLANK is not necessary. In this case, the range of the 128MHz variable phase reference signal need only be 90° or 180° respectively, - e.g. a change of 180° in the reference signal will change the 2Bit sampler clock by 360°, - i.e. no change. Hence the coincidence problem mentioned above can be avoided in 1 and 2Bit modes by adding an extra 180° to the 128MHz sampler clock. This is probably of little practical interest as it introduces a different method which is not applicable to 4Bit mode.

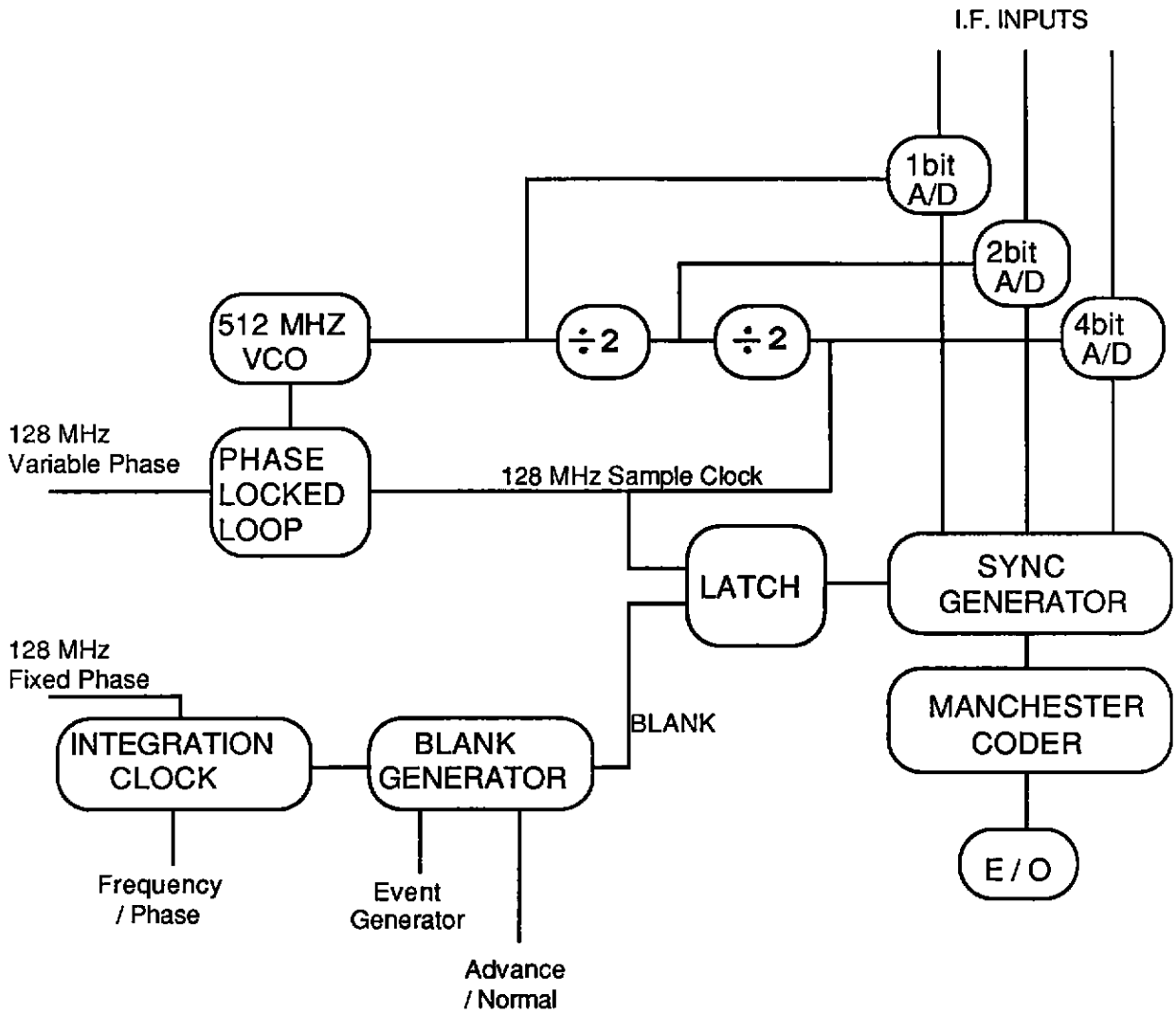
I.F. INPUTS
1bit A/D
2bit A/D
4bit A/D
512 MHZ VCO
÷2
÷2
128 MHz Variable Phase
PHASE LOCKED LOOP
128 MHz Sample Clock
LATCH
SYNC GENERATOR
128 MHz Fixed Phase
INTEGRATION CLOCK
BLANK GENERATOR
BLANK
MANCHESTER CODER
E / O
Frequency / Phase
Event Generator
Advance / Normal

Figure 1.