DRAFT

AUSTRALIA TELESCOPE L.O. SYSTEMS. 24 Jan 1990

The following report is an updated draft of part of a user manual for the local oscillator systems for the AT compact array. It contains specifications, programming instructions and notes for users. It is issued now to aid users, to allow comment and to help discover oversights or errors.

A.C.Young

FIG 1 RACK LAYOUT

0 Introduction:

FIG 2 & 3 LO DIAGRAMS FIG 4 CONV. SYSTEM

1 Specifications:

- 1.1 "7 GHz" (C/X) SYNTHESISER (Module L4)
- 1.2 "2 GHz" (L/S) SYNTHESISER (Module L3)
- 1.3 UHF SYNTHESISERS (module L2)
- 1.4 SAMPLER CLOCK OSCILLATORS (Module L1)
- 1.5 SYNC GENERATOR CLOCK

2 Programming the local oscillators

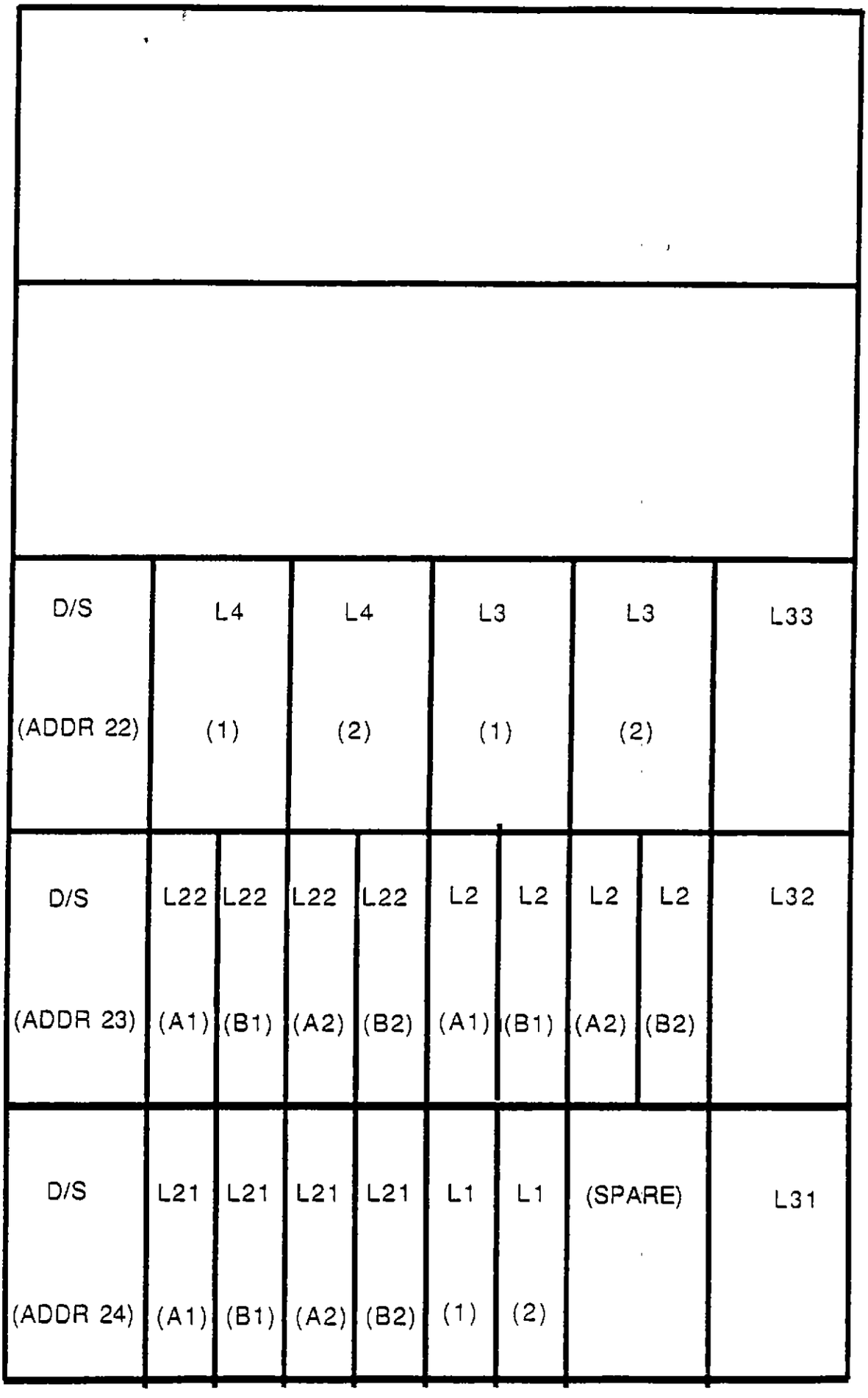
- 2.1 "7 GHz" (C/X) SYNTHESISER (Module L4)
- 2.2 "2 GHz" (L/S) SYNTHESISER (Module L3)
- 2.3 UHF SYNTHESISER (Module L2)
- 2.4 PHASE ROTATION (UHF SYNTHESISER and SAMPLER CLOCK)
  - Phase calculation
  - Rate calculation
  - Second derivative calculation
  - Check bits calculation
  - Bit pattern construction
- 2.5 GENERAL
  - Event generator-LO stop/run pulse requirements

3

- 3.1 A QUICK FAULT FINDING GUIDE
- 3.2 OPERATION OF LO INTERFACES
- 3.3 YIG TUNED OSCILLATORS
- 3.4 MIXERS
- 3.5 MODULE ADDRESS BOARD
- 3.6 TEMPERATURE MON BOARD
- 3.7 POSITRONIC CONNECTORS
- 3.8 5MHz LO DISTRIBUTION DIAGRAM.

23 MAY 1990

L.O. RACK LAYOUT. (Front View)



THE AT LOCAL OSCILLATOR SYSTEM

This manual is intended as an introduction to the Australia Telescope local oscillator (LO) system, as a guide to the use of the LOs and also to describe various components or techniques which are common to all modules such as racks, phase detectors and mixers. For more detailed information the individual manuals should be consulted.

BASICS

Virtually all radio astronomy receivers down convert the incoming microwave signal to a more managable frequency for subsequent filtering, sampling and computer processing. This down conversion is accomplished by subtracting a known, fixed and stable LO frequency from the incoming signal frequency.

It is possible to construct an astronomy receiver containing only a high gain amplifier and a sampler to convert the signal to digital form for a computer or correlator. This system will probably work to several hundred MHz, but tuning is difficult and there are severe design problems at microwave frequencies at the present time.

Down conversion can be accomplished in a single step, but it is more common to use several stages to avoid unwanted 'image' responses, especially in receivers with a wide tuning range. Variable input tuning (as in normal AM radios) is otherwise necessary and this creates difficulties, especially with computer control of the tuning. Multiple conversion does however increase the likelihood of the internal generation of unwanted spurious 'birdie'signals. At each conversion the LO frequency is subtracted from the signal frequency to produce a new signal containing the same signal information but translated to a lower and more managable 'intermediate frequency 'or IF. Each conversion stage requires a separate LO and all LO signals in all antennas must be locked together in phase in order to preserve the coherence of the signal.

The most straightforward way to do this would be by generating all LOs at the central building, splitting each signal 6 ways and sending to all 6 antennas. It is impractical to send of the order of 5 GHz over at least 2 km of cable. Instead a lower reference frequency F_1 of 160 MHz is sent to each antenna and all required LO signals are derived from this reference. This is about the highest frequency that is practical since even with large (22 mm diameter) coaxial cable, the loss at 160 MHz is such that less than 1/10,000 of the signal power sent actually arrives at the far end.

All LOs are controlled using methods of closed loop frequency control (phase lock loops). Phase locked oscillators (for historical reasons commonly known as 'synthesisers') are not continuously variable in frequency but can only be tuned in descrete steps. Within the AT, the LOs are tuneable in steps of 320 MHz, 10 MHz or 1 MHz depending on the synthesiser. The effective total antenna LO (ie.the sum of all LOs) is always variable in 1 MHz steps. Finer steps will be available within the narrowband backend system.

With the exception of L1 all LOs are programmable via the datasets. Generally this requires a 16 bit transfer on the bus plus the setting of several single bit lines to set operating mode etc. The phase rotators require four 16 bit transactions.

All LOs and phase rotators are stopped for 16 mS at the end of every 5 Second cycle. At that time the frequency and phase will be changed to reflect the new data loaded within the preceeding cycle. For faster frequency switching the cycle time can be reduced to 1 second.

All LOs have nominally 10mW (+10dBm) of output power with typically around ± 1dB variation with frequency.

Figure 1 shows the components of the LO system and its relationship to the receiver conversion system. Figure 2 shows the LO modules in more detail with the individual loops and reference frequencies shown.

THE LINE STABILISER

This subsystem measures the electrical length of the LO reference distribution cable between the central building and each antenna. The corrections for cable length changes are made indirectly via the computer, rather than in a closed electrical loop. At each antenna a high spectral purity 5 MHz crystal oscillator is connected to a series of doublers to give F_2 = 160 MHz as one of its outputs. This 160 MHz is compared and locked (via a voltage control applied to the 5 MHz oscillator) to the incoming F_1 = 160 MHz in a phase lock loop. The antenna 160 MHz is also sent back to the centre where it is compared in phase to the origional F_1 reference. All cable length changes are monitored by this measurement of the round trip path length and appropriate corrections made. The outgoing F_1 reference is actually sent as two separate frequencies of 160.05 MHz and 0.05 MHz to prevent cross coupling to the return 160 MHz. There are many additional complications to this scheme since all antennas share the same cable. Refer to the appropriate manual for more details.

THE REFERENCE CHAIN (L31, I32, I33)

The previously mentioned chain of doublers is part of a reference chain at the antenna which generates, from the basic 5MHz oscillator (stabilised by the line stabiliser), all the frequencies needed by the LO synthesisers, sampler clock and integration clock. These are 5, 7.99, 9.99, 10, 20, 120, 128, 160, 320, 480, 640, and 800 MHz. A series of 7 doublers, amplifiers and filters first generate 5, 10, 20, 40, 80, 160, 320 and 640 MHz and a series of stable dividers give 1 MHz, 2 MHz and 10 kHz. A phase lock loop generates 9.99 MHz from 10 MHz and 10 kHz and then 7.99 MHz is obtained by mixing 2 MHz with 9.99 MHz. The 120 MHz reference is derived from a mix of 80 and 40 MHz and 128 MHz from 120, 10 and 2 MHz. Similarly 480 and 800 MHz are obtained from 640 and 160 MHz.

THE 7 GHz SYNTHESISER (L4)

There are two phase locked 7 GHz LO synthesisers per antenna with each driving two receiver channels. They are not used for ~~input~~ receive frequencies below 3 GHz. The internal phase-lock loop locks with a 10 MHz offset to a 'comb' of frequencies (320 MHz spacing) generated by

a 'step recovery diode' pulse generator. The output is obtained from a YIG (Yttrium Iron Garnet ferrite resonator) tuned oscillator and can take frequencies of N * 320 ± 10 MHz within the range of 6710 to 8330 MHz.

THE 2 GHz SYNTHESISER (L3)

There are two phase locked 2 GHz LO synthesisers per antenna with each driving two receiver channels. The internal phase-lock loop locks with a 5 MHz offset to a 'comb' of frequencies (20 MHz spacing) generated by a 'step recovery diode' pulse generator. The output is obtained from a YIG tuned oscillator and takes frequencies of N * 20 ± 5 MHz within the range of 1815 to 2215 MHz.

THE UHF SYNTHESISER (L2)

There are four independant phase locked synthesisers per antenna. The double-offset loop locks with a 10 MHz final offset to a simplified 'comb' of frequencies (160 MHz spacing) generated by simple mixing and an extra offset of frequency F = 41 to 50 MHz.. The output is obtained from a varactor tuned oscillator and takes frequencies of N * 160 ± (F -10) MHz within the range of 511 to 840 MHz. The signal of frequency F is derived from a simpler secondary loop with a feedback divider and 1MHz reference.

The 10 MHz final offset is variable in phase (and rate and second deriv.) via the phase rotators.

THE SAMPLER CLOCK (L1)

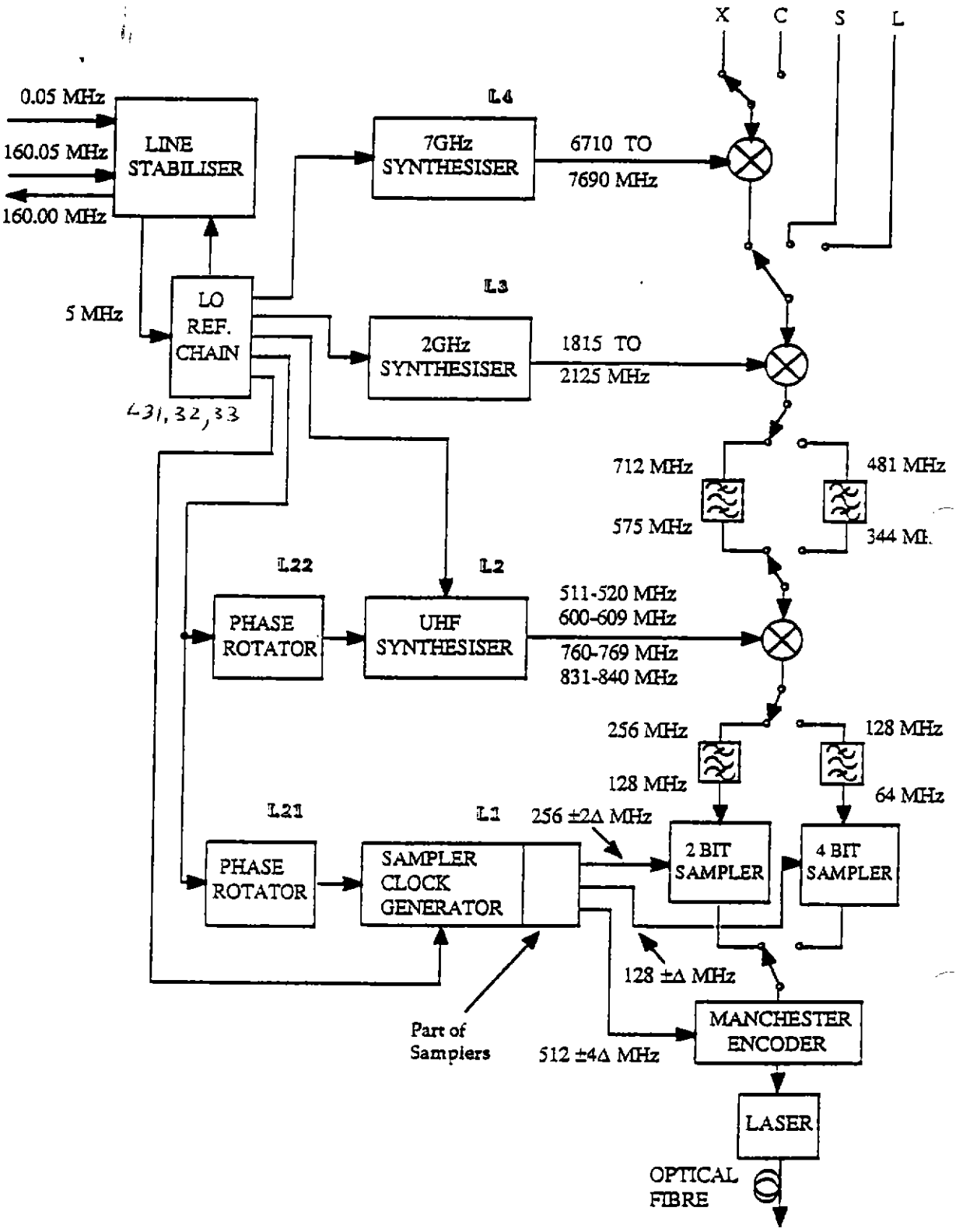
There are four independant sampler clocks per antenna. Each is a phase-locked oscillator which is fixed in frequency. The loop locks to 512 MHz with a division by 4 feedback divider, within the sampler module. This gives the 512, 256 and 128 MHz clocks needed by the samplers and coders. The 128 MHz signal is phase-locked to the 8 MHz phase rotated signal, with a 120 MHz offset.

THE PHASE ROTATORS (L21, L22)

The phase rotator L22 contains a 10 MHz loop with a 10 kHz offset and a 9.99 MHz reference. Similarly the phase rotator L21 contains an 8 MHz loop with a 10 kHz offset and a 7.99 MHz reference.

The 10 kHz offset frequency is derived from 20 MHz in a special continuously variable digital divider. The 10 kHz frequency (and hence the output frequency) can be set and varied in phase in 0.18 degree steps. This variation in phase can be performed on the run to achieve phase rates up to a maximum of 720 degrees per millisecond. By varying the rate at which phase is changed a second derivative (curvature) capability is obtained.

The output of L22 is used as an offset within L2 and the phase changes are transferred to the UHF LO output. Similarly L21 is used by the sampler clock.



THE ANTENNA L.O. SYSTEM

SHOWING ITS RELATIONSHIP TO THE CONVERSION SYSTEM

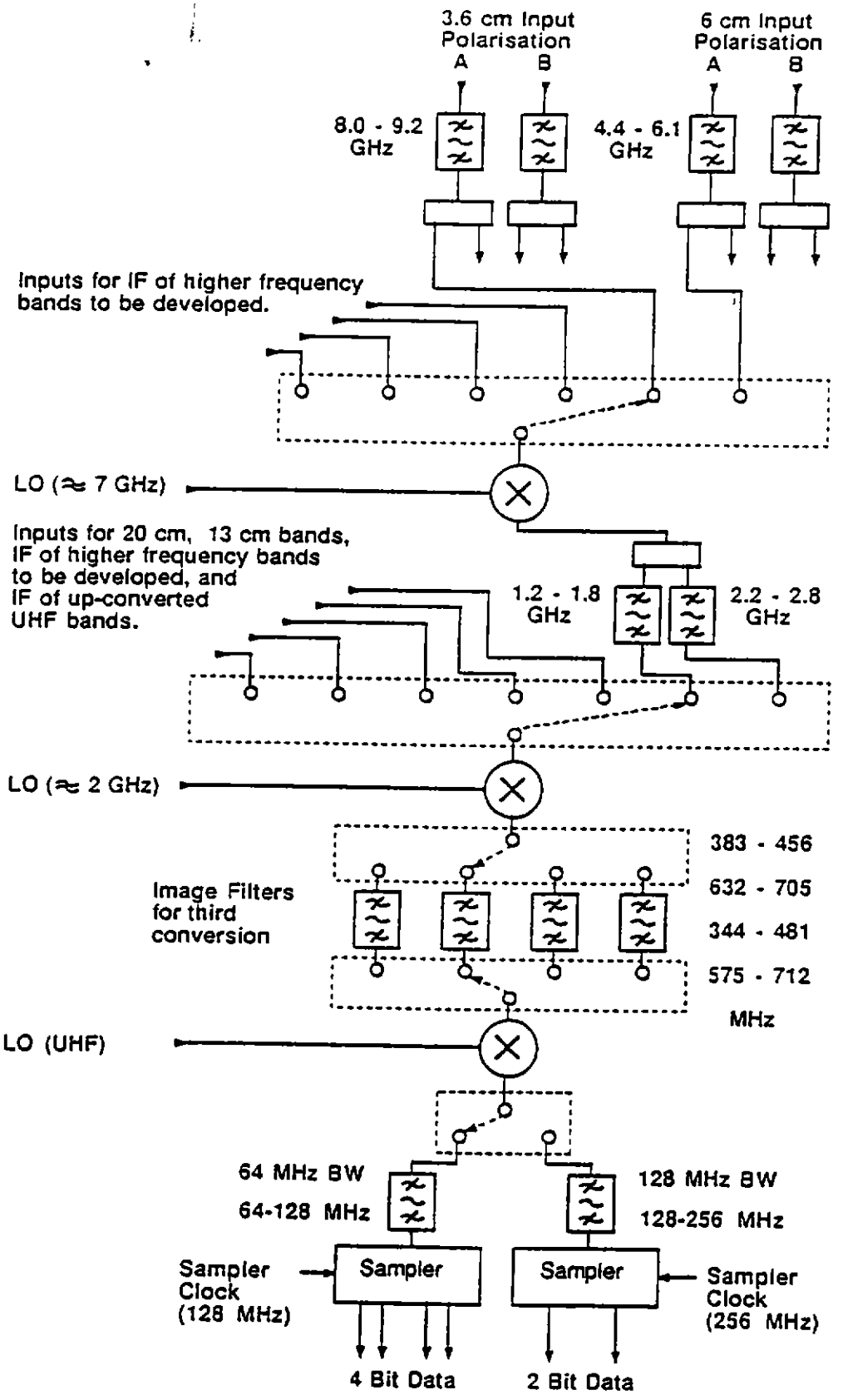


Fig 1. Australia Telescope Antenna Down-Conversion System

1.1' "7 GHz" (C/X) SYNTHESISER (Module L4) Specifications:
Each antenna contains two independent 7 GHz synthesisers.
Each has two identical outputs, giving 4 outputs for the 4 conversion channels.

POWER OUTPUT (Each output)
10 milliwatts (+10 dBm) ± 2 dB

FREQUENCY RANGE
6710 to 8330 MHz

OUTPUT FREQUENCY
Can only take discrete values given by

F = N * 320 ± 10 MHz
(where N is an integer between 21 and 25).

This is essentially 320 MHz steps.

PHASE NOISE
Better than 3 degrees rms.
This should give much less than 1% loss of correlation

PHASE STABILITY
Better than 3 degrees rms over any 30 minutes
With respect to central site "clock"
This is necessary to maintain accuracy between calibrations.

HARMONICS
At least 50 dB below carrier

SPURIOUS OUTPUTS
At least 100 dB below carrier
This is needed to avoid spurious signals in the IF from contaminating the spectra. Phase switching will give another 20dB of rejection and phase rotatio.. will usually remove any residual.

FREQUENCY SWITCHING
16 milliseconds maximum blanking time needed to switch frequencies.
Once per 5 second sync cycle maximum switching rate
(can be reduced by reducing the 5 sec cycle).
Note: There may be tighter software constraints.

1.2 "2 GHz" (L/S) SYNTHESISER (Module L3) Specifications:

Each antenna contains two independent 2 GHz synthesisers
Each has two identical outputs, giving 4 outputs for the 4 conversion channels.

POWER OUTPUT (Each output)
10 milliwatts (+ 10 dBm) ± 1.5 dB

FREQUENCY RANGE
1815 to 2215 MHz

OUTPUT FREQUENCY
Can only take discrete values given by

$F = N * 20 \pm 5$ MHz
(where N is an integer between 91 and 111)

That is 10 MHz steps.

PHASE NOISE
Better than 3 degrees rms.
This should give much less than 1% loss of correlation

PHASE STABILITY
Better than 1 degree rms over 30 minutes
With respect to central site "clock"
This is necessary to maintain accuracy between calibrations.

HARMONICS
At least 50 dB below carrier.

SPURIOUS OUTPUTS
At least 100 dB below carrier
This is needed to avoid spurious signals in the IF from contaminating the spectra. Phase switching will give another 20dB of rejection and phase rotation will usually remove any residual.

FREQUENCY SWITCHING
16 milliseconds maximum blanking time needed to switch frequencies.
Once per 5 second sync cycle maximum switching rate
(can be reduced by reducing the 5 sec cycle).
Note: There may be tighter software constraints.

1.3 UHF SYNTHESISER (module L2) Specifications:

Each antenna contains four independent UHF synthesisers with each output driving one of the 4 conversion channels.

Each synthesiser can be independently set in frequency, phase, rate, etc. by using its associated phase rotator.

POWER OUTPUT
10 milliwatts (+ 10 dBm) ±1.5 dB.

FREQUENCY RANGE (Rest frquencies - without phase rotation)
Four separate bands are provided with 1 MHz steps within each band.
Band L 4 gives 511 to 520 MHz
Band L 2 gives 600 to 609 MHz
Band U4 gives 760 to 769 MHz
Band U2 gives 831 to 840 MHz

PHASE NOISE
Better than 3 degrees rms
This should give much less than 1% loss of correlation

PHASE STABILITY
Better than 1 degree rms over 30 minutes
With respect to central site "clock" reference.
This is necessary to maintain accuracy between calibrations.

HARMONICS
At least 30 dB below carrier

SPURIOUS OUTPUTS
At least 70 dB below carrier - See under "Phase rate" for close-in sidebands.
This is needed to avoid spurious signals in the IF from contaminating the spectra. Phase switching will give another 20dB of rejection and phase rotation will usually remove any residual.

FREQUENCY SWITCHING
16 milliseconds blanking time needed to switch frequencies.
Once per 5 second sync cycle maximum switching rate
(can be reduced by reducing the 5 sec cycle but there may be software constraints)

PHASE ROTATOR SWITCHING
16 milliseconds blanking time needed (concurrent with frequency switching).
Once per 5 second sync cycle maximum switching rate
(can be reduced by reducing the 5 sec cycle but there may be software constraints)

PHASE

Start phase can be set over the range 0 to 360 degrees in 0.18 degree steps.
Start phase is the phase at the start of the next 5 sec. sync cycle as defined by the event generator L.O. stop - run (TTL lo to hi) transition.

PHASE RATE (First derivative)

Start phase rate can be set over the range - 2 KHz (ie. > 10^4 rads/sec) to + 2 KHz in steps < 0.2 millihertz (0.07 deg / sec)
This rate is the rate at the start of the next 5 second sync cycle (see programming section).

Rate is a "staircase" type slope with a step size of 0.18 degrees. This results in close-in sidebands (less than 100kHz away) which are at least 55 dB below carrier.

SECOND DERIVATIVE (phase curvature)

Can be set over the range + 2.4 Hz per sec.to - 2.4 Hz per sec in steps of approximately 10^{-5} Hz per sec.

1.4 SAMPLER CLOCK OSCILLATOR (Module L1) Specifications:

Each antenna contains four independent oscillators (2 per module) to drive the four samplers.

Each oscillator can be independantly set in phase (ie. time delay), rate and second derivative by using its associated phase rotator. Other than via the phase rotator this oscillator is not computer controlled.

(the samplers determine the 512 / 256 / 128 MHz selection).

POWER OUTPUT

10 milliwatts (+10 dBm) ± 1dB

FREQUENCY

The output rest frequency is 512 MHz (without phase rotation) for 1 bit sampling and this is then twice divided by two in the samplers for 2 and 4 bit sampling. After dividing by four the resulting 128MHz (ie. 4 bit sampling signal) has a phase (time delay) and rate which can be set over the same range as the UHF synthesiser .

It is important to note that the sampler clock output is divided by 2 or 4 in the samplers. However the phase and phase rate (and 2nd deriv) are automatically doubled for 2 bit sampling and doubled again for 1 bit sampling so that the time delay is independant of sample rate (see below).

Caution is needed since there is a maximum range of 0 to 360 degrees or 0 to 7.8125 nSeconds. (There is actually only 0.5 this at 2bit and 0.25 at 1 bit but the window selection within the samplers looks after this ??). Any further delay must be made in the delay units.

PHASE NOISE

Better than 3 degrees rms

PHASE STABILITY

Better than 1 degree rms over 30 minutes (at 128MHz)
With respect to central site "clock"

SPURIOUS AND HARMONIC OUTPUTS

At least 50 dB below carrier

DELAY (PHASE)

Start delay can be set over the range 0 to 7.8125 nS (ie. 0 to 360° at 128MHz)
in 0.00390625 nS steps (0.18° at 128MHz)
Start delay is the delay at the start of the next 5 second sync cycle
as defined by the *lo to hi* transition of the event generator L.O.stop-run pulse.

DELAY RATE (First derivative)

Can be set over the range ± 15 μS per second (ie. ≈ ± 10^4 rads/sec at 128MHz) in steps of <0.002 nS per second (0.07 deg / sec).

This rate is the rate at the start of the next 5 second sync cycle.

SECOND DERIVATIVE (phase curvature)

Although not normally required this can be set over the range ± 18 nS per sec^2 (± 2.4 Hz at 128MHz) in steps of approximately 0.08pS per sec^2.

1.5 SYNC GENERATOR CLOCK Specifications:

The sync generator clock gives a single CW output and provides the clock for the sync generator to give the nominally 5 second sync pulses. There is only one such clock in each antenna and it is part of the reference chain in module L31. This clock is not computer controlled.

POWER OUTPUT

10 milliwatts (+10 dBm) ±1 dB

FREQUENCY

128 MHz

PHASE NOISE

Better than 5 degrees rms

PHASE STABILITY

Better than 5 degree rms over 30 minutes
With respect to central site "clock"

SPURIOUS AND HARMONIC OUTPUTS

At least 25 dB below carrier

2 Programming the local oscillators

2.1 "7 GHz" (C/X) SYNTHESISER (Module L4) Programming

There are two 7GHz synthesisers which are referred to in software as "L401"and "L402" and are found at locations AL303 and AL305 (A is the antenna number). These are controlled by the data set with decimal address 22 (16 hex). The full accmaint address is therefore 16 03 or 16 05. ?????????

Frequency data can be loaded into this module prior to switching to a new frequency without disturbing the current operation of the module. Two such frequencies can be loaded and selected by single bit lines. To set to a frequency that has been preloaded, select F1 or F2 via the single bit line and set the "enable next event" single bit line high. The freqency will change on the next blanking pulse of the event generator "LO stop/run" pulse. Restore the "enable next event"line to TTL low to prevent frequency resetting every 5 seconds.

The frequency of this L.O. is set by a 16 bit digital word. The numbers which have to be sent to the appropriate data set and thence to the module interface are shown below. The 12 most significant bits set the free running frequency of the YIG oscillator where 4096 corresponds to 10.0 GHz.

ie.

$$M = 2^{12} * F / (10,000 \text{ MHz})$$

or

$$M = 0.4096 * F (\text{MHz})$$

where

$$6710 \leq F \leq 8330 \text{ MHz}$$

and F can only take discrete values given by

$$F = N * 320 \pm 10 \text{ MHz} \quad (N \text{ is an integer between 21 and 25 })$$

eg. for F = 7050 MHz, M = 2888 = 1011 0100 1000

The next bit controls the sign of the gain of the loop amplifier, a 1 corresponds to an upper sideband lock and a 0 to a lower sideband lock (ie. - 10 MHz).
eg. for 7050 MHz this bit is 1 (since 7050 = 22 * 320 + 10).
The last three bits are reserved for future use and are normally set to zero.
The ability to insert a 3 bit number here should be preserved.

The table entries (over) marked as "*" are out of range and may not lock but are used for testing.

FREQUENCY (MHz)		DECIMAL (First 12 bits only)	BINARY				HEX NO.
5750	*	*2355*	*1001*	*0011*	*0011*	*0000*	*93 30*
5770	*	*2363*	*1001*	*0011*	*1011*	*1000*	*93 B8*
6070	*	*2486*	*1001*	*0011*	*0110*	*0000*	*9B 50*
6090	*	*2494*	*1001*	*0011*	*1110*	*1000*	*9B E8*
6390	*	*2617*	*1010*	*0011*	*1001*	*0000*	*A3 90*
6410	*	*2626*	*1010*	*0100*	*0010*	*1000*	*A4 28*
6710		2748	1010	1011	1100	0000	AB C0
6730		2757	1010	1100	0101	1000	AC 58
7030		2879	1011	0011	1111	0000	B3 F0
7050		2888	1011	0100	1000	1000	B4 88
7350		3011	1011	1100	0011	0000	BC 30
7370		3019	1011	1100	1011	1000	BC B8
7670		3142	1100	0100	0110	0000	C4 60
7690		3150	1100	0100	1110	1000	C4 E8
7990		3273	1100	1100	1001	0000	CC 90
8010		3281	1100	1101	0001	1000	CD 18
8310		3404	1101	0100	1100	0000	D4 C0
8330		3412	1101	0101	0100	1000	D5 48
8630	*	*3535*	*1101*	*1100*	*1111*	*0000*	*DC F0*
8650	*	*3543*	*1101*	*1101*	*0111*	*1000*	*DD 78*
8950	*	*3666*	*1110*	*0101*	*0010*	*0000*	*E5 20*
8970	*	*3674*	*1110*	*0101*	*1010*	*1000*	*E5 A8*
9270	*	*3797*	*1110*	*1101*	*0101*	*0000*	*ED 50*
9290	*	*3805*	*1110*	*1101*	*1101*	*1000*	*ED D8*

2.2 "2 GHz" (L/S) SYNTHESISER (Module L3) Programming

There are two 2GHz synthesisers which are referred to in software as "L301"and "L302" and are found at locations AL307 and AL309 (A is the antenna number). These are controlled by the data set with decimal address 22 (16 hex). The full accmaint address is therefore 16 07 or 16 09. ??????

Frequency data can be loaded into this module prior to switching to a new frequency without disturbing the current operation of the module. Two such frequencies can be loaded and selected by single bit lines. To set to a frequency that has been preloaded, select F1 or F2 via the single bit line and set the "enable next event" single bit line high. The freqency will change on the next blanking pulse of the event generator "LO stop/run" pulse. Restore the "enable next event"line (ie. set to TTL low) to prevent frequency resetting every 5 seconds.

The frequency of this L.O. is set by a 16 bit digital word. The numbers which have to be sent to the appropriate data set and thence to the module interface are shown below. The 12 most significant bits set the free running frequency of the YIG oscillator where 4096 corresponds to 2.5 GHz.

ie.

$$M = 2^{12} * F / (2500 \text{ MHz})$$

or

$$M = 1.6384 * F (\text{MHz})$$

where

$$1815 \leq F \leq 2215 \text{ MHz}$$

and F can only take discrete values given by

$$F = N * 20 \pm 5 \text{ MHz} \quad (N \text{ is an integer between 91 and 111 })$$

eg. for F = 1985 MHz M = 3252 = 1100 1011 0100

The next bit controls the sign of the gain of the loop amplifier, a 1 corresponds to an upper sideband lock and a 0 to a lower sideband lock (ie. - 5 MHz).
eg. for 1985 MHz this bit is 1 (since 1985 = 99 * 20 + 5).
The 3 least significant bits are reserved for future use and are normally set to 0.
The ability to insert a 3 bit number here should be preserved.

Table entries (over) marked as "*" are out of range and may not lock but are use for testing.

FREQUENCY (MHz)		DECIMAL (First 12 bits only)	BINARY				HEX
1 795	*	*2941*	*1011*	*0111*	*1101*	*0000*	*B7 D0*
1 805	*	*2957*	*1011*	*1000*	*1101*	*1000*	*B8 D8*
1 815		2974	1011	1001	1110	0000	B9 E0
1 825		2990	1011	1010	1110	1000	BA E8
1 835		3006	1011	1011	1110	0000	BB E0
1 845		3023	1011	1100	1111	1000	BC F8
1 855		3039	1011	1101	1111	0000	BD F0
1 865		3056	1011	1111	0000	1000	BF 08
1 875		3072	1100	0000	0000	0000	C0 00
1 885		3088	1100	0001	0000	1000	C1 08
1 895		3105	1100	0010	0001	0000	C2 10
1 905		3121	1100	0011	0001	1000	C3 18
1 915		3138	1100	0100	0010	0000	C4 20
1 925		3154	1100	0101	0010	1000	C5 28
1 935		3170	1100	0110	0010	0000	C6 20
1 945		3187	1100	0111	0011	1000	C7 38
1 955		3203	1100	1000	0011	0000	C8 30
1 965		3219	1100	1001	0011	1000	C9 38
1 975		3236	1100	1010	0100	0000	CA 40
1 985		3252	1100	1011	0100	1000	CB 48
1 995		3269	1100	1100	0101	0000	CC 50
2 005		3285	1100	1101	0101	1000	CD 58
2 015		3301	1100	1110	0101	0000	CE 50
2 025		3318	1100	1111	0110	1000	CF 68
2 035		3334	1101	0000	0110	0000	D0 60
2 045		3351	1101	0001	0111	1000	D1 78
2 055		3367	1101	0010	0111	0000	D2 70
2 065		3383	1101	0011	0111	1000	D3 78
2 075		3400	1101	0100	1000	0000	D4 80
2 085		3416	1101	0101	1000	1000	D5 88
2 095		3432	1101	0110	1000	0000	D6 80
2 105		3449	1101	0111	1001	1000	D7 98
2 115		3465	1101	1000	1001	0000	D8 90
2 125		3482	1101	1001	1010	1000	D9 A8
2 135		3498	1101	1010	1010	0000	DAA0
2 145		3514	1101	1011	1010	1000	DB A8
2 155		3531	1101	1100	1011	0000	DC B0
2 165		3547	1101	1101	1011	1000	DD B8
2 175		3564	1101	1110	1100	0000	DE C0
2 185		3580	1101	1111	1100	1000	DF C8
2 195		3596	1110	0000	1100	0000	E0 C0
2 205		3613	1110	0001	1101	1000	E1 D8
2 215		3629	1110	0010	1101	0000	E2 D0

2.3 UHF SYNTHESISER (Module L2) Programming

There are four UHF synthesisers which are referred to in software as "L2A1", "L2A2", "L2B1" and "L2B2" and are found at locations AL407 , AL408, AL409 and AL410 and are phase controlled by the phase rotator modules (L22A1 toL22B2–se next section) in locations AL403, AL404, AL405 and AL406 respectively where A is the antenna number.

These are controlled by the data set with address 23 (17 hex).
The full address is therefore 17 07 , 17 08, 17 09 or 17 10. ???????

Frequency data can be loaded into this module prior to switching to a new frequency without disturbing the current operation of the module. Two such frequencies can be loaded and selected by single bit lines. To set to a frequency that has been preloaded, select F1 or F2 via the single bit line and set the "enable next event" single bit line high. The freqency will change on the next blanking pulse of the event generator "LO stop/run" pulse. Restore the "enable next event"line to prevent frequency resetting every 5 seconds.

The frequency can only take values in 1MHz steps over 4 separated bands
Band L 4 gives 511 to 520 MHz
Band L 2 gives 600 to 609 MHz
Band U4 gives 760 to 769 MHz
Band U2 gives 831 to 840 MHz

An 8 bit number is required to set the rest frequency.
The most significant bit is not used and should be set to 0 (1 in manual).
The next two bits set the required band .
The five least significant bits set the 1 MHz steps as shown in the table over.

Entries marked with "*" are not valid (high phase error) but are used for testing.

Phase ,rate etc are set via the phase rotator -- see section 2.4

FREQ (MHz)		BINARY	HEX
L4 (000)			
510	*	*0001 1000*	*18*
511		0001 0111	17
512		0001 0110	16
513		0001 0101	15
514		0001 0100	14
515		0001 0011	13
516		0001 0010	12
517		0001 0001	11
518		0001 0000	10
519		0000 1111	0F
520		0000 1110	0E
L2 (001)			
600		0010 1110	2E
601		0010 1111	2F
602		0011 0000	30
603		0011 0001	31
604		0011 0010	32
605		0011 0011	33
606		0011 0100	34
607		0011 0101	35
608		0011 0110	36
609		0011 0111	37
610	*	*0011 1000*	*38*

FREQ (MHz)		BINARY	HEX
U4 (011)			
760		0110 1110	6E
761		0110 1111	6F
762		0111 0000	70
763		0111 0001	71
764		0111 0010	72
765		0111 0011	73
766		0111 0100	74
767		0111 0101	75
768		0111 0110	76
769		0111 0111	77
770	*	*0111 1000*	*78*
U2 (010)			
830	*	*0101 1000*	*58*
831		0101 0111	57
832		0101 0110	56
833		0101 0101	55
834		0101 0100	54
835		0101 0011	53
836		0101 0010	52
837		0101 0001	51
838		0101 0000	50
839		0100 1111	4F
840		0100 1110	4E

2.4 PHASE ROTATION Programming (UHF SYNTHESISER and SAMPLER CLOCK)

Each UHF oscillator and sampler clock has an associated phase rotator which can have its output phase , first derivative (phase rate) and second derivative set at the start of each 5 second sync cycle.

There are four UHF phase rotators which are referred to in software as "L22A1' "L22B1", "L22A2" and "L22B2" and are found at locations AL403 , AL404, AL405 and AL406 where A is the antenna number.
These are controlled by the data set with address 23 (17 hex) and the full module address is therefore 17 03 , 17 04, 17 05 or 17 06. ?????????

There are four sampler phase rotators which are referred to in software as "L21A1", "L21B1", "L21A2" and "L21B2" and are found at locations AL503 , AL504, AL505 and AL506 where A is the antenna number.
These are controlled by the data set with address 24 (18 hex)and the full module address is therefore 18 03 , 18 04, 18 05 or 18 06. ?????????

The sampler phase rotator is identical to the UHF rotator and operates at 128MHz. Each degree of phase is equivalent to 0.0217 nSec. (1000/(128*360)). This is still true for 2 or 1 bit sampling since the frequency doubling automatically takes care of the necessary phase doubling. For example each nanosecond of delay requires exactly 46.08 degrees of phase for 1, 2 or 4 bit sampling.

The second derivative can be disabled (ie.set to zero) by setting a data bit to zero and both rate and second derivative can be disabled by setting another data bit to zero. This can reduce data transfer when these functions are not needed and also helps testing.

A checking facility is included to increase confidence in the operation of the phase rotator. Precalculated check data can be loaded into the phase rotator, along with the set - up data. Registers within the phase rotators are compared with this data at the end of each sync cycle. If an error is detected a single bit is flagged at the end of the cycle (only 6 phase bits are tested but this is sufficient for reasonable confidence). This bit is held latched during the next cycle.

PHASE

Phase can be set to any value over the full 0 to 360° range and requires an 11 bit number where the MSB is 0 for < 180 deg and 1 for ≥ 180 deg and the following 10 bits specify the residual phase value N (after subtraction of 180° if relevent).

N = Phase (degrees) / 0.18 = Phase (rads) *1000 / π

where $0 \leq N < 1000$ (excluding the MSB)
and **"Phase" means actual phase modulo 180°**

e.g. for 236 degrees Set MSB to 1 (since ≥180°) followed by
N = 56 / 0.18 = 311 and the binary number is 101 0011 0111.

For the samplers delay is varied by varying the phase at 128MHz with 0.18 deg. step size this is equivalent to a delay step size of 1/256 = 0.003906 nSec. For example 1nS delay requires 46.08 degrees and N = 46.08 / 0.18 = 256 or 001 0000 0000.
Note that when operating in the 1, 2 or 4 bit mode the phase ,rate etc. is automatically doubled or quadrupled to give the same delay ,delay rate etc. but always with the constraint of 0 to 360 degrees maximum at the actual clock frequency.

RATE

Phase rate can be set over the range - 2kHz to + 2kHz
(actually -1.999 to +3.333 kHz)
and requires a 25 bit signed number M (24 bits + sign) where -

$$M = 2^{26} * F / (10^4 + F)$$ and the inverse function is $$F = 10^4 * M / (2^{26} - M)$$

where $2^{-24} < M < 2^{24}$
and F is the <u>signed</u> rate in Hz (the sign bit is 1 for negative rate).

e.g. for +100 Hz fringe rate $M = 2^{26} / 101 = +664444$ and the required binary number is 00001010 00100011 01111100 with a 0 in the sign bit and 1 in the rate enable bit .

for -100 Hz fringe rate $M = -2^{26} / 99 = -677867$ and the required binary number is 00001010 01100111 00111011 with a 1 in the sign bit and 1 in the rate enable bit .

Note that this function is slightly nonlinear .
– Merely changing the sign is not sufficient to give -100Hz.

For the samplers a delay rate (eg. 1 nS per Second) must be converted to degrees per second at 128MHz and thence to frequency (eg. 1nS per Sec.= 46.08 deg.per Sec or 0.128 Hz.).

SECOND DERIVATIVE

This facility is normally only needed for the long baseline array or where the phase is updated infrequently (eg. where the sync cycle has been lengthened). When not needed it should be disabled by setting the enable bit to 0.

Second derivative can be set over at least a ± 2.4 Hz range (depending on the rate) and requires a **signed** 19 bit number K (18 bits plus separate sign).

$$K = C * 2^{43} / (10^4 (10^4 + F))$$

where C is the required 2nd deriv. (Hz per sec). The sign bit is 1 for a positive second deriv. - see later.
and f is the **signed** rate (Hz)

e.g. for + 0.01 Hz per sec. (at f = 100 Hz rate)
K = 871 (= 10 00000011 01100111 with a 1 in the sign bit and rate and second derivative enabled).

Note on signs

A positive value for phase will advance the phase of the UHF local oscillator in Bands L2 and U4. Similarly, a positive value of rate parameter F (ie. sign bit = 0) will increase the UHF LO frequency in these bands.

However the reverse is true in bands L4 and U2 due to a change in the conversion sign within this LO synthesiser module.

For all sampler clock frequencies a positive value will advance the phase and rate (ie. reduce the delay).

Second derivative signs are confusing and need care. A positive value for second derivative parameter C (ie. sign bit = 1) always gives an increase in the absolute value of F. The sign of K is therefore opposite to that of the required second derivative when rate is negative. K must therefore change sign at transit.

This can give problems when the second derivative goes through zero (e.g. at transit) unless C is set to zero for that cycle. A similar problem exists when rate goes through zero since the sign of the second derivative or rate cannot chan during a 5 sec sync cycle.

Notes on limits

For the worst case of an equatorial source, an east west baseline of 1000 km at 100 GHz (or 3000 km at 30 GHz), and one antenna of an interferometer pair not phase rotated, phase is required to vary by $\pm$ 2.1 $*10^9$ radians during a day.
Phase rate is required to vary to a maximum of $\pm$ 24.2 kHz and second derivative by $\pm$ 1.76 Hz per second. The sampler requires much lower values.

Start phase has no limit since N * 360° is equivalent to 0°.

The phase rotator has a limited range of phase rate (sufficient for > 300 km at 22 GHz). However this can be increased by offsetting the local oscillator rest frequency in steps of a few kHz (in the station common LO). Phase calibration must be carried out at every such step and so its use is limited to about once or twice per hour. It is worth noting that the phase rotator actually has - 2kHz to + 3.333kHz (ie. 5.3333kHz total) range but this must be used with caution sin on some bands this is inverted to become - 3.333 to + 2 kHz.

Second derivative range can not be extended - except possibly in hardware (removing a divider) but is sufficient for any forseeable need.

Notes on resolution

Phase steps (0.18 deg.) are made small enough to avoid generating unwanted sidebands due to phase modulation during rate stepping

Rate steps (0.2 millihertz or 0.07°/sec) give a maximum of $\pm$0.18 deg. phase error after 5 seconds and permit the cycle time to be increased to beyond 100 seconds before errors are excessive.

Second derivative steps (.00001 Hz per sec.) similarly give negligible errors in 5seconds. They also permit 100 second cycle times but only with short baselines or low frequencies (eg. 6 km and 50 GHz or 100 km and 3 GHz or lower) due to the lack of higher derivatives.

CHECK BITS

Whilst the phase rotator operates for typically 5 seconds minus about 10 mSec each sync cycle the phase rotates from S = start phase to F =final phase.

where $F = S + 10^4 Hz * 4.99 sec + Rate * 4.99 sec + SD * (4.99 sec)^2$

For example with 237°, +100Hz and +0.01 Hz/sec

F=237+ (49900+499+0.249) *360° modulo 360° =326.64 = 1<u>1100101</u>1111

Where F = (phase modulo 180°) / 0.18 as before.

This number can be precalculated and loaded into a latch for comparison with the actual phase at the end of the cycle. If the phase reaches the correct value a single bit line goes high.

Only the 6 bits underlined in the above example are tested (due to limited latch space) with the MSB and 4 LS bits not tested. Occasional errors are to be expected due to rounding errors (ie.±1 bit). If say 70% of cycles return a high check bit then this implies that all is probably well.

BIT PATTERN

The sub address within the phase rotator module is 1 to 4 ?????????

Address 1 16 bits (Hi/Lo byte) contains (MSB first)

Two MS bits of the check code
Two LS bits of the second derivative.
Rate enable bit (1 to enable)
Second derivative enable (1 to enable)
Second derivative sign (1 for negative)
Rate sign (1 for negative).
The first 8 bits of the rate

Address 2 contains the remaining 16 bits of the rate (LSB last)

Address 3 contains (MSB first)

The remaining 4 bits of the check code
A spare bit (set to 0)
The 11 bits of the phase (180° bit first)

Address 4 contains the 16 MS bits of the second derivative (MSB first)

2.5 GENERAL

Event generator - LO stop/run pulse

This pulse stops and then restarts the phase rotators and sets in the new frequencies. It also takes any module out of manual operation.
The event generator is required to give a logic signal which is Hi for the period during integration and remain Hi for a guard time of 1 millisecond after integration stops at the end of the 5 sec. sync cycle. , It must then go Lo and then 10 milliseconds later at precisely defined time T_r this line must go Hi again.
Tr is the time for which the rate and second derivative are calculated. It is 5 milliseconds before the the next integration starts. This gives the LO system time to stabilize. It assumes a blank time of 16 milliseconds.

On the falling edge the phase rotators stop, the new frequencies and phase rates etc are loaded into the working registers and the frequency changing sequence is started. On the rising edge the phase rotators are started from the new values.

Maint/Obs

??????????????????????????

F1/F2 Select

??????????????????????????

~~MIKE KESTEVEN.~~

3.1

~~2.6~~

A Quick Fault Finding Guide for the L.O. Racks.

~~(For modules delivered to the site before February 1990, only.)~~

Event Generator.

To easily check the Event Generator sense and operation, put L21or L22 in OBServing mode . After the internal MANual timer has timed out, the loops should normally be in lock, and go out of lock during every blanking period. — They will be out of lock for most of the time if the event generato twisted pair is reversed.

L2, L3, L4.

Pushing the MANUAL button should set the modules in lock.
(This confirms that the locking electronics are working, and the signals from the reference chain seem OK.)
If these modules go out of MANual whenever any single bit in the bin is accessed, then the modules are in MAINTainance mode. If the modules then go out of lock at this time, that would suggest that the frequency data the module is using is rubbish- either rubbish data from the ACC, or data has been written to FREQUENCY 1, but the FRSW line is telling the module to use FREQUENCY 2.

If the module is in OBServing mode, and the module will not apparently stay in MANual mode, the Event Generator lines are probably around the wrong way. (~~On new modules~~, the green LED on the L4 front panels should be normally out, and flash during each blanking period.)

If the module locks in MANual mode, but will not lock in OBServation mode, the same comments as above, about incorrect data, label or setting of the FRSW line apply.

If the modules do not momentarily go out of lock every blanking period, the ENAB line is effectively disabling the Event Generator to that module.

L21/L22 Modules.

The MANual mode takes precedence over OBServation or MAINTainance modes. Its duration in MANual mode is set entirely by the internal timer. After this times out, the module is the mode set by the MODe line (this can be tested as below).

In OBServation Mode, the loops should go out of lock every blanking period. In MAINTainance mode, the loops will go out of lock when the MRS line is in a (keyboard) 1 mode. In MAINTainance mode, the rotators start again when the MRS line is returned to a (keyboard) 0 mode.

27
3.2

OPERATION OF L.O. INTERFACES.

G. McCulloch.
16 January 1990.

This note describes the operation of the Data Set interfaces used in L.O. modules. It applies to the following modules:

L21, L22	Phase rotators.
L2	U.H.F Synthesiser (parts of 512-840 MHz., in 1 MHz steps.)
L3	2GHz. (L/S) Synthesiser (1815-2220 MHz., in 10 MHz. steps.)
L4	7GHz. (C/X) Synthesiser (6710-7690 MHz., in 320 MHz. steps.)

Modules L31, L32, L33 and L1 do not contain interfaces, although, like the above modules, have a Module Address Board (see below for description).

As far as possible, the method of operation, and the conventions, are carried on throughout all the modules, although, as can be expected, there are differences as required by the functions of each module type.

NOTE: The terminology adopted for this description is that LO and HI refer to a real TTL voltage level (<0.7 V and >2.0 V respectively). To set a data set COMmand line HI requires a keyboard request of a 0, and a MONitor request which returns a 0 indicates that the line is in the HI state. When a data set is reset and initialized, all single bit COMmand lines are in the HI state.

DATA SETS.

Each L.O. rack uses three D3 Data Sets, one in each horizontal bin, arranged as follows:

Bin 3, D/S address 22, controls and monitors 2 x L4, 2 x L3 and 1 x L33.
Bin 4, D/S address 23, controls and monitors 4 x L22, 4 x L2 and 1x L32.
Bin 5, D/S address 24, controls and monitors 4 X L21, 2 x L1 and 1 x L31.

Data can be written to a module from a data set at any time. L21 and L22 can only store data which will be used during the next integration period. L2, L3 and L4 can hold two sets of data, called F1 and F2, and either set can be selected for use during the next integration period.

The whole L.O. rack uses a single Event Generator signal. Each data set generates a SBDRDY pulse every time any single bit command line is changed. This SBDRDY pulse is connected to every module in a bin.

Data Input Format.

The data set's 6 bit address bus (BADD) and 8 bit data bus (BDAT), along with the WR/RD, HI/LO and STRobe lines, are used to enter observing parameters into the interface of a module. BADD0..3 are used to specify which module is being addressed, and BADD4,5 are used to specify the type of data being entered, as shown below.

L21, L22 Modules.

BADD4 and 5 are used as follows:
00 is for the 16 most significant second derivative data bits.
01 is for the 11 start phase bits and the lower 4 check bits.
10 is for the lower 16 bits of the rate data.
11 is for the upper 8 rate bits, sign bits, two least significant second derivative bits, , two most significant check bits and rate and second derivative enable bits.
(See ACY's "L.O. Specifications." for the full details.)

L2, L3, L4 Modules.

BADD4 is used a follows:
0 is for entering Frequency 1 (F1) data.
1 is for entering Frequency 2 (F2) data.

BADD5 is not used, and has no effect.

The output frequency of a module, F1 or F2, is selected by the Frequency Switch (FRSW) single bit command. LO for Frequency 1, HI for Frequency 2.

Module Address Board.

All modules have a small Module Address board. To enable any module (of the correct variety) to be plugged into any position in the array, without having to preset any address switches, the address of a position is determined by a four bit code which is hardwired to the backplane of the bin. This code is picked up when a module is plugged in. It is compared with BADD 0..3 by the address board, and produces a version of the strobe called the Decoded Strobe. This signal is the strobe used within the module. BADD 4,5 are used for the address of registers within a module, e.g. for start phase and phase rate, or for frequency 1 and frequency 2. The Module Address board also has an eight bit word which can be read via the address and data buses. BDAT 0...5 contain the serial number of the

module, and BDAT 6,7 contain the version type of the module. Serial numbers for each type of module start from 1. (00_H would indicate that the serial number of a module has not been encoded, and FF_H would indicate that a module has not been plugged into that position). The version is set by links which can be easily changed. (The version code is intended to be used to identify different hardware versions of a particular module type. Should a module be changed, which then necessitates a different control or monitoring procedure, the module can be given another version number. The computer software would then able to interrogate each module, determine the version of hardware it contains, and then use the correct procedure for that module.)

The board also has an open collector gate which is connected to a single bit MONitor line called the Bin Wired Or (BIN#WROR)[1] line. Each data set has one Bin Wired Or line. This is a dedicated single bit line, which is intended to be checked by the data set every integration period, as a quick method of indicating that all modules are in the observing mode, and probably working properly. If one or more modules in a bin either has a loop out of lock, or has been set into other than OBServing mode (see later), then this line will be pulled LO. At the same time, at least one single bit MONitor line will also be pulled LO, enabling the reason for the alarm to be determined.

Explanation of the Modes of Operation.

All modules (except L1, L31, L32 and L33) have three modes of operation- MANual, MAINTainance and OBServation mode.

The OBServation mode is the usual observing mode for the module. This mode requires an Event Generator pulse to indicate the beginning of each integration period. The presence of this pulse can be seen on the front panel of L4 modules- the green "EVENT" LED will flash briefly with every Event Generator pulse. It should be off during each integration period.

The MAINTainance mode is intended for operating a module via the dataset and computer, especially at Culgoora, where it could be operated from the control building to check on the module's operation, if a fault is suspected, or to narrow down the area of a fault before removing a module from service. The observing software would be made aware that the module had left its control, and that any data collected from that telescope would be corrupted. Under MAINT mode, complete control of the

[1]Replace the # with the Bin Number i.e. BIN3WROR is the Bin Wired Or line associated with the modules in Bin 3 .

module is possible. In this mode, an Event Generator pulse is not required, and any pulses it receives are ignored.

MANual is intended to be used for testing on the bench, or as a quick functional test of the R.F. sections of a module on a telescope, to determine if it is probably working properly. It is independent of the data set. It overrides which ever other mode the module may have been placed in. It is selected by pushing the blue button on the front panel of a module.

N.B. For the MANual mode on modules L2, L3 and L4 to function properly, the Event Generator must be in its normal (observing) state. This can be easily ascertained- the Event Generator is in the required state if the green LED on L4 modules is off. The state is irrelevant for MANual mode in L21 and L22.

From MANual mode, L21 and L22 modules return to OBServation or MAINTainance mode immediately after an internal timer has timed out (approximately 12 seconds). L2, L3 and L4 modules are returned to their previous mode by the next Event Generator or SBDRDY pulse. See later for more details.

Using the Operating Modes.

MAINTainance or OBServing mode is determined by a single bit command MODe line. Setting this HI will place the module in OBServing mode, and LO in MAINTainance mode. For L21, L22 modules, the mode change occurs immediately. For L2, L3 and L4 modules, if the MODe line is changed from HI to LO, the module will immediately go into the MAINTainance mode. When the MODe line is taken from LO to HI, the module will only go into the OBServing mode after the next Event Generator pulse.

Observing Mode.

This is the normal observing mode. The MODe command line is HI, the OBS monitor line is LO and, assuming that the loops are in lock, the BIN#WROR line for each data set is HI. Data for the next integration period may be written to each module at any time, but will (usually) only be acted upon on the Event Generator pulse at the start of the next integration period. Should a loop be out of lock, the BIN#WROR line will be LO, and a LOK single bit monitor line will be LO, enabling the faulty loop to be identified.

L21, L22 Modules.

In OBServing mode, these modules take up the new data every time the Event Generator line pulses.

L3, L4 Modules.

In OBServing mode, these modules normally go through their complete retuning procedure every time the Event Generator pulses. This means that they break lock, the oscillator is swept to the top of its tuning range and back down to the new frequency, and then relocked. All this takes about 10 mSec. If it is thought desirable to avoid this continual retuning (for example, if phase lock is uncertain or phase jumps are suspected), then the single bit command called ENAB (Enable Next Event) may be used. This line should normally be left HI, but if it is brought LO, the Event Generator to that particular module will be effectively disabled. (Caution. If this is done, it will be impossible to tune the oscillator to another frequency until this line is again taken HI. Note that it is possible, using some of the analog monitor points, to *estimate* the present frequency of these modules and therefore confirm that the frequency has changed, but we would not expect this to be done routinely during observations.) One special case concerning the ENAB line exists, and this is explained under MANual mode.

Changing the FRSW single bit will not have any effect until after the next (enabled) Event Generator pulse is received.

L2 Modules.

These modules are also equipped with an ENAB (Enable Next Event) line. Every time the Event Generator operates, one loop is unlocked and relocked. If it is thought desirable to avoid this continual retuning (for example, if phase lock is uncertain or phase jumps are suspected), then the single bit command called ENAB (Enable Next Event) may be used. This line should normally be left HI, but if it is brought LO, the Event Generator to that particular module will be effectively disabled. (Caution. If this is done, it will be impossible to tune the oscillator to another frequency until this line is again taken HI. Note that on these modules, it is very difficult to estimate the present frequency using the analog monitor points, and therefore to check that a frequency change has occurred.) One special case concerning the ENAB line exists, and this is explained under MANual mode.

Changing the FRSW single bit will not have any effect until after the next (enabled) Event Generator pulse is received.

Maintainance Mode.

This mode enables the whole module to be operated via a data set. It is intended for checking a module's performance remotely, for performing engineering tests on a particular module, or for investigating the effect of a particular module's operation on some part of the system. New data may be written to any module at any time.

The MODe line is brought LO. This brings the BIN#WROR line LO, and sets the OBSMON line HI.

L21, L22 Modules.

In the MAINTainance mode, the MRS (Maintainance Run Stop) line replaces the Event Generator to stop and restart the rotators. It is normally set HI. To run the phase rotators requires two single bit commands. The particular MRS line is first set LO, which stops the rotators and latches in the new data. It is then returned HI , which sets them off again. While this line is LO, the loop within the module will be out of lock, and the red LED on the front panel will be on.

L2, L3, L4 Modules.

When these modules are in MAINTainance mode, the Event Generator pulse is replaced by the SBDRDY pulse from the data set. (Note. Because this pulse is generated every time any single bit line from the data set is commanded, and the same SBDRDY line goes to every module in a bin, changing a line for one module could cause unexpected changes in other modules in the same bin, which are in MAINTainance mode.)

Two sets of frequency data (F1 and F2) may be stored in the module, and selected by the FRSW command. If the module is required to be set to a new frequency, then the data must be first written to the module, and then the frequency must be asked for, using the single bit line, FRSW. (FRSW is set LO for F1 and HI for F2). This is to generate the SBDRDY pulse required for initiating the retuning process.

Manual Mode.

In all modules, this is accessed by pushing the button on the front panel. The red "MANUAL" LED will light.

The data which is used for MANual mode is independent of any other data which may have been entered into a module.

L21,L22 Modules.

The BIN WIRed OR line will be pulled LO and the OBS mon line will also be pulled LO while the module is in this mode.

The data for the manual mode is hardwired on the interface board, and cannot be changed. Pushing the button loads this data into the phase rotator, and starts its operation. The duration of the time a phase rotator is in this mode is set by an internal timer (approximately 12 seconds), and while in this mode, the red LED on the front panel will show. The prewired data causes the rotator to start at a high phase rate, and to decelerate to a final phase of about 12 degrees. The output phase of the rotator can be measured using the analog phase meter, which is available on the front panel of the module. (12 degrees is equivalent to 0.34 volts.)

Although the MANual LED is now off, the BINWROR line has returned HI and the OBS monitor line has returned LO, the module will stay at 12 degrees until the next Event Generator pulse (if it is in OBServing mode), or toggling of the MRS line (if it is in MAINTainance mode). It will then use the data previously written into its internal latches.

ALTHOUGH THE MANUAL LED IS NOW OFF, THE BIN WIRED OR ~~AND~~ IS STILL LO AND THE OBS MON ? IS HI UNTIL THE NEXT EVENT GEN. PULSE

L2, L3, L4 Modules.

The BIN WIRed OR line will be pulled LO and the MANual MON line will also be pulled LO.

Data for the manual mode is set by sets of internal switches on the interface board. Most of the data is set by rotary , binary encoding switches. However, some of the data is set by slide DIP switches. See ACY's "L.O. Specifications" for information about the settings as a function of frequency.

If the MODe line is set HI (OBServing mode), the module will remain in MANual mode until the arrival of the next Event Generator signal. If the MODe line is LO (MAINTainance mode), it will remain in MANual mode until the arrival of the next SBDRDY pulse.

If the data set on the switches is changed, it will be necessary to push the MANUAL button again, for the module to respond to this new data.

The special case mentioned earlier is when a module is in OBServation mode and the ENAB line is LO. The MANual button is then pushed. It will go into MANual mode immediately, with its output frequency being determined by the internal switches. The next Event Generator pulse will *not* be ignored, but will put the module back into OBServing mode. Subsequent Event Generator pulses will, however, be ignored. Its output frequency will determined by the FRSW line, and the data contained in the data latches.

NON IDEAL BEHAVIOUR

The ideal Local Oscillator (LO) is a perfect sinewave of exactly known phase. The AT local oscillators have been designed to approach this ideal but there are inevitably errors. The errors of consequence are: spurious signals, phase drift, phase noise, harmonics and amplitude errors, (roughly in order of decreasing importance).

4.1 SPURIOUS SIGNALS

(a) Radiated

Any LO signal from a YTO, VCO or a 'comb' or mixer product can 'leak' from the LO system and reach the ultra sensitive AT receivers and interfere with the desired astronomy signal. All LO signals with components above 20 MHz are carried in solid copper coaxial cables and tightly sealed 'RF boxes'. At the higher microwave frequencies very small amounts of LO signals still leak from the RF boxes and connectors and the modules themsleves provide an additional high level of shielding in L3 and L4. Wire mesh gaskets around the module joints and heavily filtered 'feedthroughs' on all dc lines provide very effective shielding. Of course, once the reqired LO signal leaves the modules it can leak from an imperfect connector (or backwards up through the conversion mixers etc) and into the LNAs. To reduce the effect of such leakage, the conversion system was designed so that the LO frequencies always lie outside the receiving bands.

It is very difficult to test for leakage since the total AT system is much more sensitive than any test equipment. In summary, It is wise to keep all lids tightly screwed on without leaving any screws out.

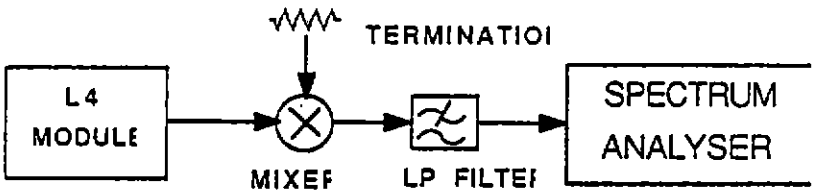
(b) Conducted

Most commercial synthesisers have non-harmonic spurious signals at least 60dB below the wanted signal. Tests on prototype receivers showed that even when spurious signals were 120 dB down they could still be harmful in the AT system. However, spurious signals close to the LO signal result in a conversion system IF product which is outside the IF bandwidth and are therefore less of a problem. For example any of the comb generator signal in L4 reaching the 7 GHz output line will result in low level spurious signals spaced every 320 MHz. A spurious signal at 5.5 GHz on a 7 GHz LO signal will mix in the conversion system to give a 1.5 GHz IF signal which is within the IF filter band. An extensive development effort was necessary to approach the -120 dB level. The gain and noise figure of the phase detector IF amplifiers were improved to allow operation at the lowest possible 'comb' level. Filters were then added in the internal mixer

6. This shows diagram

input lines to remove the most damaging spurious frequencies. A two stage isolator in L4 and a single isolator in L3 reduce the levels still further.

A spectrum analyser cannot directly measure such low spurious levels in the presence of a high LO signal. A notch filter could remove the LO carrier and improve the situation. A better solution is to feed the LO signal into a mixer with the rf port terminated and put a spectrum analyser on the IF output and look for signals within the IF bandwidth. This models the actual conversion system and reveals problems due to high order mixer products that can easily be otherwise overlooked. The diagram below show a typical layout.



In summary, LO spurious signals need to be 120 dB below the LO signal in many parts of the spectrum and this can be quite difficult to measure.

4.2 PHASE DRIFT.

A synthesis telescope is essentially a receiving phased array and requires that all L.Os be tightly controlled to preserve phase accuracy. Every so often (20 to 60 minutes typically), the phase of each antenna is 'calibrated' by looking at a reference object in the sky and comparing the received phase to the calculated phase. Between such calibrations, LO phase should be as stable as possible. A slow linear phase drift is not too serious since it can be removed by this calibration process. However, random phase changes or cyclic variations (e.g. phase shifts caused by air conditioner temperature cycling or sun and wind effects) must be less than the phase changes caused by atmospheric effects on the received astronomy signal. Studies at the VLA show that for baselines of several km, the received signals undergo a delay through the atmosphere and that the total effective path length varies by typically 1 mm RMS in the timescales of 1 minute to 1 hour. This is for a high dry site in better than average conditions. Narrabri is likely to be at least as bad as this. 1 mm is equivalent to approximately 1 degree RMS at 1 GHz and 10 degrees RMS at 10 GHz. Drifts, random changes and cyclic phase variations within any receiver/LO system should be no greater than this so that ultimate performance is limited by the atmosphere and not by equipment limitations.

During development, most components were tested for temperature drift and this was a major factor in the selection of design approach and components

Don't replace page since I have over/ref.

(eg. phase detectors, amplifiers, doublers and filters). A large part of the phase variations in the LO system will be due to the LO reference distribution from the central site over coaxial cable. This will be largely calibrated out by the round trip line stabiliser system.

In summary, LO phase variations should be kept below ± 1 degree (per GHz of LO frequency) so that total antenna phase noise is below 1 degree RMS per GHz.

4.3 PHASE NOISE

to do

4.4 HARMONICS

LO harmonics will result in unwanted conversion products that can interfere with the wanted IF signals. Many oscillators have 2nd and 3rd harmonics in the -15 to -30 dB range where at least -40 dB is necessary. This is th reason that most LO modules have low pass filters in the output lines. This results in harmonics typically wll below -60 dB. This is easily checked with a spectrum analyser provided the instument is not driven too hard, since harmonics are easily regenerated within the spectum analyser itself.

4.5 AMPLITUDE ERRORS

(a) Amplitude modulation (AM). 50 Hz AM is extremely small in all YTO, VCO and VCXO loops within the AT since the power supplies are highly regulated. All YTO and VCO oscillators have a power supply sensitivity of around 1 dB per volt and the power supply ripple is less than 1 mV. AM can also be generated by an interfering signal and the worst case of this is the 128 MHz signal which is generated by mixing rather than in a PLL. This results in several nearby signals with a level around -30 dB below the main signal. This gives 8 MHz amplitude modulation of less than 1 dB. All other LO output signals should have negligible AM.

(b) Amplitude change with frequency.

All oscillators will give an output level which has some variation as the frequency is changed. Amplitude variation will move the conversion mixer drive level away from the optimum value and the aim is to keep this within ± 1dB. Amplitude drift with temperature and age should be less than 1dB. If any of these effects prove to be excessive then L2, L3 and L4 have provision for the retrofit of a level-trim computer input.

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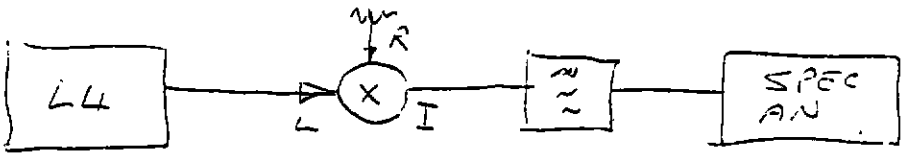

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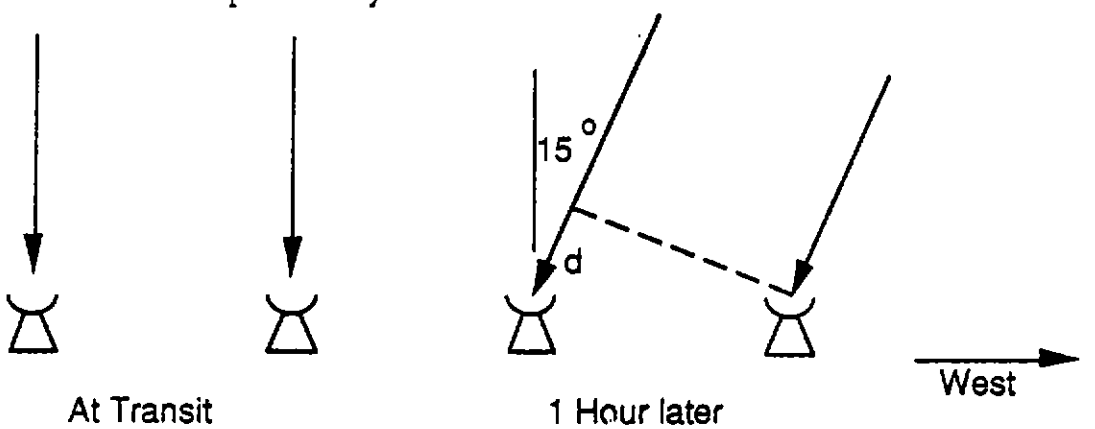
Phase Rotation and Delay Stepping.

This note outlines the reasons for phase rotation and delay stepping and describes some of the techniques used, with emphasis on the approach used in the Australia Telescope.

As the earth rotates, the astronomical object being observed (e.g. star, galaxy, quasar - all of which will be referred to as a 'source') appears to move across the sky with one revolution per day (15 degrees per hour or 0.25 degrees per minute). As a result, there is a continual change in the relative propagation path lengths from the source to each antenna. For example, consider an interferometer using two antennas separated by 1 km.



When the source is directly overhead, there will be exactly equal path lengths from the source to each antenna. However, the relative path lengths are continually changing and, after 1 hour, one path will be longer by 260 metres (i.e. d = Sin 15° • 1 km). When directly overhead, the relative path length is changing at the maximum rate, which is:

73 mm per second (per km of baseline).

This is for the worst case for a source passing directly overhead, with an east-west interferometer sited on the equator. For any other geometry, the rate of change of path difference is always lower than this (as given in the appendix) with the rate of change reducing to zero for a star which is at the south celestial pole.

Since the velocity of light is 300mm per nS, the maximum rate of change of time delay T between the same signal reaching the two antennas is:

0.243 nS per second (per km of baseline).

A path difference of 1 nS means that there is a phase difference, between the

antennas, of 360° at a frequency of 1 GHz. Therefore, if the path difference changes at a rate of 1 nS per second, this gives a phase change rate of 360° per second (or 1 Hz) at 1 GHz. The maximum so called 'fringe' rate (or phase rotation rate) is then:

0.243 Hz for each GHz of receive frequency (and each km of baseline).

For example, with an interferometer separation of 4.1 km, the maximum delay rate is 1 nS per second (3.6 μS per hour) which corresponds to a fringe rate of 10 Hz at a receive frequency of 10 GHz.

To be able to correlate the signals from two antennas, this fringe rate must be removed, otherwise the rotating phase will result in a much reduced average correlator output. As a rough guide, a 26 degree linear rotation (±13°) during an integration period, reduces the correlation by around 1%, whereas a 180 degree rotation gives a decorrelation loss of 35%. Since the previous example with a 4.1 km baseline gives 10 Hz at 10 GHz, or 3600° for each second of integration, it is clear that the phase rotation must be removed.

Removal with a phase shifter

Consider the case of an antenna separation of 4.1 km and a receive frequency of 500 MHz. The delay rate (worst case) is 1 nS per second and it is therefore necessary to remove 180° of phase delay, each second at 500 MHz. This can be achieved by a suitable, continuously-variable phase shifter in the incoming line (or phase rotator in the local oscillator).

However, if the receiver has a bandwidth of 100 MHz (e.g. 450 to 550 MHz), then it is necessary to remove only 162° for a component at 450 MHz and 198° at 550 MHz. This is because, for a given delay, phase shift is proportional to frequency. However, if a simple phase rotator is used to remove this phase rotation, then this will remove the same phase shift at all frequencies. The remaining 18° per second rotation (90 degrees during a 5 second integration) at the band edges will result in a decorrelation loss of 10 % at these edges. The situation degrades rapidly with increasing integration period and for larger bandwidths. In the early days of interferometry with small bandwidths and small baselines, this problem was not as severe.

Removal with delay stepping

Removing the **delay** change rather than the resultant phase change is the more correct approach. This is usually achieved by placing a variable,

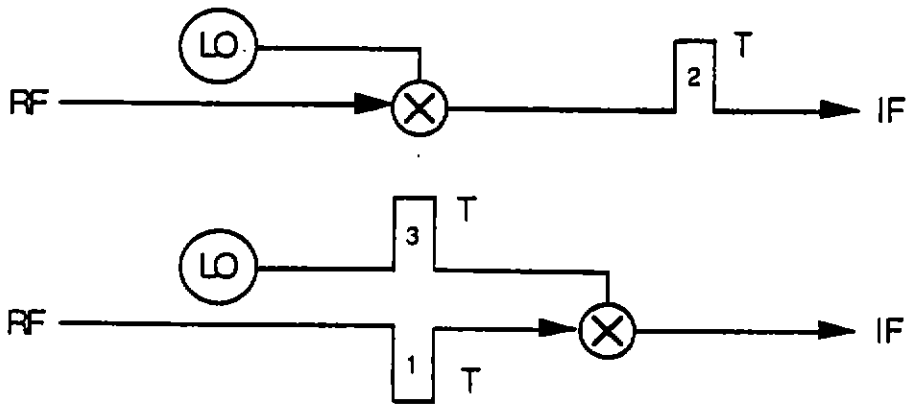
compensating delay within the antenna which has the shortest propagation path length. However, with high frequency, wide band receivers, this is difficult to achieve in the incoming signal path and it is usual to place the delay unit after down-conversion. A down-conversion system subtracts a stable, reference 'LO' frequency from the incoming frequency to produce a lower 'IF' frequency. It is much more convenient to place the delay compensation element in the IF signal path, rather than in the RF input path. However, simple delay is then no longer all that is necessary.

Consider the previous 500 MHz interferometer example, where an extra 1 nS (per second) delay is required within the antenna which has the shortest propagation path length. As before, this corresponds to 180° per second at 500 MHz (also 162° at 450 MHz and 198° at 550 MHz). If the IF is centred at a frequency of 100 MHz (i.e. LO = 400 MHz and IF from 50 to 150 MHz), then a 1 nS extra delay (each second) in the IF changes the phase by only 36° at 100 MHz and this is clearly insufficient to cancel the incoming 180° phase.

If 5 ns extra delay is inserted instead, then this produces the required 180° at the band centre, but produces 270° at the 150 MHz band edge (corresponding to 550 MHz input) instead of 198°. The only way to totally remove the extra phase delay is to use a combination of phase rotation and delay correction (unless the delay is at the incoming frequency and this is rare).

Combined phase rotation and delay stepping

An useful way of looking at this is to consider the two situations below where each case has a simple conversion with equivalent delays inserted.



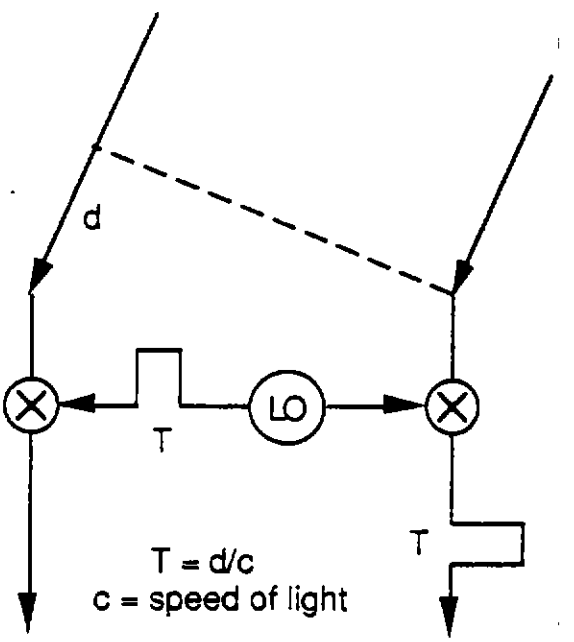
The first case has a single delay in the IF line, whereas the second case has delays in both RF and LO lines. In both cases the IF output is delayed by time T, since

delaying all input signals is equivalent to delaying the output signal. If one antenna has the first structure and the second antenna has the second structure, then the output will be delayed by the same amount, over the full bandwidth.

Therefore a propogation delay T (labelled 1) in the RF of the second antenna can be cancelled by an IF delay T (i.e. 2) in the first antenna **plus** a delay T (i.e. 3) in the LO of the second antenna. The delay in the LO of the second antenna is required to ensure that, in both antennas the LO and RF signals enter the mixer with the same **relative** phase. Without this, the different frequency components of the IF will be out of phase between antennas, leading to a loss of correlation.

Since the LO is a single cw frequency, an LO delay difference between antennas is **exactly** equivalent to a phase shift in one of them. A phase shifter can therefore be used in the LO line instead of a variable delay without error. This is usually a far simpler alternative. However the phase delay of $T * 2 * \pi * f_{LO}$ radians must be recalculated each time the LO frequency is changed but this is not very difficult.

The delay correction in the IF path should be exactly the extra delay T needed by that antenna to equalize the different propogation delays. The local oscillator phase must then be delayed by this same amount T (but in the other antenna).



The example with f_{REC} = 550 MHz and a fringe rate of 0.5 Hz (1 nS per second) may have one or more conversions to a final IF of 100 MHz where the delay unit operates. The phase of the local oscillator (or IF) must then be rotated by a continuously varying phase shifter (often referred to as fringe, lobe or phase

rotators). With a 400 MHz total LO this must be performed at the rate of 0.4 Hz or 144° per second (1 nS per second at 400 MHz). Obviously, if the receive frequency is 5 GHz, then the phase rates must be proportionally higher.

General comments

The phase shift in the local oscillator can be obtained with either an analog phase shifter, or as part of a phase lock loop. The use of phase lock loops in the local oscillator opens the way for highly linear, well controlled phase shifting techniques based on digital circuits. The AT phase rotator is an example of this and its operation is described in the relevant manual.

The delay correction in the IF path can be performed by switching in sections of delay line or by other analog delay circuits but these schemes are far from ideal. However, if the IF signal is ultimately sampled and digitised then simple digital shift registers can be used as delay lines. The only inherent limitation of digital delay lines is that the minimum delay step size ΔT is fixed and equal to the sampler clock period. A sampler clock at 200 MHz gives a minimum delay step $\Delta T = 5$ nS. If the bandwidth is 100 MHz as before, then there is up to ± 2.5 nS delay error and this will produce 50 MHz * 2.5 ns * 360° = 45° at the band edges at ± 50 MHz. Fortunately, small delay corrections (up to $\pm 1/2$ clock period), referred to as fractional-bit delays, are easily applied by adjusting the phase of the sampler clock and thus changing the sampling time as a result. The phase of the sampler clock is changed in exactly the same way as the phase of the local oscillator.

Digital delay lines consist of specialised shift registers. Moderate values of delay, referred to as fine delay, are applied directly to the sampler output (after it is received at the central building in the AT). The bit stream is then converted to a 32 bit parallel bus with each line operating at a slower speed. The majority of the delay, referred to as coarse delay, is then applied to these lines using highly integrated devices at this slower speed. In the AT, a total coarse delay of at least 10 μS, equivalent to half the maximum 6 km baseline is needed in each antenna path. A maximum fine delay of at least 32 bits or 125 nS is required and the fractional bit delay ranges up to 4 nS in steps of 0.004 nS (all with 256 MHz sampling). For more details refer to the relevent delay unit manual.

The phase and delay rates are not a constant value with time but are cosine functions of time as shown in the appendix below. The values for the

setting of the phase rotators and delay lines must therefore be updated very frequently. For very long baselines this can present a problem and the AT phase rotators have the ability to accept a varying phase rate (second derivative of phase, or phase curvature) to permit much longer intervals between phase rotator settings. Details of this are in the relevant manual.

In the previous examples the antenna without the internal delay line is referred to as being at the 'delay centre'. This assumed that one antenna is fixed and the other has a variable delay line. However, it is more common to have delay units in all antennas and this allows the delay centre to be set to the most convenient point and this may be between antennas, for example. This requires that some antennas can have delay removed rather than added and so there must be a long initial internal delay. Of course the above discussion is easily extended to the case of many antennas by regarding each pair in turn as an interferometer.

APPENDIX

The phase difference (in radians) between a signal arriving at an antenna and a reference point (e.g. another antenna) will be given by:

$$\phi(t) = \{ \sin\partial \sin d + \cos\partial \cos d \cos (H(t) - h) \} * 2\pi D / \lambda$$

where D is the distance from the antenna to the reference point, H is the hour angle of the centre of the source (field centre), ∂ is the declination of the source centre, h is the hour angle of the vector joining the antenna and the reference point, d is the declination of this vector and λ is the wavelength of the received signal.

The fringe rate is the rate of change of phase with time:

$$d\phi/dt = dH(t)/dt * \{ \cos\partial \cos d \sin (H(t) - h) \} * 2\pi D / \lambda$$

where the angular rotation rate of the earth (in radians per second) is:

$$dH(t)/dt = 2\pi / (24 * 60 * 60) = 7.27 * 10^{-5}$$

The maximum fringe rate will occur when d and ∂ are both 0° and H(t) - h is 90° (the source directly above the antenna) and is given by:

$$d\phi/dt \text{ max} = 7.27 * 10^{-5} * 2\pi D / \lambda$$

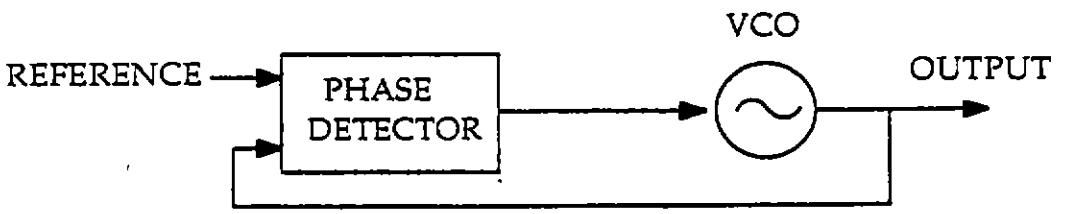
For the AT 6 km baseline, observing at 100 GHz, the maximum fringe rate would be 914 radians per second (145 Hz).

PHASE - LOCK LOOPS

4.1 FUNDAMENTALS

Phase-lock loops are widely used to clean up noisy signals (filter function), to decode FM signals (demodulator function) and to generate new frequencies (synthesiser function). The AT Phase-lock loops are almost all of the latter (synthesiser) type where the reference for the loop is a stable, unmodulated, low-noise, high-level signal. This primer is intended to show how the loops within the AT work and why certain approaches were chosen.

The simplest phase-lock loop (PLL) contains an internal oscillator which is locked in phase to an external reference signal such that the internal oscillator has exactly the same frequency (unlike an AFC loop) and the same phase as the reference signal, usually to within better than a few degrees. Only 2 components are essential: an electronically tunable oscillator (eg. a VCO) and a phase comparison device (phase detector).

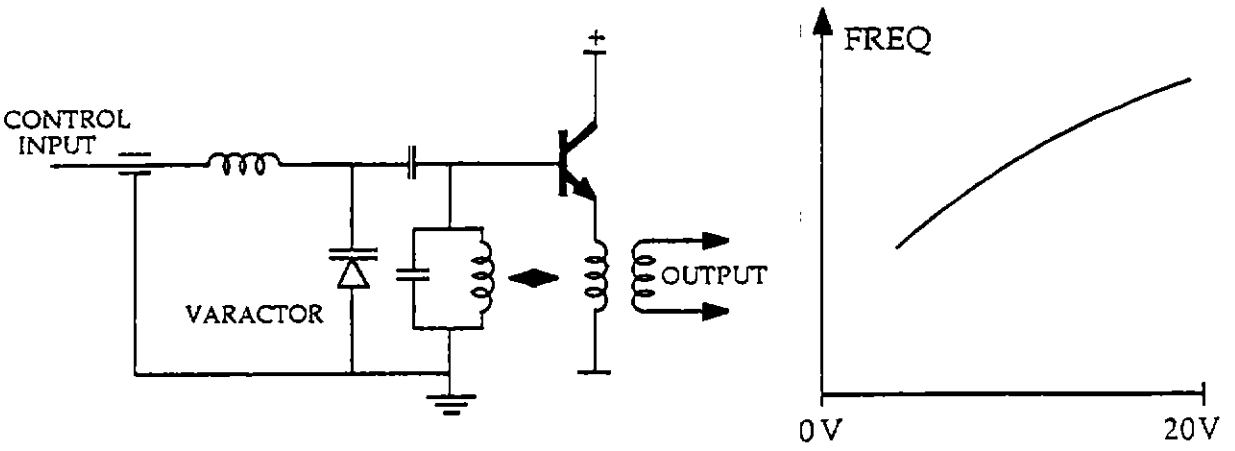


The Electronically Tunable Oscillator

Any oscillator (e.g. microwave cavity, LC tuned, stripline or crystal) can be electronically tuned by the addition of a voltage variable capacitor (or inductor). There are three common types and these are: voltage-controlled oscillators (VCOs), voltage-controlled quartz crystal oscillators (VCXOs) and YIG-tuned oscillators (YTOs - see separate section).

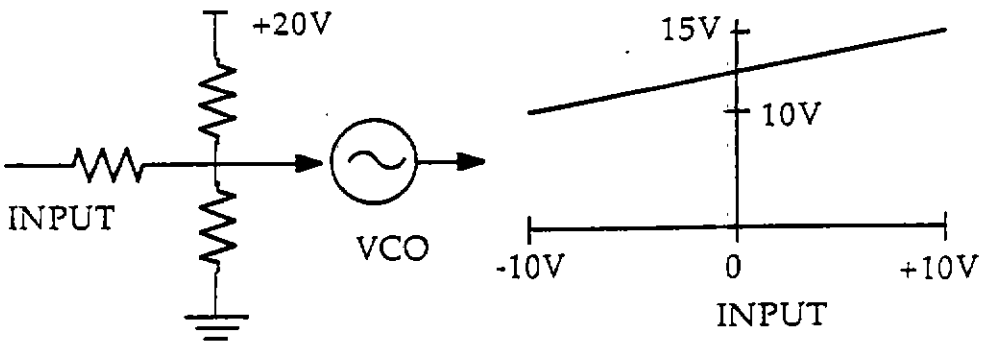
Most VCOs use variable capacitance diodes (varactors) which, when the reverse bias is varied, have a capacitance which varies over typically a 4 to 1 range. The varactor is used with a fixed inductor, microstrip line or cavity etc. to give a variable tuned circuit which is used as the frequency determining circuit within the oscillator. Since the varactor is reverse biased it behaves like a low loss capacitor and it appears as an open circuit to the control input.

In order to avoid any leakage of the rf oscillator signal back along the d.c. control line, there is usually a hefty filter in this line within the oscillator and this can have a major effect on loop stability as described later.



The circuit above shows a 'bare bones' VCO circuit illustrating the method of voltage control using a varactor diode and a typical control function. The voltage range is not centred about zero volts but typically runs from +2 to +20 volts. In PLL terminology the slope of this curve is represented by the variable K_o in frequency (radians per second) per volt of control input.

The majority of commercial VCOs tune over a 2 to 1 frequency range and the frequency increases with a more positive voltage (+ve K_o) although some VCXOs are reversed. The AT local oscillators often require a more modest tuning range and since most d.c. amplifiers give out a symmetrical ± 10V, an external attenuator and level shifter is used in the control line. This usually takes the form shown below. The attenuator changes the tuning slope K_o and for all YTOs and VCOs in the AT, this results in a tuning sensitivity of 1 MHz per volt ($K_o = 2\pi \cdot 10^6$). Attenuators and level shifters are not used with VCXOs which have a symmetrical tuning slope of around 1kHz per volt (except in L42 where a special VCXO has approximately 1Hz per volt).



The AT uses voltage controlled LC oscillators (VCOs) made by Vari-L at:
40 to 50 MHz (L2), 510 to 840 MHz (L2) and 512 MHz (L1)
Voltage controlled Crystal oscillators (VCXO) made by Greenway at:
8 MHz (L21), 10 MHz (L22) and 9.99 MHz (L31)
with a special low noise VCXO made by Vectron at 5 MHz (L42)
and YIG tuned oscillators (YTOs) made by Avantek at:
1815 to 2215 MHz (L3) and 6710 to 8010 MHz (L4)

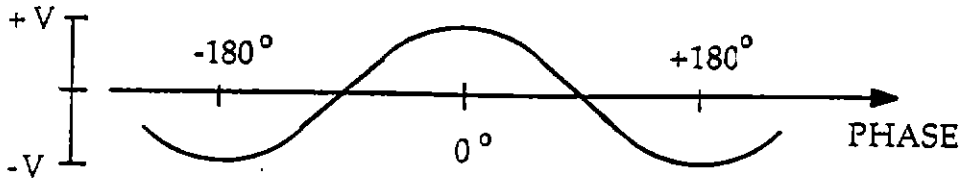
They are all commercial oscillators since a considerable development effort is required to produce reliable wide range tuning without spurious frequency jumps, latchups or sidebands (even some of the AT commercial VCXOs sometimes give these problems). All AT oscillators have an output of at least 10 milliwatts.

The crystal oscillators differ from the VCOs in that the tuning range is very narrow (e.g. ± 5 kHz in L22, ± 1 Hz in L42) due to the high quartz-crystal Q factor. They are usually arranged so that the tuning voltage is bipolar (centred around 0 volts) and often have a negative K_o.

The YIG tuned oscillators (see separate description) are highly linear, wide tuning range microwave devices. Since they are magnetically tuned by means of a field coil, they require a tuning current rather than a tuning voltage. A voltage to current converter is therefore usually found in association with them. All YTOs in the AT have both a coarse tuning coil and an 'FM' coil for loop control fine tuning.

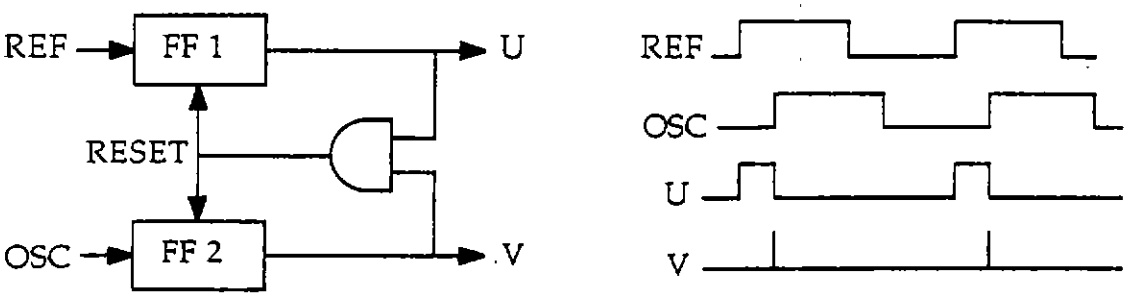
The Phase Detector.

A phase detector can be any device that produces an output as a function of the phase difference between two input signals. The simplest phase detector consists of a dc coupled mixer (see separate section) since the d.c. voltage output from the IF port is a simple function of the phase difference between the RF and LO inputs. For a double balanced mixer (e.g. TFM-1), this is typically a cosine function as shown below.

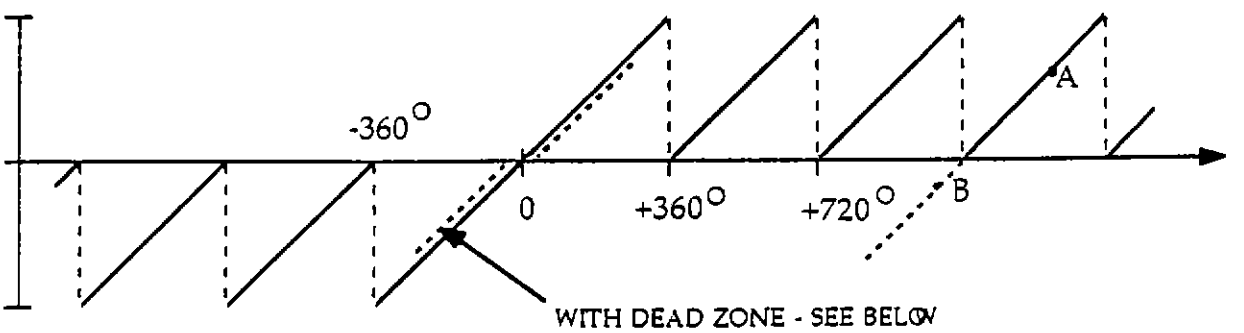


The resistance of a phase-lock loop (PLL) to being knocked out of lock or slipping cycles is dependant on the extent of the slope each side of the zero crossing. Since this is only ± 90 degrees (ie. 0 to 180°) in the previous figure, the AT does not use this form of phase detector. There are many types of phase detectors which have extended range, with most using digital elements. The most successful and popular are those based around digital flip flops. (e.g. MC 4044, MC 12040, HC 4046, etc).

Consider the circuit below with just two flipflops and an AND gate.



On the first positive going input edge of the reference input, FF1 is set. When the OSC input also goes high, FF2 is also set but at the instant that the V output rises, a reset signal is generated by the AND gate and both flipflops are restored to the rest state. Output V will therefore have virtually zero width. As the phase difference increases, the U output pulse length increases linearly all the way to 360° before starting again from zero. The width of the U pulse output is proportional to phase. If the phase is reduced instead, then the pulse width reduces until zero width is reached. It is easy to see that if the phase is reduced still further then U output will stay at zero width and V output will instead increase linearly (ie. U and V reverse roles). Filtering and averaging the pulses will give an average dc level from each output which is proportional to the pulse width. The difference between these outputs will then be of the form shown below:



Two versions are used in the AT local oscillators. The MC 12040 is an ECL

implimentation of this circuit with other elements added to improve performance especially at high speed. The MC 4044 is a TTL version and this chip also contains a quadrature detector and charge pump neither of which is used in the AT. A word of warning is appropriate here. Some phase detectors (PD) chips have a dead zone near zero degrees (eg. HC 4046) as illustrated by the exaggerated dotted line above. This can be catastrophic in a phase sensitive environment such as the AT, especially in a loop with divider. For example 50 degree jumps in phase were observed when the 1 MHz phase detector in L2 was heated, with such a phase detector installed, as the operating point drifted across the 1 degree dead zone.

The digital form of phase detector has 2 important advantages:
1. The positive slope around zero degrees is highly linear and extends to a full ± 360 degees to reduce the incidence of cycle slipping.

Note that - 180 degrees does not give the same value as + 180 degrees due to the memory characteristic of the internal flip flops.

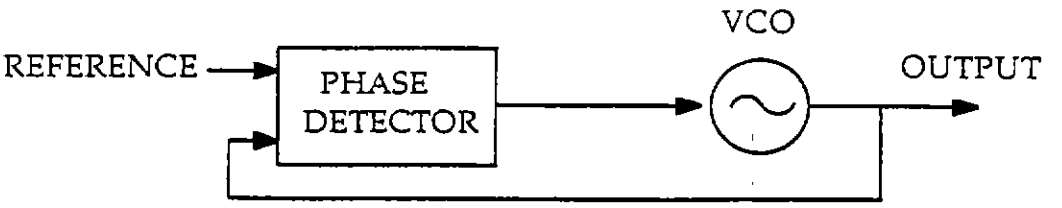
Also note that if the phase is taken to the point A and then reversed it will not retrace the entire curve but will cross the axis to point B as shown.
2. Beyond 360 degrees the output always stays above zero (and beyond - 360 degrees always below zero). This means that if the input signals are not equal in frequency then the phase is continually increasing (or decreasing) and the output is always high (or low). This frequency discrimination is vital for fast phase locking from an unlocked state and is the reason that these devices are usually called "phase/frequency detectors". It also means that sweep circuits are usually not needed for aquiring phase lock.

The phase error signal is not available directly at the output of the detector chip and additional components are needed to do the averaging and differencing. The MC4044 and MC12040 devices have two pulsed outputs U and V. An RC filter on each output and a differential amplifier are used within the AT local oscillator systems to generate the phase correction voltage (see separate description of the phase detector sub module). The term 'phase detector' will henceforth refer to the PD chip plus its associated differential amplifier. The slope of the phase detector characteristic K_d in volts per radian is an important parameter and is typically around 0.3 volt per radian for most AT phase detectors.

Below a few MHz, the MC 4044 was found to have the best temperature stability due to the larger and reasonably well defined output voltage swings. However, at high frequencies, the higher speed of the MC 12040 resulted in better stability.

4.2 PHASE - LOCK LOOP OPERATION

The theory of phase-lock loops is covered extensively in the literature (eg. F. Gardner "Phaselock Techniques"). The description here merely aims to give an introductory working knowledge to assist in fault location and to help understand the design motives. Any modifications or redesign should only be carried out after a more extensive understanding is obtained and a method of checking the loop dynamics and phase noise is available.



Consider the most basic loop above. If the loop is initially in lock with zero phase detector output then it is easy to see that if the reference advances slightly in phase then the phase detector output will move in a positive direction (assuming a positive K_o). This produces a slight increase in the frequency of the VCO. An increased frequency means that the VCO phase will advance relative to the reference thus reducing the phase error. As the phase of the VCO approaches the phase of the reference, the phase detector output reduces to zero once more and the VCO resumes its original frequency but with the required new phase. In this way the VCO tracks all phase changes of the reference input. In the same way any phase drifts, jumps or noise within the VCO are largely removed by a similar reasoning.

As the VCO drifts with temperature or age (or the reference changes frequency etc.) then a non zero VCO control voltage is required to maintain phase lock. This implies a non zero phase detector output and a non zero phase error which drifts with time. To give a very low phase error, either the VCO offset and drift is small, or the loop gain factor $K_o K_d$ must be large, since phase error = VCO error (in Hz) $\cdot$ $2\pi / K_o K_d$. The alternative is to use a high gain amplifier between the phase detector output and the VCO as is done in all AT loops.

Loop Stability

The loop operation described so far is very similar to the feedback mechanism around a simple operational amplifier with a resistive feedback network. The main difference is in the difficulty of obtaining stable phase lock

loop operation.

4.5 MIXERS

An proper understanding of the operation of mixers is desirable to be able to analyse the generation of spurious signals within the LO system.

Basics

A mixer is usually used to translate an input frequency to another frequency by mixing with an LO frequency. Ideally the output frequency is the sum or difference (but more usually both) of the LO and input frequencies. Unfortunately dozens, scores, hundreds or perhaps thousands of other products are also present at the output.

Any nonlinear device will act as a frequency converter or mixer. Nonlinear capacitors (varactors) can be used as in parametric amplifiers and even saturating inductors or voltage variable resistors could be used. However diodes used as non linear resistors are the most useful and widely used mixer component.

The simplest single ended mixer uses a single diode and filters to separate the signal, LO and IF ports. It is rarely used since it has poor supression of intermodulation and higher order products and LO amplitude noise. A single balanced mixer uses 2 diodes and a balun transformer to drive the LO to two ports in antiphase. This gives improved rejection of even order products, LO and LO noise.

Double balanced mixers

The most common mixer is the double balanced mixer consisting of 4 diodes and 2 balun transformers and is almost the only mixer used in the AT. Ideally all products are balanced out except those with odd input or LO harmonics. This mixer can be quite accurately viewed as an analog multiplier with the output being the product of the input (RF) waveform and a squarewave at the LO frequency. The output spectrum then contains the sum and difference of the input RF and LO fundamental frquencies, the sum and difference of the RF and LO third harmonic (1/3 or 10 dB down below the wanted product),the sum and difference of the RF and LO fifth harmonic (1/5 or 14 dB down) etc.

Due to diode and balun imbalance there are also terms with even LO harmonics and terms containing the harmonics of the RF frequency. However these terms are normally much lower provided the RF input level is low (-20 dBm or below). Within the

LO system it is common to operate the RF signal at up to 0dBm input and the terms involving the RF harmonics are only 20 to 40 dB down (especially the odd harmonics).

For example,with an input RF of 21.5 MHz (-5 dBm) and an LO of 100 MHz (+7 dBm) the output spectrum is typically as shown below (next page). Note that these outputs appear on the IF output ports but that similar products appear on the LO and RF ports and can feedthrough and seriously interfere with other subsystems if not sufficiently isolated.

The LO input is normally operated with +7 dBm (5mW) input power. At this power the output sum and difference are each around 7dB (typically $\pm$ 1 dB) below the RF input level. This loss is independant of RF level up to about 0 dBm where saturation starts to set in. The loss is also independant of LO power above about 4 dBm. Below this level the mixer is 'starved' of LO and loss increases but some unwanted products decrease and this can be useful.

Mixer input levels are therefore quite important and should not be altered from the design value without careful consideration.

BLOCK DIAGRAMS

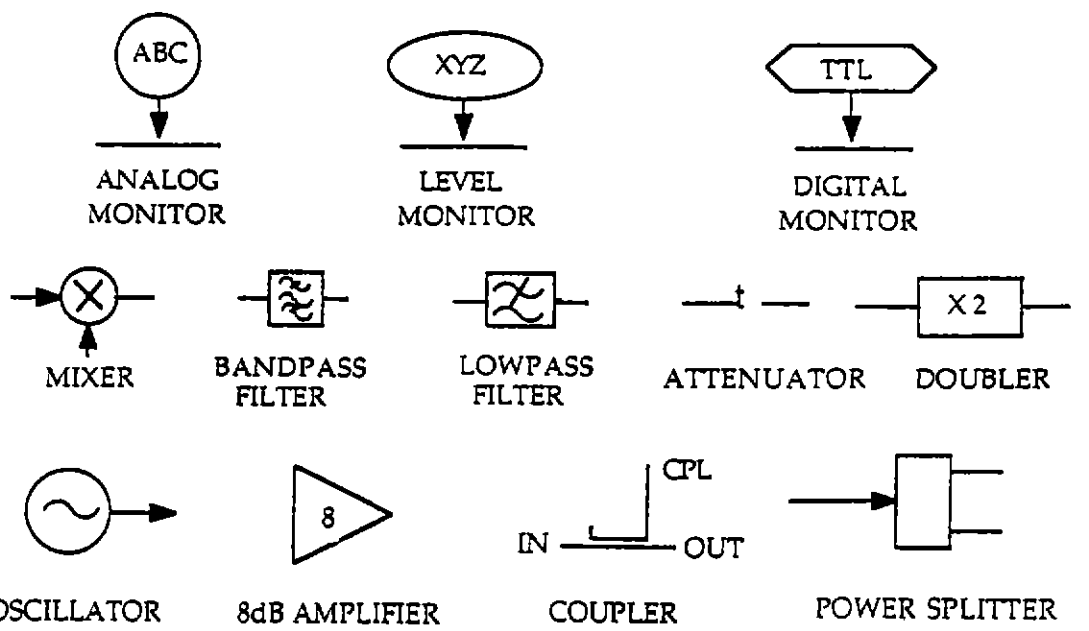
5.1 Introduction:

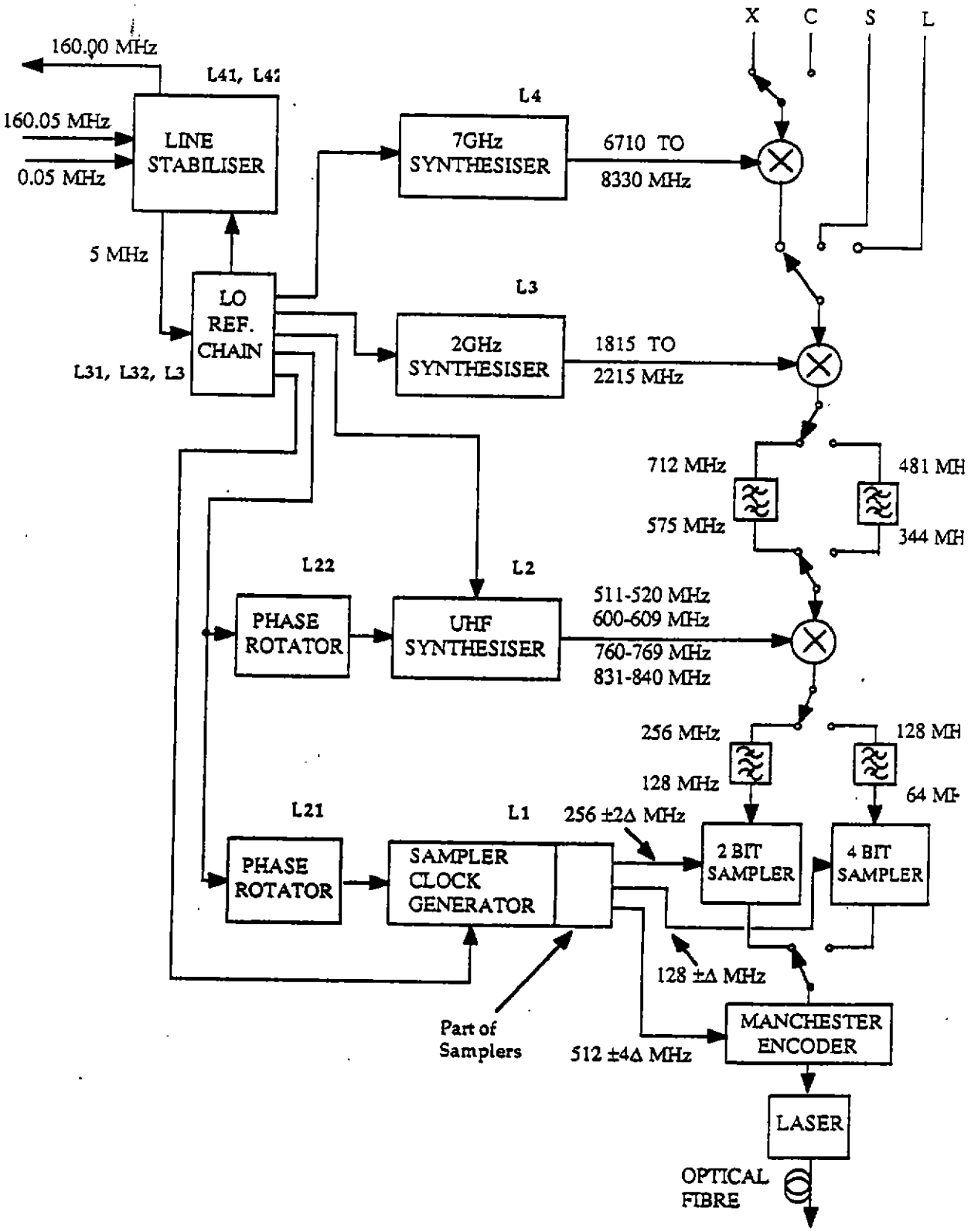
The following diagrams are included in this manual to help in locating monitor points, and to assist users. The first figure shows the overall LO system and its relation to the conversion system. This is followed by a more detailed LO diagram showing the individual loops. The individual module diagrams follow.

5.2 Monitor points:

Analog monitor points are shown as a circle with the monitor point name inside and a line connecting to the line being monitored as shown below. Such a monitor point measures the dc voltage at that point. They should not be confused with an oval monitor point which is also an analog monitor but has an rf detector built in. These level monitors therefore do not measure the dc voltage on the line but rather the rf level. They are intended only to detect the presence and general level of signals in the LO system rather than as accurate level meters. They generally lie anywhere between linear and square law depending on the drive level and frequency, and a temperature dependance of around 1% of the output voltage per degree C is to be expected, but this will also depend on drive level. Digital single bit monitor points are denoted by a stretched hexagonal shape.

5.3 Symbols used:





THE ANTENNA L.O. SYSTEM

SHOWING ITS RELATIONSHIP TO THE CONVERSION SYSTEM

3.3

YIG TUNED OSCILLATORS

YIG tuned oscillators (referred to as YTO or YIG oscillators or simply YIGs) use resonant spheres of Yttrium Iron Garnet (YIG) for tuning. Yttrium iron garnet is a ferrite material which is generally used in the form of a highly polished sphere of diameter in the range of 0.3 to 0.5mm. The reason that this material is used is that the resonant frequency of the sphere is linearly dependant on the strength of an applied external magnetic field due to the precession of its free electron dipoles. The rate, or frequency, of this precession is $f = 2.8\ H$ where H is the applied bias field in oersteds.

When the YIG sphere is positioned inside a small wire loop then the input impedance of this loop is similar to that of a simple LC tuned circuit with the resonant frequency controlled by the applied magnetic field. The YTO uses such a loop and YIG sphere as the resonant tank in a microwave oscillator. The entire oscillator is positioned between the pole pieces of a strong electromagnet and the whole assembly is magnetically shielded resulting in a very compact unit.

The advantages of YIG oscillators are:

More than octave bandwidth (eg. 4 to 10GHz or 1 to 2.2GHz)
Excellent tuning linearity (typically +/- 0.1% +/- 1% offset)
Low drift (typically a few MHz over time and temperature)
Low phase noise (typ. better than -100dBc/Hz at 100kHz offset)

- except that there is usually a large amount of 50Hz magnetic interference.

The disadvantages are that a current rather than a voltage is needed for tuning and the required current is rather high (typically 0.2 to 0.5 A). Phase noise due to 50Hz effects is large (from both magnetic coupling and ripple on the tuning current since only 1ppm or 1μA of hum produces 20kHz jitter). However this is removed if the YTO is properly phase locked. They are also complex and expensive (typically $1K to 3K) but quite reliable.

Magnetic hysterisis produces an uncertainty in frequency of a few MHz which depends on the previous frequency value. Tuning speed is also slow and this limits phase lock bandwidths. These problems are circumvented by using a small auxilliary 'FM' magnetic field coil. Since this coil is directly around the sphere and not on the electromagnet, hysterisis is not present for this coil. Due to a much lower inductance and largely air core, the bandwidth is also high (typically > 1MHz). However the presence of feedthroughs (around 1nF) on the inputs make this difficult to achieve.

To minimise temperature drift a small heater bar with steep negative temperature coefficient is used as a closed loop 'oven' in the mounting of the YIG sphere.

3.4

MIXERS

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BASICS

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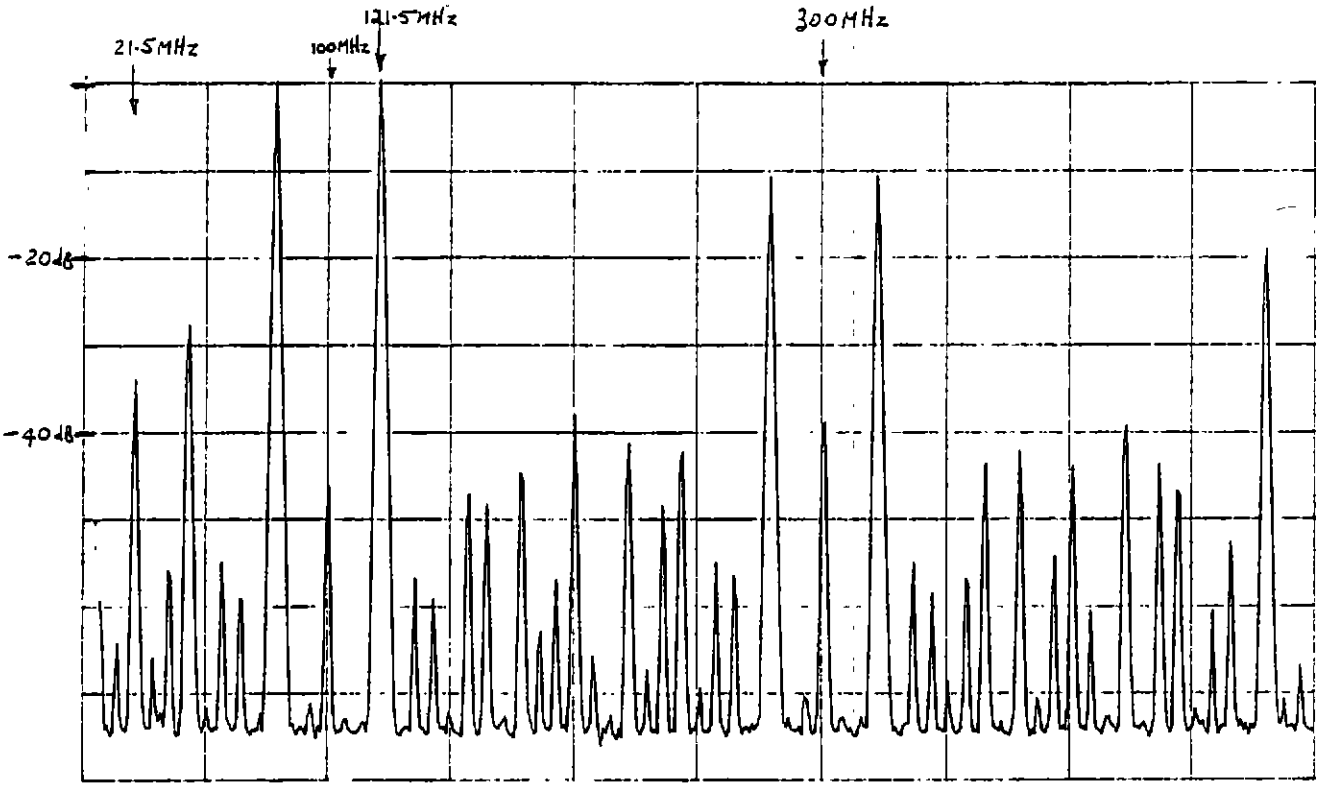
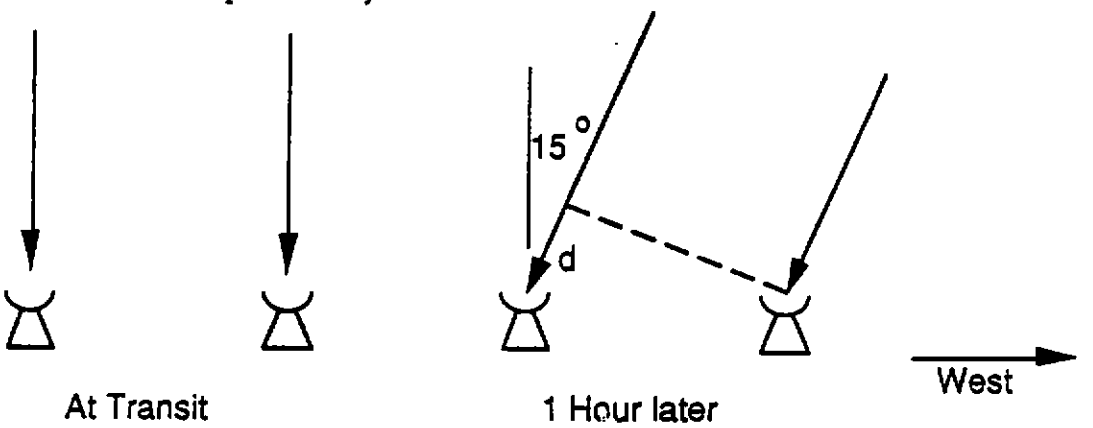


Phase Rotation and Delay Stepping.

This note outlines the reasons for phase rotation and delay stepping and describes some of the techniques used, with emphasis on the approach used in the Australia Telescope.

As the earth rotates, the astronomical object being observed (e.g. star, galaxy, quasar - all of which will be referred to as a 'source') appears to move across the sky with one revolution per day (15 degrees per hour or 0.25 degrees per minute). As a result, there is a continual change in the relative propagation path lengths from the source to each antenna. For example, consider an interferometer using two antennas separated by 1 km.



When the source is directly overhead, there will be exactly equal path lengths from the source to each antenna. However, the relative path lengths are continually changing and, after 1 hour, one path will be longer by 260 metres (i.e. d = Sin 15° • 1 km). When directly overhead, the relative path length is changing at the maximum rate, which is:

73 mm per second (per km of baseline).

This is for the worst case for a source passing directly overhead, with an east-west interferometer sited on the equator. For any other geometry, the rate of change of path difference is always lower than this (as given in the appendix) with the rate of change reducing to zero for a star which is at the south celestial pole.

Since the velocity of light is 300mm per nS, the maximum rate of change of time delay T between the same signal reaching the two antennas is:

0.243 nS per second (per km of baseline).

A path difference of 1 nS means that there is a phase difference, between the

antennas, of 360° at a frequency of 1 GHz. Therefore, if the path difference changes at a rate of 1 nS per second, this gives a phase change rate of 360° per second (or 1 Hz) at 1 GHz. The maximum so called 'fringe' rate (or phase rotation rate) is then:

0.243 Hz for each GHz of receive frequency (and each km of baseline).

For example, with an interferometer separation of 4.1 km, the maximum delay rate is 1 nS per second (3.6 μS per hour) which corresponds to a fringe rate of 10 Hz at a receive frequency of 10 GHz.

To be able to correlate the signals from two antennas, this fringe rate must be removed, otherwise the rotating phase will result in a much reduced average correlator output. As a rough guide, a 26 degree linear rotation (±13°) during an integration period, reduces the correlation by around 1%, whereas a 180 degree rotation gives a decorrelation loss of 35%. Since the previous example with a 4.1 km baseline gives 10 Hz at 10 GHz, or 3600° for each second of integration, it is clear that the phase rotation must be removed.

Removal with a phase shifter

Consider the case of an antenna separation of 4.1 km and a receive frequency of 500 MHz. The delay rate (worst case) is 1 nS per second and it is therefore necessary to remove 180° of phase delay, each second at 500 MHz. This can be achieved by a suitable, continuously-variable phase shifter in the incoming line (or phase rotator in the local oscillator).

However, if the receiver has a bandwidth of 100 MHz (e.g. 450 to 550 MHz), then it is necessary to remove only 162° for a component at 450 MHz and 198° at 550 MHz. This is because, for a given delay, phase shift is proportional to frequency. However, if a simple phase rotator is used to remove this phase rotation, then this will remove the same phase shift at all frequencies. The remaining 18° per second rotation (90 degrees during a 5 second integration) at the band edges will result in a decorrelation loss of 10 % at these edges. The situation degrades rapidly with increasing integration period and for larger bandwidths. In the early days of interferometry with small bandwidths and small baselines, this problem was not as severe.

Removal with delay stepping

Removing the **delay** change rather than the resultant phase change is the more correct approach. This is usually achieved by placing a variable,

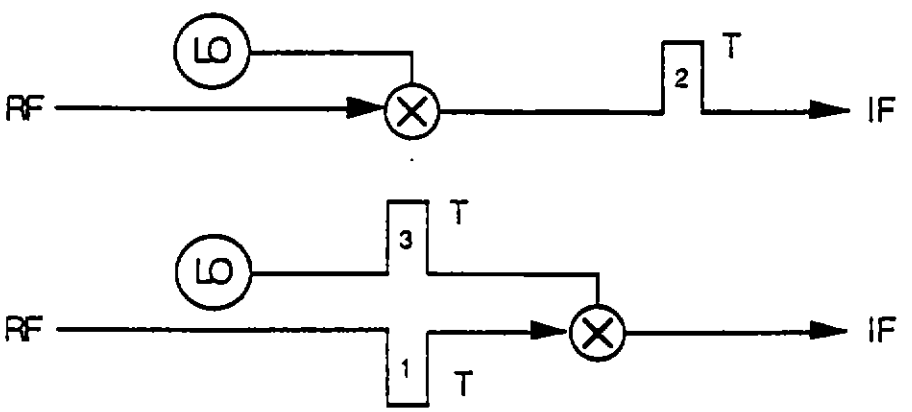
compensating delay within the antenna which has the shortest propagation path length. However, with high frequency, wide band receivers, this is difficult to achieve in the incoming signal path and it is usual to place the delay unit after down-conversion. A down-conversion system subtracts a stable, reference 'LO' frequency from the incoming frequency to produce a lower 'IF' frequency. It is much more convenient to place the delay compensation element in the IF signal path, rather than in the RF input path. However, simple delay is then no longer all that is necessary.

Consider the previous 500 MHz interferometer example, where an extra 1 nS (per second) delay is required within the antenna which has the shortest propagation path length. As before, this corresponds to 180° per second at 500 MHz (also 162° at 450 MHz and 198° at 550 MHz). If the IF is centred at a frequency of 100 MHz (i.e. LO = 400 MHz and IF from 50 to 150 MHz), then a 1 nS extra delay (each second) in the IF changes the phase by only 36° at 100 MHz and this is clearly insufficient to cancel the incoming 180° phase.

If 5 ns extra delay is inserted instead, then this produces the required 180° at the band centre, but produces 270° at the 150 MHz band edge (corresponding to 550 MHz input) instead of 198°. The only way to totally remove the extra phase delay is to use a combination of phase rotation and delay correction (unless the delay is at the incoming frequency and this is rare).

Combined phase rotation and delay stepping

An useful way of looking at this is to consider the two situations below where each case has a simple conversion with equivalent delays inserted.



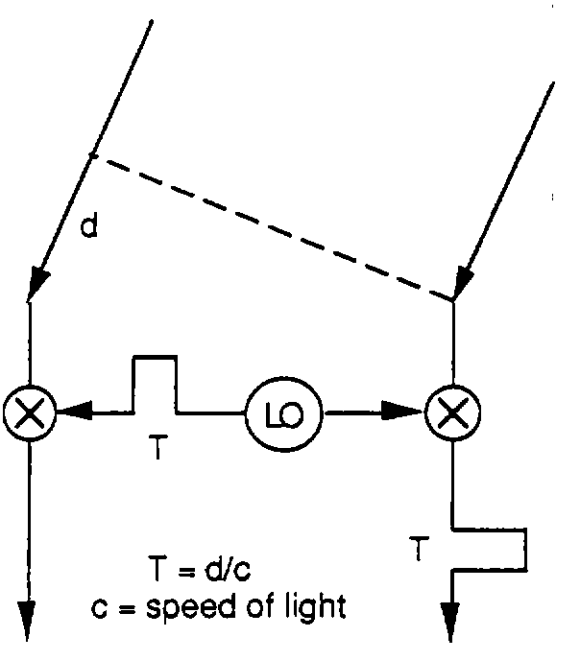
The first case has a single delay in the IF line, whereas the second case has delays in both RF and LO lines. In both cases the IF output is delayed by time T, since

delaying all input signals is equivalent to delaying the output signal. If one antenna has the first structure and the second antenna has the second structure, then the output will be delayed by the same amount, over the full bandwidth.

Therefore a propogation delay T (labelled 1) in the RF of the second antenna can be cancelled by an IF delay T (i.e. 2) in the first antenna **plus** a delay T (i.e. 3) in the LO of the second antenna. The delay in the LO of the second antenna is required to ensure that, in both antennas the LO and RF signals enter the mixer with the same **relative** phase. Without this, the different frequency components of the IF will be out of phase between antennas, leading to a loss of correlation.

Since the LO is a single cw frequency, an LO delay difference between antennas is **exactly** equivalent to a phase shift in one of them. A phase shifter can therefore be used in the LO line instead of a variable delay without error. This is usually a far simpler alternative. However the phase delay of $T * 2 * \pi * f_{LO}$ radians must be recalculated each time the LO frequency is changed but this is not very difficult.

The delay correction in the IF path should be exactly the extra delay T needed by that antenna to equalize the different propogation delays. The local oscillator phase must then be delayed by this same amount T (but in the other antenna).



The example with f_{REC} = 550 MHz and a fringe rate of 0.5 Hz (1 nS per second) may have one or more conversions to a final IF of 100 MHz where the delay unit operates. The phase of the local oscillator (or IF) must then be rotated by a continuously varying phase shifter (often referred to as fringe, lobe or phase

rotators). With a 400 MHz total LO this must be performed at the rate of 0.4 Hz or 144° per second (1 nS per second at 400 MHz). Obviously, if the receive frequency is 5 GHz, then the phase rates must be proportionally higher.

General comments

The phase shift in the local oscillator can be obtained with either an analog phase shifter, or as part of a phase lock loop. The use of phase lock loops in the local oscillator opens the way for highly linear, well controlled phase shifting techniques based on digital circuits. The AT phase rotator is an example of this and its operation is described in the relevant manual.

The delay correction in the IF path can be performed by switching in sections of delay line or by other analog delay circuits but these schemes are far from ideal. However, if the IF signal is ultimately sampled and digitised then simple digital shift registers can be used as delay lines. The only inherent limitation of digital delay lines is that the minimum delay step size ΔT is fixed and equal to the sampler clock period. A sampler clock at 200 MHz gives a minimum delay step $\Delta T = 5$ nS. If the bandwidth is 100 MHz as before, then there is up to ± 2.5 nS delay error and this will produce 50 MHz • 2.5 ns • 360° = 45° at the band edges at ± 50 MHz. Fortunately, small delay corrections (up to $\pm 1/2$ clock period), referred to as fractional-bit delays, are easily applied by adjusting the phase of the sampler clock and thus changing the sampling time as a result. The phase of the sampler clock is changed in exactly the same way as the phase of the local oscillator.

Digital delay lines consist of specialised shift registers. Moderate values of delay, referred to as fine delay, are applied directly to the sampler output (after it is received at the central building in the AT). The bit stream is then converted to a 32 bit parallel bus with each line operating at a slower speed. The majority of the delay, referred to as coarse delay, is then applied to these lines using highly integrated devices at this slower speed. In the AT, a total coarse delay of at least 10 μS, equivalent to half the maximum 6 km baseline is needed in each antenna path. A maximum fine delay of at least 32 bits or 125 nS is required and the fractional bit delay ranges up to 4 nS in steps of 0.004 nS (all with 256 MHz sampling). For more details refer to the relevent delay unit manual.

The phase and delay rates are not a constant value with time but are cosine functions of time as shown in the appendix below. The values for the

setting of the phase rotators and delay lines must therefore be updated very frequently. For very long baselines this can present a problem and the AT phase rotators have the ability to accept a varying phase rate (second derivative of phase, or phase curvature) to permit much longer intervals between phase rotator settings. Details of this are in the relevant manual.

In the previous examples the antenna without the internal delay line is referred to as being at the 'delay centre'. This assumed that one antenna is fixed and the other has a variable delay line. However, it is more common to have delay units in all antennas and this allows the delay centre to be set to the most convenient point and this may be between antennas, for example. This requires that some antennas can have delay removed rather than added and so there must be a long initial internal delay. Of course the above discussion is easily extended to the case of many antennas by regarding each pair in turn as an interferometer.

APPENDIX

The phase difference (in radians) between a signal arriving at an antenna and a reference point (e.g. another antenna) will be given by:

$$\phi(t) = \{ \sin \partial \ \sin d + \cos \partial \ \cos d \cos (H(t) - h) \} * 2 \pi D / \lambda$$

where D is the distance from the antenna to the reference point, H is the hour angle of the centre of the source (field centre), ∂ is the declination of the source centre, h is the hour angle of the vector joining the antenna and the reference point, d is the declination of this vector and λ is the wavelength of the received signal.

The fringe rate is the rate of change of phase with time:

$$d\phi/dt = dH(t)/dt * \{ \cos \partial \ \cos d \ \sin (H(t) - h) \} * 2 \pi D / \lambda$$

where the angular rotation rate of the earth (in radians per second) is:

$$dH(t)/dt = 2 \pi / (24 * 60 * 60) = 7.27 * 10^{-5}$$

The maximum fringe rate will occur when d and ∂ are both 0° and H(t) - h is 90° (the source directly above the antenna) and is given by:

$$d\phi/dt \max = 7.27 * 10^{-5} * 2 \pi D / \lambda$$

For the AT 6 km baseline, observing at 100 GHz, the maximum fringe rate would be 914 radians per second (145 Hz).

MODULE ADDRESS BOARD.

G. McCulloch.
22 January 1990.

Circuit diagram L-/001/01.

This small board is included in all L.O. and Fibre Optic modules (except L2, where its function is included on the interface board itself). It serves mainly two purposes- to detect when a particular module is being addressed via the bus, and to enable the serial number of a module to be read via the dataset. It also provides a method for a module to indicate to a dataset that the module is not in proper OBServing condition, so that its data may be flagged as suspect.

The eight bit serial number read via the bus consists of two sections- the six bit serial number of the module, and two bit version number. The serial number is set by drilling out links on the PCB, and is intended to be permanent. The version number is set by links on headers, and is easily changed. The version code is intended to be used to identify different hardware versions of the same module type. Should a module be changed, in such a way which necessitates a different control or monitoring procedure, the module can be given another version number. The computer software would then be able to interrogate each module, determine the version of the hardware it contains, and then use the correct procedure for that module.

There are no adjustments, although the serial number and version number of the particular module must be encoded.

CIRCUIT DESCRIPTION.

Dataset signals via the 100 pin connector have been grouped in a way which is common to all the L.O. and Fibre modules. This has allowed a 26 conductor ribbon and mass termination connectors to be used for the wiring- both inside the modules and along the back of the rack. The address board is connected across the ribbon, and in those modules which also contain a dataset interface, the ribbon continues on the the interface with the same signals.

The dataset address bus has six bits. In the L.O. rack, the lower four bits (BADD0...3) are used to set the address of a module's position along a bin, and the upper two bits (BADD4,5) are used to address registers within a module (e.g. for start phase and phase rate in L21/L22, and for frequency 1 and frequency 2 in L3 and L4.) The code for a particular position along a bin is hardwired into the rack wiring, and consists of links between

particular pairs of pins on the 100 pin connector. When a module is placed in the rack, this code forces some of the "B" inputs of U1 (74LS85) to be grounded. The "A" inputs are connected to the BADD0...3 of the dataset. When the two codes match, pin 6 goes HI. This is then ANDed with the STRobe from the dataset, to give a signal called Decoded STRobe. Thus, this Decoded STRobe only pulses when this particular module is addressed, and is used within the module for further strobing functions.

To read the serial number, U3 (74ALS541) is taken out of the high impedance mode when the WR/RD line (pin 1) and the Decoded STRobe (pin 19) are both LO, implying that this is the module required to read out its serial number. This then impresses the serial number code present on the input side of U3 (pins 2 to 9)across the data lines, where it is able to be read by the dataset.

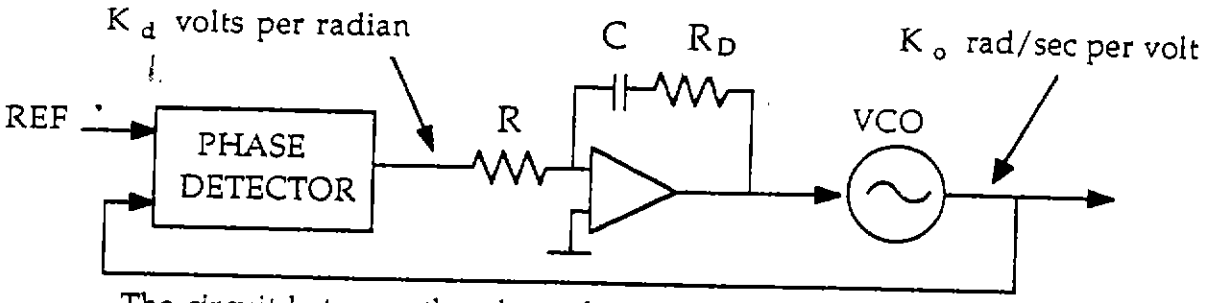
A dataset can look at a particular single bit MONitor line in each bin, and determine quickly whether all modules in the bin are probably in the correct operating mode, and all the loops in lock. U2 (74LS03) was chosen to be an open collector device, so that it could be used for the Bin Wired OR function. This allowed the same signal from all the modules in the bin to be connected in parallel using the ribbon, and any one of them can pull the line LO, indicating a fault. (Each module also has some additional single bit monitors, allowing the computer to use the dataset to determine the reason for the fault condition.) An "OUT OF LOCK" signal from each phase detecctor in a module, and an input from the interface indicating the mode the module is in, are the two inputs used. The PCB has been laid out, so that either or both inputs can be connected to ground, depending on the module's configuration.

An operational amplifier circuit is normally arranged to have negative (ie. 180 degree) feedback at all frequencies where the gain is greater than one. If care is not taken then there may be several rolloff mechanisms at frequencies of greater than 1 MHz. For example, internal stray capacitances or a capacitor on the output of the amplifier (in a phase-lock loop there are the filters in the oscillator tuning input, the phase detector output filter and amplifier stray capacitances). These can combine to give an extra phase lag in excess of 180 degrees which, combined with the inherent 180 degree negative feedback will give a total of 360 degrees. If the gain is sufficient then oscillation occurs.

The usual method of operational amplifier stabilisation is to place a single very large RC time constant within the loop (ie. a dominant pole - with rolloff typically starting at 10 Hz). A maximum of 90 degrees phase lag then occurs due to this pole. At the frequency at which other rolloff phase shifts start to become significant, the loop gain is below unity. This is a simple first order (or regulator) loop. Unfortunately most phase lock loops are second order (as are most servo systems).

An important step in understanding PLLs is to realise that the oscillator tuning voltage varies oscillator frequency rather than phase but that the phase detector output is proportional to phase rather than frequency. Since frequency $\omega = d\phi/dt$ and conversely phase $\phi = \int \omega \, dt$, the oscillator acts as an integrator from the point of view of phase. Since an integrator always gives 90 degrees phase lag, it would seem that there must be no other phase shifts approaching an extra 90 degrees lag up to the frequency at which the gain equals unity. Unfortunately, if no additional filter is added, then it is not possible to achieve both high loop gain and stability at once (since high loop gain would also mean extremely high loop bandwidth in such a first order loop).

It is, however, possible to insert another large time constant (pole) within the loop (with an extra 90 degree phase shift) provided an additional phase lead circuit reduces the phase shift to well below 90 degrees at the frequency of unity gain (it is truly surprising that at mid frequencies there is 180+90+90 degrees of loop phase but that the feedback is still 'negative' and stable provided that the gain is large). The AT achieves this controlled phase shift by using a modified integrator filter as shown below.



The circuit between the phase detector and the oscillator is called the 'loop filter'. Since there are now effectively two integrators within the loop (the oscillator and the operational amplifier), the loop gain falls as $1/\omega^2$ and this is a second order loop. The loop speed or bandwidth (where loop gain drops to unity) is determined primarily by R and C. The damping resistor R_D provides stability by removing the 90 degree integrator lag at high frequences.

If R_D is made variable (as is often done during development) then as R_D approaches zero the integrator lag is not removed and instability occurs at the frequency of unity gain (seen as a peaking of the phase noise at this frequency offset each side of the oscillator centre frequency). This is called the natural frequency ω_n of the loop where $\omega_n = \sqrt{(K_o K_d / R \cdot C)}$ radians per second. The natural frequency ω_n is only equal to the frequency of unity loop gain ω_u when damping is zero. Otherwise $\omega_u = 2 \cdot \partial \cdot \omega_n$ approximately (for $\partial > 1$), where ∂ is the 'damping facter' (see below).

If R_D is made equal to the reactance of C at the natural frequency ω_n (ie. where $R_D = 1/(\omega_n C)$), then the loop is near 'critically' (ie. reasonably but not excessively) damped. R_D is normally left at or near this value (usually a little higher). Then $\omega_u = 1.4\ \omega_n$ and the so called 'damping facter' ∂ is 0.5 (∂ is proportional to R_D with $\partial = R_D \omega_n C/2$) .

If R_D is increased well beyond this point, the frequency of unity loop gain (ω_u) increases in proportion to R_D until a point is reached where the frequency of unity gain exceeds the frequency where unintended phase shifts are excessive and instability occurs once again. This frequency where instability can occur should be as high as possible and always greater than 10 times the natural frequency ω_n. All loop components should therefore be of sufficiently wide bandwidth. If this is not done then it proves to be very difficult to achieve both good stability and low phase noise even when R_D is set for optimum damping.

Alternatively, stability could be achieved by setting ω_n very low but another problem occurs due to the inherent oscillator "phase noise" (see later).

Since no oscillator is ideal the output phase will wander randomly. If the oscillator phase moves around slowly, then the loop negative feedback will remove this, as was shown previously. However, very rapid oscillator phase changes which occur at a rate exceeding the loop bandwidth cannot be removed by the loop. These remaining high speed phase fluctuations can, if large enough, exceed 360 degrees and phase lock will be lost momentarily (better described as cycle slipping). Obviously ω_n must therefore be large enough to reduce the probability of this happening to a low enough value. For example a PLL with 20° rms phase noise will slip cycles around once per second, whereas a loop with 10° noise will do so less than once per day (for ω_n of 50 kHz). Of course the loop specification may call for even lower phase noise and then ω_n may need to be increased further than is necessary to stop cycle slipping.

For VCO and YTO loops, a value of ω_n around 20 kHz to 100 kHz is appropriate to achieve a phase noise of less than 3 degrees. This will require that all loop components have low phase shifts in the MHz region and is the reason that wide band amplifiers (AD847) and other high frequency circuits are used within the phase detector and YTO and VCO driver circuits. Due to the inherently lower phase noise of loops containing VCXOs, they have lower bandwidths of typically 1KHz (and around 10 Hz for L42) and require far less care in this regard. It is strictly the noise bandwidth that we should be considering here. This is around twice the unity gain bandwidth (except when the loop is very underdamped) and this is usually close to the natural frequency ω_n.

The loop clearly acts as a high pass filter for VCO noise since it removes all the low frequency components. However the loop follows all low frequency noise on the reference but ignores all high frequency components. The loop therefore functions as a low pass filter to reference inputs and is a widely used application of phase-lock loops. The loops in the line stabiliser and the satellite LO transfer are used this way to filter out higher frequency noise from the reference. The effective filter bandwidth is then twice the loop bandwidth.

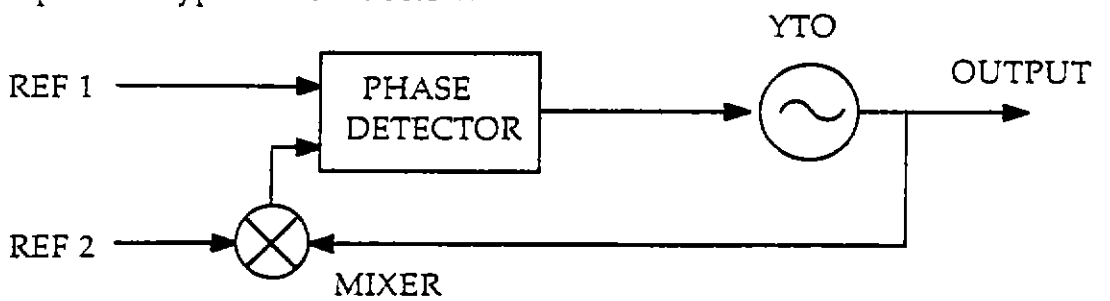
The loop can be disabled, for testing or during frequency changes, by shorting the integrator output to the inverting input (ie. bridging the R_D, C combination) and all most AT loops have a switch included to do this. This reduces the integrator gain to zero and forces the integrator output to zero. The oscillator will then be 'free running' at its uncontrolled frequency.

Divider Loops

Divider phase-lock loops contain a digital divider with division ratio N placed within the feedback path between the VCO and the phase detector. The loop then locks with the VCO at a frequency of N times the reference frequency. If the divider ratio is programmable then the frequency can be changed in steps of the reference frequency. For example the LF loop in module L2 uses a reference of 1 MHz and a divider ratio of 40 to 50 to give an output of 40 to 50 MHz in 1 MHz steps. The natural frequency is then $\omega_n = \sqrt{(K_o K_d / N \cdot R \cdot C)}$ and varies as N and the output frequency changes.

Offset Loops

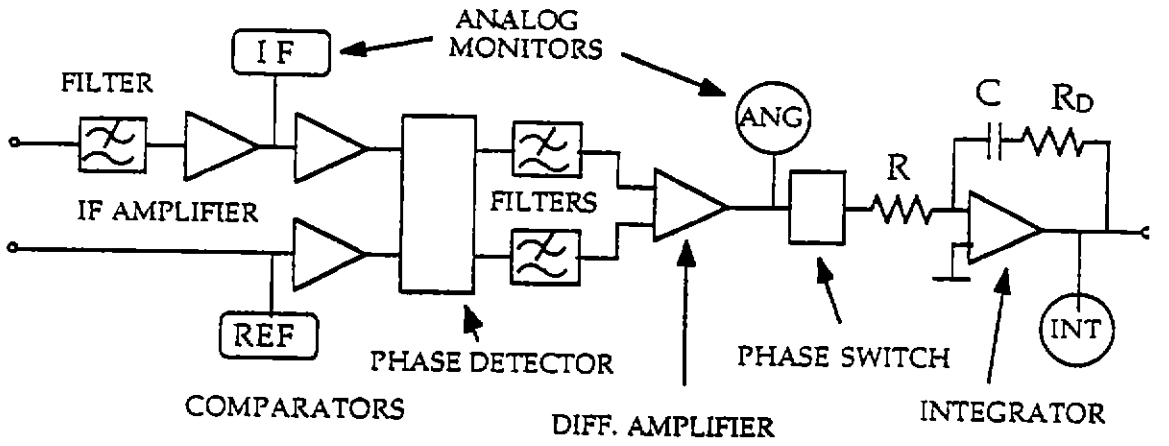
Most AT loops are offset phase-lock loops whereby a fixed reference frequency is subtracted from the oscillator before phase comparison. A typical loop of this type is shown below.



This arrangement forces the oscillator to follow the sum of the two reference frequencies. For example if Ref 1 is 10 MHz with phase of 20 degrees and Ref 2 is 7040 MHz (as in L4) with a phase of 50 degrees then the oscillator is at 7050 MHz with a phase of 70 degrees or 7030 MHz with a phase of 30 degrees (ie. the output is the sum of the phases also). The choice of 7030 or 7050 MHz is made by reversing the polarity of the phase detector output by inserting an inverter amplifier at the phase detector output. The L2 module uses a doubly-offset loop (the UHF loop) where the output is the sum of 3 input frequencies with 2 subtracting mixers in the feedback path.

4.3 PHASE DETECTOR SUB-MODULES

This sub module (RF box) contains the phase detector, integrator (loop filter) and lock-detection circuitry. There are several versions of phase detectors used within the AT LO system but all are very similar in form. The 10 MHz version used in L4 will be described first and the changes required for other variants will then be considered. This description should be read in conjunction with the appropriate circuit diagram.



Since most input signals are analog (sinewaves), each input contains a very-high-speed comparator (Plessey SP 9680) to give digital inputs (square wave ECL signals) to the phase detector device. One input (the IF input which comes from a mixer) has a 2 stage IF amplifier (MSA 670 and NE 592) preceeding the comparator to ensure adequate signal level and optimum signal to noise performance. Two low pass filters remove input signals above 20 MHz (eg. unwanted mixer products and noise) and an input network ensures a reasonable match to the external mixer at all frequencies. Each input to the comparator has a detector and inverting amplifier to monitor signal level.

The 10 MHz ECL comparator outputs feed directly into the MC 12040 phase/frequency detector device (see earlier description). The MC 12040 acts only on the positive-going edge and this edge must be clean with no ringing or multiple zero crossings. Inability to lock and illogical behaviour can be due to the presence of fast (hard to detect) multiple zero crossings or ringing on the positive going edge. This may be caused by oscillation in the IF amplifier (MSA 670 or NE 592), ringing in the comparator or by excessive IF noise

The MC 12040 has dual digital (ECL) outputs. These outputs (pins 3 and 12) are not truly balanced since only one output is toggling at any time, with

the other output permanently high. As the input phase difference goes through zero, this situation reverses with the other output toggling. The pulse width on the active output is proportional to the phase error. When the loop is locked the phase error should be zero but circuit inbalance (or VCO noise) results in very narrow output pulses on one or both outputs. These pulses must be adequately filtered otherwise they appear on the VCO control input and result in sidebands at the 10 MHz reference frequency and its harmonics. A simple RC filter partially removes these pulses (especially the higher harmonics) but there is a limit to the amount of low pass filtering achievable without impairing the stability of the phase lock loop. An LC notch filter (27 pF and 10 µH prior to the integrator) adds to the rejection of the fundamental component.

Since the phase detector output information exists in the difference between the two outputs, a differential amplifier follows. This amplifier has a gain of 5 and a bandwidth in excess of 5 MHz. The output of this amplifier is a DC voltage proportional to phase difference with K_d approximately 0.3 volts per radian. A balance control trimpot provides an offset to correct for phase detector and amplifier unbalance and is adjusted for minimim 10 MHz signal in the integrator output (or on the oscillator sidebands), with the loop closed.

The differential amplifier is followed by the notch filter to reject the reference frequency and an inverting unity gain amplifier which can be switched in or out remotely by a CMOS changeover switch (AD 7512) to invert the error sense and lock to the other sideband (eg 7030 MHz vs 7050 MHz).

Finally the phase error signal arrives at the integrator with R = 2·2 kΩ, C = 8·2 nF and R_D = 820 Ω. Provision has been made to easily substitute a variable resistor for R_D during loop testing. A CMOS switch allows the integrator to be reset to zero output and thus disable the loop. This is most useful if the loop happens to latch up in an unlocked state as can happen, especially if the oscillator is poorly adjusted for frequency. It is also convenient for loop testing since a short to ground on the control line will effectively open the loop. This 'loop disable' switch is always activated by the interface circuits when a new frequency is selected to minimise any risk of latch up. The integrator gives out a voltage in the range -10 to + 10 volts. Since the integrator has very large dc gain the integrator input should be very close to zero when the loop is in lock and this is used to indicate a locked condition.

The phase detector output and the integrator output both have analog monitor outputs via buffer amplifiers. Both points also have digital window detectors to flag an out-of-lock or out-of-range condition respectively. The out-of-lock window accepts only ± 90 mV at the phase detector output and the out-of-range detector accepts ±10 Vat the integrator output before a fault condition is flagged. Both flags have front panel LED indicators and TTL data set outputs. The out-of-lock indicator has a fast attack/slow decay circuit to catch and extend a momentary loss-of-lock indication. Power rails of +15, -15, +5 and -5 volts are required and heavy internal filtering is necessary to avoid unwanted coupling. The phase detector circuit is mounted on a small PCB within a Mk 6 RF box with component side upward. All phase detectors using MC 12040s and in Mk6 boxes have the same component designations located at the same place on all the PCBs. Some components are left out of different versions and the lists of component numbers are not continuous for that reason.

The 5 MHz Version (L3 Module)

This is virtually the same as the previously described 10 MHz version in L4 module except that the IF filter and notch filter (following the differential amplifier) components are both scaled down in frequency.

The 10 MHz Version (L2 Module)

This is virtually the same as the previously described 10 MHz version in L4 module except that the IF filter is of a slightly more complex design.

The 8 MHz Version (L1 Module)

This is similar to the previously described 10 MHz versions. The IF filter and notch filter (following the differential amplifier) components are both scaled down in frequency. The IF amplifier, inverting amplifier, associated CMOS switch and 'loop disable' switch have all been deleted and the input filter has also been replaced by a steeper commercial filter.

The 1 MHz Version (L2 Module)

This is the same in principle to the previously described versions but uses different components and a different PCB layout. The main difference is that TTL rather than ECL components are used for greater phase stability at low frequency. The phase detector is an MC 4044 and the IF comparator is an LM 311. The reference input is TTL and does not need a comparator. An inverter is not needed and the IF and notch filter components are both scaled down in frequency. A smaller PCB and Mk 5 RF box is used since there is little room to spare in this

module. The analog monitors on the IF and REF inputs have been designed to be sensitive to both level and frequency. Since both are TTL signals, the amplitudes are well defined but, due to a fault, the frequency could be in error. This will then be detectable as a change in monitor level

The 10 kHz Version (L31 Module)

This is scaled down version of the 1 MHz detector with filter components scaled down in frequency. Due to the very low frequency of operation, a 'twin tee' notch filter is used rather than an LC filter. This meant a different PCB layout but still uses a Mk5 RF box.

The 50kHz Version (L42 Module)

This is a very special version for the line stabiliser. It uses similar components to the 1MHz version but it includes a 'hold' switch, and extra offset nulling components. There are comparators on each input but no notch filters, amplifiers or IF filters (these are external). A Mk6 RF box is used.

For more details of particular versions, consult the relevent manual.

4.4 YIG TUNED OSCILLATORS

YIG tuned oscillators (referred to as YTO or YIG oscillators or simply YIGs) use resonant spheres of Yttrium Iron Garnet (YIG) for tuning. Yttrium iron garnet is a ferrite material which is generally used in the form of a highly polished sphere of diameter in the range of 0.3 to 0.5mm. The reason that this material is used is that the resonant frequency of the sphere is linearly dependant on the strength of an applied external magnetic field due to the precession of its free electron dipoles. The rate, or frequency, of this precession is $f = 2.8\ H$ where H is the applied bias field in oersteds.

When the YIG sphere is positioned inside a small wire loop then the input impedance of this loop is similar to that of a simple LC tuned circuit with the resonant frequency controlled by the applied magnetic field. The YTO uses such a loop and YIG sphere as the resonant tank in a microwave oscillator. The entire oscillator is positioned between the pole pieces of a strong electromagnet and the whole assembly is magnetically shielded resulting in a very compact unit.

The advantages of YIG oscillators are:

More than octave bandwidth (eg. 4 to 10GHz or 1 to 2.2GHz)
Excellent tuning linearity (typically +/- 0.1% +/- 1% offset)
Low drift (typically a few MHz over time and temperature)
Low phase noise (typ. better than -100dBc/Hz at 100kHz offset)
-except that there is usually a large amount of 50Hz magnetic interference.

The disadvantages are that a current rather than a voltage is needed for tuning and the required current is rather high (typically 0.2 to 0.5 A). Phase noise due to 50Hz effects is large (from both magnetic coupling and ripple on the tuning current since only 1ppm or 1μA of hum produces 20kHz jitter). However this is removed if the YTO is properly phase locked. They are also complex and expensive (typically $1K to 3K) but quite reliable.

Magnetic hysterisis produces an uncertainty in frequency of a few MHz which depends on the previous frequency value. Tuning speed is also slow and this limits phase lock bandwidths. These

problems are circumvented by using a small auxilliary 'FM' magnetic field coil. Since this coil is directly around the sphere and not on the electromagnet, hysterisis is not present for this coil. Due to a much lower inductance and largely air core, the bandwidth is also high (typically > 1MHz). However the presence of feedthroughs (around 1nF) on the inputs make this difficult to achieve.

To minimise temperature drift a small heater bar with steep negative temperature coefficient is used as a closed loop 'oven' in the mounting of the YIG sphere.

4.5 MIXERS

An proper understanding of the operation of mixers is desirable to be able to analyse the generation of spurious signals within the LO system.

Basics

A mixer is usually used to translate an input frequency to another frequency by mixing with an LO frequency. Ideally the output frequency is the sum or difference (but more usually both) of the LO and input frequencies. Unfortunately dozens, scores, hundreds or perhaps thousands of other products are also present at the output.

Any nonlinear device will act as a frequency converter or mixer. Nonlinear capacitors (varactors) can be used as in parametric amplifiers and even saturating inductors or voltage variable resistors could be used. However diodes used as non linear resistors are the most useful and widely used mixer component.

The simplest single ended mixer uses a single diode and filters to separate the signal, LO and IF ports. It is rarely used since it has poor supression of intermodulation and higher order products and LO amplitude noise. A single balanced mixer uses 2 diodes and a balun transformer to drive the LO to two ports in antiphase. This gives improved rejection of even order products, LO and LO noise.

Double balanced mixers

The most common mixer is the double balanced mixer consisting of 4 diodes and 2 balun transformers and is almost the only mixer used in the AT. Ideally all products are balanced out except those with odd input or LO harmonics. This mixer can be quite accurately viewed as an analog multiplier with the output being the product of the input (RF) waveform and a squarewave at the LO frequency. The output spectrum then contains the sum and difference of the input RF and LO fundamental frquencies, the sum and difference of the RF and LO third harmonic (1/3 or 10 dB down below the wanted product),the sum and difference of the RF and LO fifth harmonic (1/5 or 14 dB down) etc.

Due to diode and balun imbalance there are also terms with even LO harmonics and terms containing the harmonics of the RF frequency. However these terms are normally much lower provided the RF input level is low (-20 dBm or below). Within the

LO system it is common to operate the RF signal at up to 0dBm input and the terms involving the RF harmonics are only 20 to 40 dB down (especially the odd harmonics).

For example,with an input RF of 21.5 MHz (-5 dBm) and an LO of 100 MHz (+7 dBm) the output spectrum is typically as shown below (next page). Note that these outputs appear on the IF output ports but that similar products appear on the LO and RF ports and can feedthrough and seriously interfere with other subsystems if not sufficiently isolated.

The LO input is normally operated with +7 dBm (5mW) input power. At this power the output sum and difference are each around 7dB (typically $\pm$ 1 dB) below the RF input level. This loss is independant of RF level up to about 0 dBm where saturation starts to set in. The loss is also independant of LO power above about 4 dBm. Below this level the mixer is 'starved' of LO and loss increases but some unwanted products decrease and this can be useful.

Mixer input levels are therefore quite important and should not be altered from the design value without careful consideration.

BLOCK DIAGRAMS

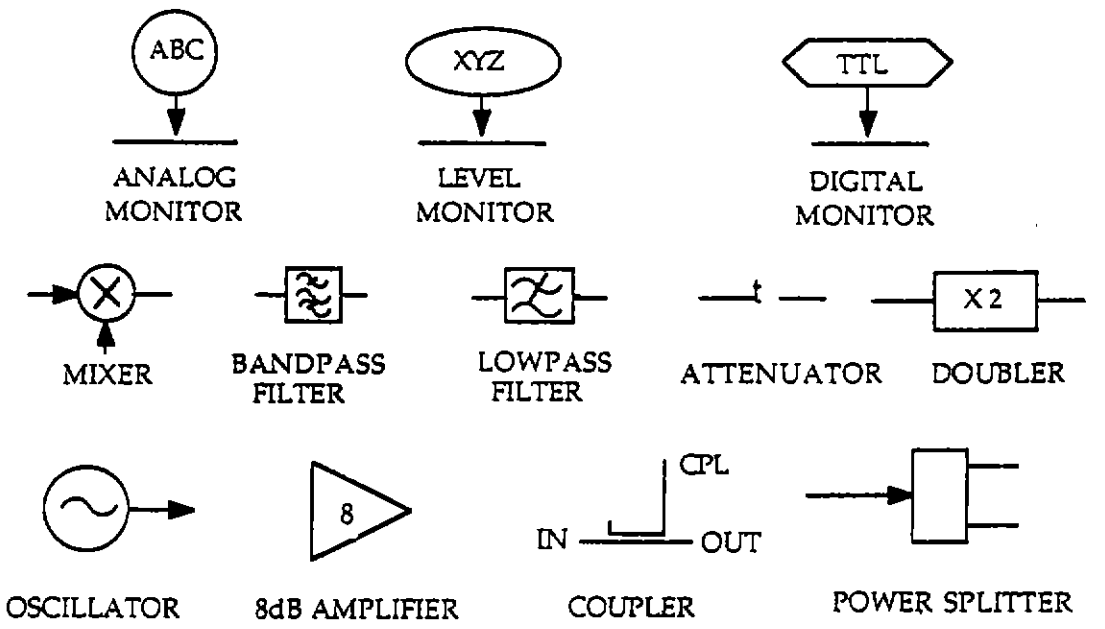
5.1 Intrdduction:

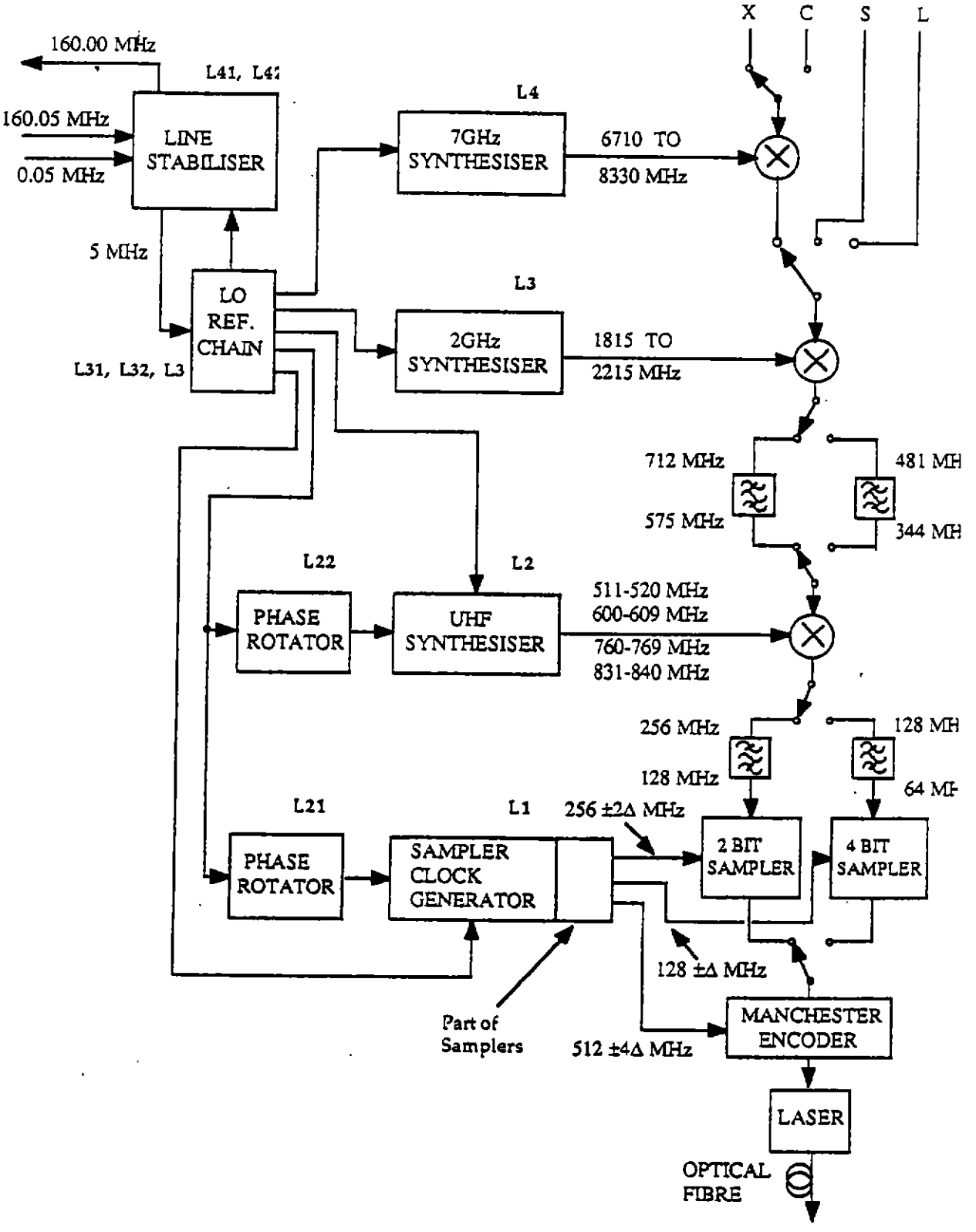
The following diagrams are included in this manual to help in locating monitor points, and to assist users. The first figure shows the overall LO system and its relation to the conversion system. This is followed by a more detailed LO diagram showing the individual loops. The individual module diagrams follow.

5.2 Monitor points:

Analog monitor points are shown as a circle with the monitor point name inside and a line connecting to the line being monitored as shown below. Such a monitor point measures the dc voltage at that point. They should not be confused with an oval monitor point which is also an analog monitor but has an rf detector built in. These level monitors therefore do not measure the dc voltage on the line but rather the rf level. They are intended only to detect the presence and general level of signals in the LO system rather than as accurate level meters. They generally lie anywhere between linear and square law depending on the drive level and frequency, and a temperature dependance of around 1% of the output voltage per degree C is to be expected, but this will also depend on drive level. Digital single bit monitor points are denoted by a stretched hexagonal shape.

5.3 Symbols used:





THE ANTENNA L.O. SYSTEM

SHOWING ITS RELATIONSHIP TO THE CONVERSION SYSTEM

3.3

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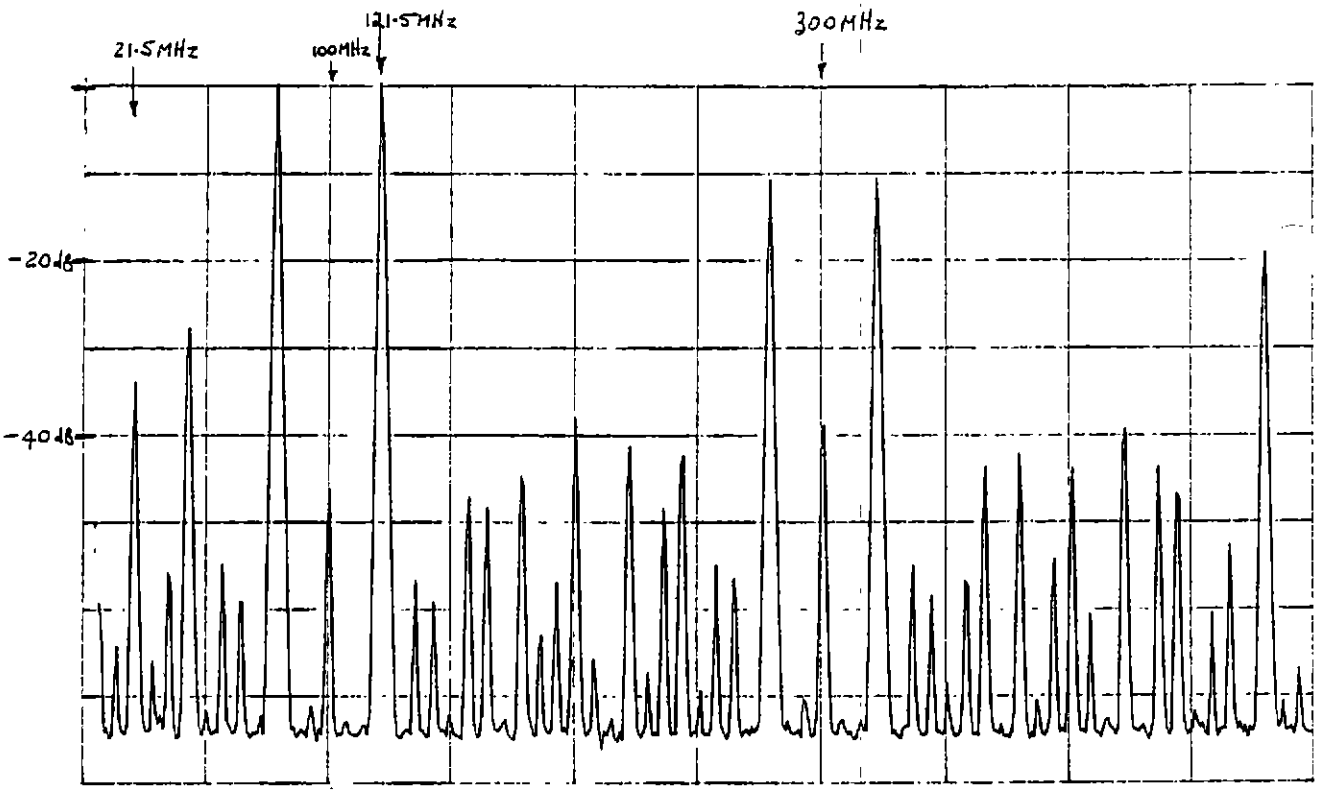
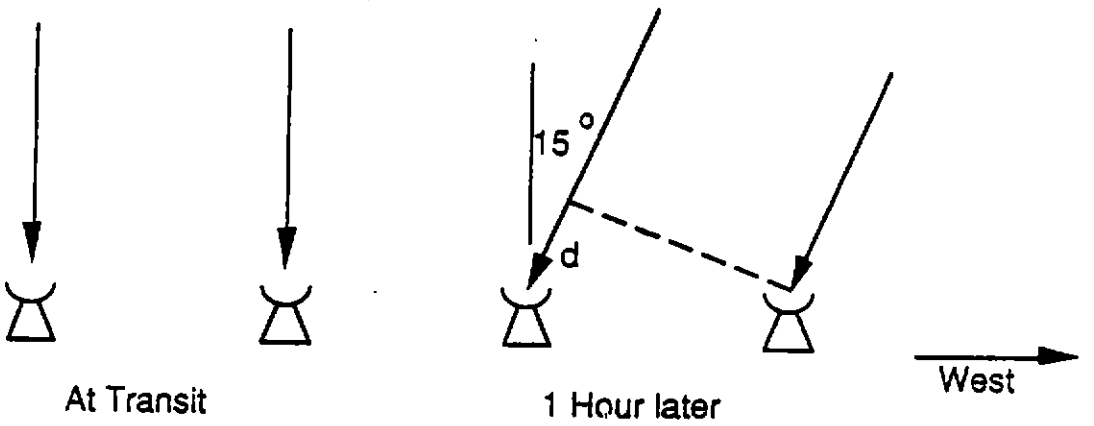


Phase Rotation and Delay Stepping.

This note outlines the reasons for phase rotation and delay stepping and describes some of the techniques used, with emphasis on the approach used in the Australia Telescope.

As the earth rotates, the astronomical object being observed (e.g. star, galaxy, quasar - all of which will be referred to as a 'source') appears to move across the sky with one revolution per day (15 degrees per hour or 0.25 degrees per minute). As a result, there is a continual change in the relative propagation path lengths from the source to each antenna. For example, consider an interferometer using two antennas separated by 1 km.



When the source is directly overhead, there will be exactly equal path lengths from the source to each antenna. However, the relative path lengths are continually changing and, after 1 hour, one path will be longer by 260 metres (i.e. d = Sin 15° * 1 km). When directly overhead, the relative path length is changing at the maximum rate, which is:

73 mm per second (per km of baseline).

This is for the worst case for a source passing directly overhead, with an east-west interferometer sited on the equator. For any other geometry, the rate of change of path difference is always lower than this (as given in the appendix) with the rate of change reducing to zero for a star which is at the south celestial pole.

Since the velocity of light is 300mm per nS, the maximum rate of change of time delay T between the same signal reaching the two antennas is:

0.243 nS per second (per km of baseline).

A path difference of 1 nS means that there is a phase difference, between the

antennas, of 360° at a frequency of 1 GHz. Therefore, if the path difference changes at a rate of 1 nS per second, this gives a phase change rate of 360° per second (or 1 Hz) at 1 GHz. The maximum so called 'fringe' rate (or phase rotation rate) is then:

0.243 Hz for each GHz of receive frequency (and each km of baseline).

For example, with an interferometer separation of 4.1 km, the maximum delay rate is 1 nS per second (3.6 μS per hour) which corresponds to a fringe rate of 10 Hz at a receive frequency of 10 GHz.

To be able to correlate the signals from two antennas, this fringe rate must be removed, otherwise the rotating phase will result in a much reduced average correlator output. As a rough guide, a 26 degree linear rotation (±13°) during an integration period, reduces the correlation by around 1%, whereas a 180 degree rotation gives a decorrelation loss of 35%. Since the previous example with a 4.1 km baseline gives 10 Hz at 10 GHz, or 3600° for each second of integration, it is clear that the phase rotation must be removed.

Removal with a phase shifter

Consider the case of an antenna separation of 4.1 km and a receive frequency of 500 MHz. The delay rate (worst case) is 1 nS per second and it is therefore necessary to remove 180° of phase delay, each second at 500 MHz. This can be achieved by a suitable, continuously-variable phase shifter in the incoming line (or phase rotator in the local oscillator).

However, if the receiver has a bandwidth of 100 MHz (e.g. 450 to 550 MHz), then it is necessary to remove only 162° for a component at 450 MHz and 198° at 550 MHz. This is because, for a given delay, phase shift is proportional to frequency. However, if a simple phase rotator is used to remove this phase rotation, then this will remove the same phase shift at all frequencies. The remaining 18° per second rotation (90 degrees during a 5 second integration) at the band edges will result in a decorrelation loss of 10 % at these edges. The situation degrades rapidly with increasing integration period and for larger bandwidths. In the early days of interferometry with small bandwidths and small baselines, this problem was not as severe.

Removal with delay stepping

Removing the **delay** change rather than the resultant phase change is the more correct approach. This is usually achieved by placing a variable,

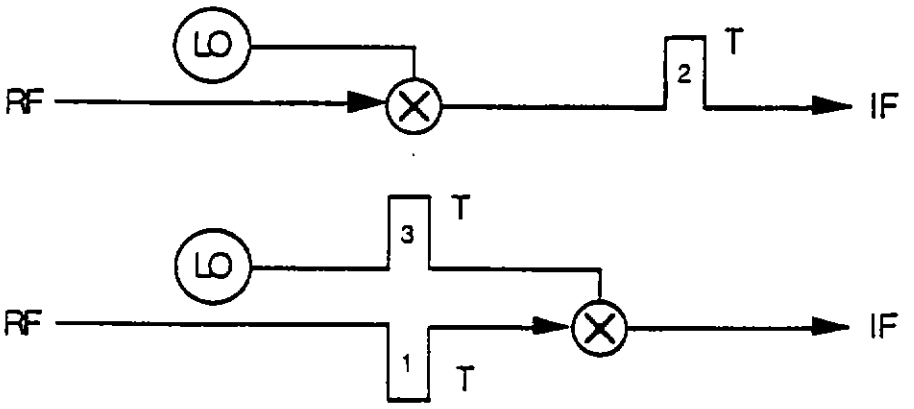
compensating delay within the antenna which has the shortest propagation path length. However, with high frequency, wide band receivers, this is difficult to achieve in the incoming signal path and it is usual to place the delay unit after down-conversion. A down-conversion system subtracts a stable, reference 'LO' frequency from the incoming frequency to produce a lower 'IF' frequency. It is much more convenient to place the delay compensation element in the IF signal path, rather than in the RF input path. However, simple delay is then no longer all that is necessary.

Consider the previous 500 MHz interferometer example, where an extra 1 nS (per second) delay is required within the antenna which has the shortest propagation path length. As before, this corresponds to 180° per second at 500 MHz (also 162° at 450 MHz and 198° at 550 MHz). If the IF is centred at a frequency of 100 MHz (i.e. LO = 400 MHz and IF from 50 to 150 MHz), then a 1 nS extra delay (each second) in the IF changes the phase by only 36° at 100 MHz and this is clearly insufficient to cancel the incoming 180° phase.

If 5 ns extra delay is inserted instead, then this produces the required 180° at the band centre, but produces 270° at the 150 MHz band edge (corresponding to 550 MHz input) instead of 198°. The only way to totally remove the extra phase delay is to use a combination of phase rotation and delay correction (unless the delay is at the incoming frequency and this is rare).

Combined phase rotation and delay stepping

An useful way of looking at this is to consider the two situations below where each case has a simple conversion with equivalent delays inserted.



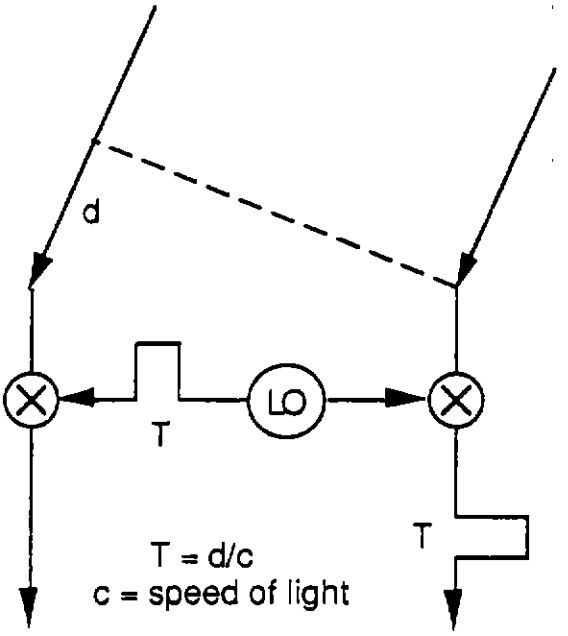
The first case has a single delay in the IF line, whereas the second case has delays in both RF and LO lines. In both cases the IF output is delayed by time T, since

delaying all input signals is equivalent to delaying the output signal. If one antenna has the first structure and the second antenna has the second structure, then the output will be delayed by the same amount, over the full bandwidth.

Therefore a propogation delay T (labelled 1) in the RF of the second antenna can be cancelled by an IF delay T (i.e. 2) in the first antenna plus a delay T (i.e. 3) in the LO of the second antenna. The delay in the LO of the second antenna is required to ensure that, in both antennas the LO and RF signals enter the mixer with the same relative phase. Without this, the different frequency components of the IF will be out of phase between antennas, leading to a loss of correlation.

Since the LO is a single cw frequency, an LO delay difference between antennas is exactly equivalent to a phase shift in one of them. A phase shifter can therefore be used in the LO line instead of a variable delay without error. This is usually a far simpler alternative. However the phase delay of $T * 2 * \pi * f_{LO}$ radians must be recalculated each time the LO frequency is changed but this is not very difficult.

The delay correction in the IF path should be exactly the extra delay T needed by that antenna to equalize the different propogation delays. The local oscillator phase must then be delayed by this same amount T (but in the other antenna).



The example with f_{REC} = 550 MHz and a fringe rate of 0.5 Hz (1 nS per second) may have one or more conversions to a final IF of 100 MHz where the delay unit operates. The phase of the local oscillator (or IF) must then be rotated by a continuously varying phase shifter (often referred to as fringe, lobe or phase

rotators). With a 400 MHz total LO this must be performed at the rate of 0.4 Hz or 144° per second (1 nS per second at 400 MHz). Obviously, if the receive frequency is 5 GHz, then the phase rates must be proportionally higher.

General comments

The phase shift in the local oscillator can be obtained with either an analog phase shifter, or as part of a phase lock loop. The use of phase lock loops in the local oscillator opens the way for highly linear, well controlled phase shifting techniques based on digital circuits. The AT phase rotator is an example of this and its operation is described in the relevant manual.

The delay correction in the IF path can be performed by switching in sections of delay line or by other analog delay circuits but these schemes are far from ideal. However, if the IF signal is ultimately sampled and digitised then simple digital shift registers can be used as delay lines. The only inherent limitation of digital delay lines is that the minimum delay step size ΔT is fixed and equal to the sampler clock period. A sampler clock at 200 MHz gives a minimum delay step $\Delta T = 5$ nS. If the bandwidth is 100 MHz as before, then there is up to ± 2.5 nS delay error and this will produce 50 MHz * 2.5 ns * 360° = 45° at the band edges at ± 50 MHz. Fortunately, small delay corrections (up to $\pm 1/2$ clock period), referred to as fractional-bit delays, are easily applied by adjusting the phase of the sampler clock and thus changing the sampling time as a result. The phase of the sampler clock is changed in exactly the same way as the phase of the local oscillator.

Digital delay lines consist of specialised shift registers. Moderate values of delay, referred to as fine delay, are applied directly to the sampler output (after it is received at the central building in the AT). The bit stream is then converted to a 32 bit parallel bus with each line operating at a slower speed. The majority of the delay, referred to as coarse delay, is then applied to these lines using highly integrated devices at this slower speed. In the AT, a total coarse delay of at least 10 μS, equivalent to half the maximum 6 km baseline is needed in each antenna path. A maximum fine delay of at least 32 bits or 125 nS is required and the fractional bit delay ranges up to 4 nS in steps of 0.004 nS (all with 256 MHz sampling). For more details refer to the relevent delay unit manual.

The phase and delay rates are not a constant value with time but are cosine functions of time as shown in the appendix below. The values for the

setting of the phase rotators and delay lines must therefore be updated very frequently. For very long baselines this can present a problem and the AT phase rotators have the ability to accept a varying phase rate (second derivative of phase, or phase curvature) to permit much longer intervals between phase rotator settings. Details of this are in the relevant manual.

In the previous examples the antenna without the internal delay line is referred to as being at the 'delay centre'. This assumed that one antenna is fixed and the other has a variable delay line. However, it is more common to have delay units in all antennas and this allows the delay centre to be set to the most convenient point and this may be between antennas, for example. This requires that some antennas can have delay removed rather than added and so there must be a long initial internal delay. Of course the above discussion is easily extended to the case of many antennas by regarding each pair in turn as an interferometer.

APPENDIX

The phase difference (in radians) between a signal arriving at an antenna and a reference point (e.g. another antenna) will be given by:

$$\Phi(t) = \{ \sin \partial \sin d + \cos \partial \cos d \cos (H(t) - h) \} * 2 \pi D / \lambda$$

where D is the distance from the antenna to the reference point, H is the hour angle of the centre of the source (field centre), ∂ is the declination of the source centre, h is the hour angle of the vector joining the antenna and the reference point, d is the declination of this vector and λ is the wavelength of the received signal.

The fringe rate is the rate of change of phase with time:

$$d\Phi/dt = dH(t)/dt * \{ \cos \partial \cos d \sin (H(t) - h) \} * 2 \pi D / \lambda$$

where the angular rotation rate of the earth (in radians per second) is:

$$dH(t)/dt = 2 \pi / (24 * 60 * 60) = 7.27 * 10^{-5}$$

The maximum fringe rate will occur when d and ∂ are both 0° and H(t) - h is 90° (the source directly above the antenna) and is given by:

$$d\Phi/dt \max = 7.27 * 10^{-5} * 2 \pi D / \lambda$$

For the AT 6 km baseline, observing at 100 GHz, the maximum fringe rate would be 914 radians per second (145 Hz).

MODULE ADDRESS BOARD.

G. McCulloch.
22 January 1990.

Circuit diagram L-/001/01.

This small board is included in all L.O. and Fibre Optic modules (except L2, where its function is included on the interface board itself). It serves mainly two purposes- to detect when a particular module is being addressed via the bus, and to enable the serial number of a module to be read via the dataset. It also provides a method for a module to indicate to a dataset that the module is not in proper OBServing condition, so that its data may be flagged as suspect.

The eight bit serial number read via the bus consists of two sections- the six bit serial number of the module, and two bit version number. The serial number is set by drilling out links on the PCB, and is intended to be permanent. The version number is set by links on headers, and is easily changed. The version code is intended to be used to identify different hardware versions of the same module type. Should a module be changed, in such a way which necessitates a different control or monitoring procedure, the module can be given another version number. The computer software would then be able to interrogate each module, determine the version of the hardware it contains, and then use the correct procedure for that module.

There are no adjustments, although the serial number and version number of the particular module must be encoded.

CIRCUIT DESCRIPTION.

Dataset signals via the 100 pin connector have been grouped in a way which is common to all the L.O. and Fibre modules. This has allowed a 26 conductor ribbon and mass termination connectors to be used for the wiring- both inside the modules and along the back of the rack. The address board is connected across the ribbon, and in those modules which also contain a dataset interface, the ribbon continues on the the interface with the same signals.

The dataset address bus has six bits. In the L.O. rack, the lower four bits (BADD0...3) are used to set the address of a module's position along a bin, and the upper two bits (BADD4,5) are used to address registers within a module (e.g. for start phase and phase rate in L21/L22, and for frequency 1 and frequency 2 in L3 and L4.) The code for a particular position along a bin is hardwired into the rack wiring, and consists of links between

particular pairs of pins on the 100 pin connector. When a module is placed in the rack, this code forces some of the "B" inputs of U1 (74LS85) to be grounded. The "A" inputs are connected to the BADD0...3 of the dataset. When the two codes match, pin 6 goes HI. This is then ANDed with the STRobe from the dataset, to give a signal called Decoded STRobe. Thus, this Decoded STRobe only pulses when this particular module is addressed, and is used within the module for further strobing functions.

To read the serial number, U3 (74ALS541) is taken out of the high impedance mode when the WR/RD line (pin 1) and the Decoded STRobe (pin 19) are both LO, implying that this is the module required to read out its serial number. This then impresses the serial number code present on the input side of U3 (pins 2 to 9)across the data lines, where it is able to be read by the dataset.

A dataset can look at a particular single bit MONitor line in each bin, and determine quickly whether all modules in the bin are probably in the correct operating mode, and all the loops in lock. U2 (74LS03) was chosen to be an open collector device, so that it could be used for the Bin Wired OR function. This allowed the same signal from all the modules in the bin to be connected in parallel using the ribbon, and any one of them can pull the line LO, indicating a fault. (Each module also has some additional single bit monitors, allowing the computer to use the dataset to determine the reason for the fault condition.) An "OUT OF LOCK" signal from each phase detecctor in a module, and an input from the interface indicating the mode the module is in, are the two inputs used. The PCB has been laid out, so that either or both inputs can be connected to ground, depending on the module's configuration.

DO NOT SCALE IF IN DOUBT ASK

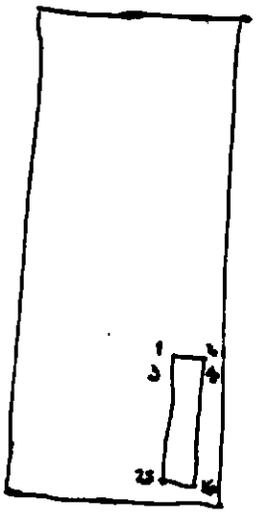
REVISIONS		
ISSUE	DESCRIPTION	APPD DATE
A	ORIGINAL ISSUE	
B	(1) 26 PIN RIBBON CONNECTOR PIN NUMBERS CHANGED (2) RP1 + RP2 10kΩ to 22kΩ (3) PIN NUMBERS ON U3 CHANGED	12 10 8.

J1 26 PIN RIBBON

RIBBON NUMBER

$\overline{\text{STROBE}}$	26
HI/$\overline{\text{LO}}$	24
WR/$\overline{\text{RD}}$	23
A5	22
A4	21
A3	20
A2	19
A1	18
A0	17
MOD ADR 3	4
MOD ADR 2	3
MOD ADR 1	2
MOD ADR 0	1
GND	25
D7	16
D6	15
D5	14
D4	13
D3	12
D2	11
D1	10
D0	9
SBDRDY	5
(GND)	6
UNALLOCATED	7
MON	8

ESS DECODED STROBE



TOP VIEW

RECEIVED
23 MAY 1988

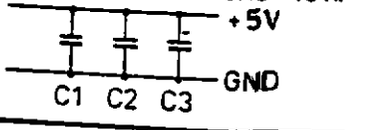
CSIRO
2 JUL 1988
RADIOPHYSICS

+5V

1/9 RP2
22kΩ

U1 74LS85
U2 74LS03
U3 74ALS541

BYPASS CAPACITORS 10 nF



CSIRO RADIOPHYSICS DIVISION

AUSTRALIA TELESCOPE PROJECT

ADDRESS DECODER BOARD

A2	L / 001 / 01 B	ISSUE B

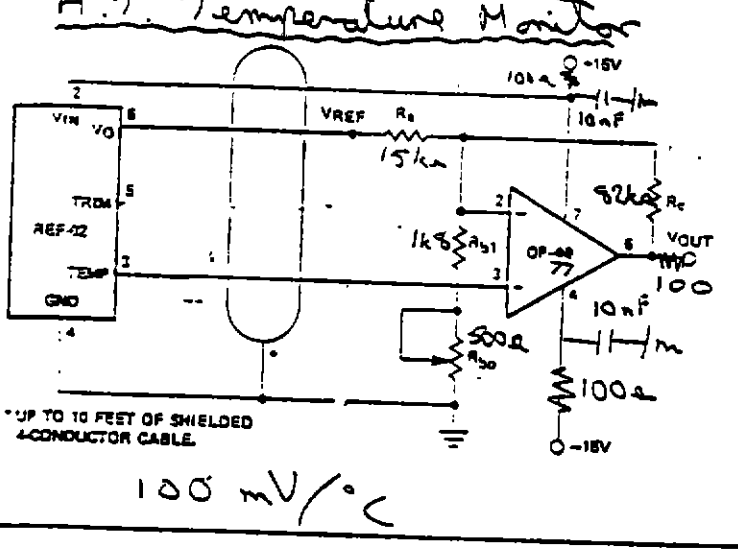
TEMP MONITOR PCB (IN ALL 40 MODULES)

DUPLICATES THIS CIRCUIT

3'6

PMI REF-02 +5V PRECISION VOLTAGE REFERENCE/TEMPERATURE TRA

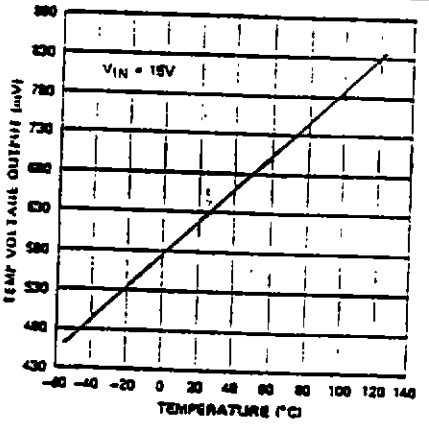
PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR



RESISTOR VALUES	
TCV_{OUT} SLOPE (Si	10mV/
TEMPERATURE RANGE	−55° C −125
OUTPUT VOLTAGE RANGE	−0.55 +1.2
ZERO-SCALE	0V @
R_s (= 1% resistor)	9.09k
R_{b1} (= 1% resistor)	1.5k
R_{bp} (Potentiometer)	200
R_c (=1% resistor)	5.11k

*For 125°C operation, the op amp ou increase V_{IN} to +18V from +15V if this

TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE (REF-02A)



REFERENCE STACK WIT REGULATION

Two REF-01's and one REF- 15.000V and 25.000V outpu circuit is near-perfect line outputs. A 27V to 55V int change which is less than t load bypass resistor (R_B) current (I_{SY}) of the 15.000V In general, any number o stacked this way. For exa outputs in 5V or 10V steps. T to 130V. However, care mus load currents do not exce (typically 21mA).

RECEIVED
23 MAY 1990

REDUCE P.C.

Copper Side

Component Side

Temp. Mon.

Component Overlay

REDUCE 2:1

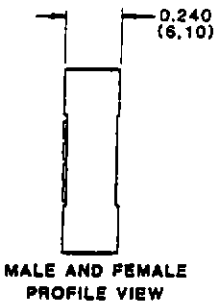
RECEIVED

23 MAY 1990

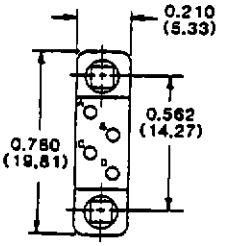
HIGH DENSITY RECTANGULAR CONNECTORS with FIXED CONTACTS

SGM (SMPL) SERIES INSULATOR DIMENSIONS

MATING FACE OF FEMALE CONNECTOR OR REAR FACE OF MALE CONNECTOR



MALE AND FEMALE
PROFILE VIEW



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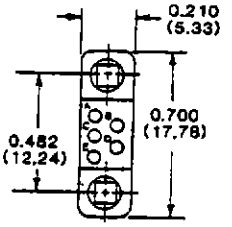

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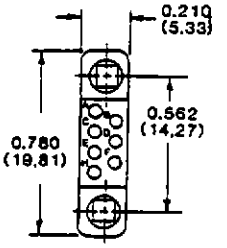

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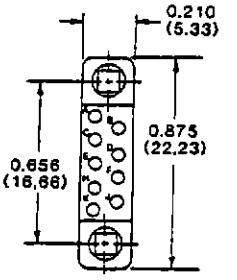

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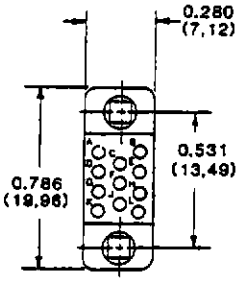

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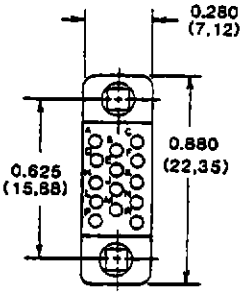

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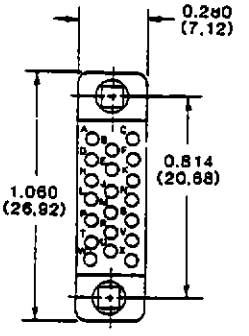

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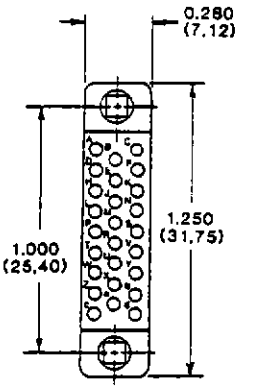

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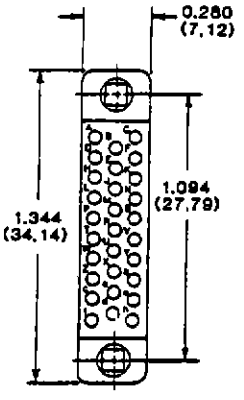

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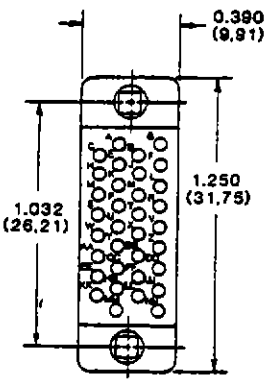

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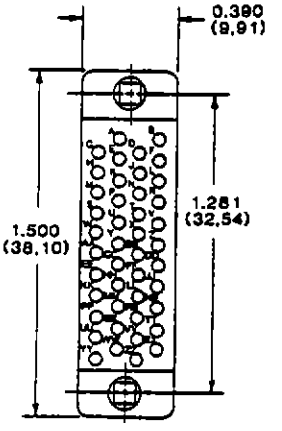

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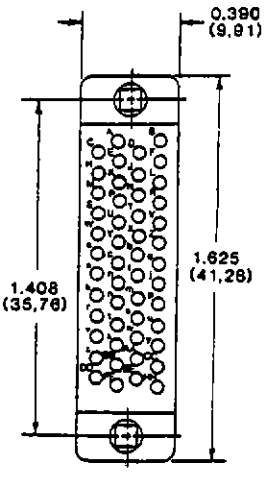


SIZE 50

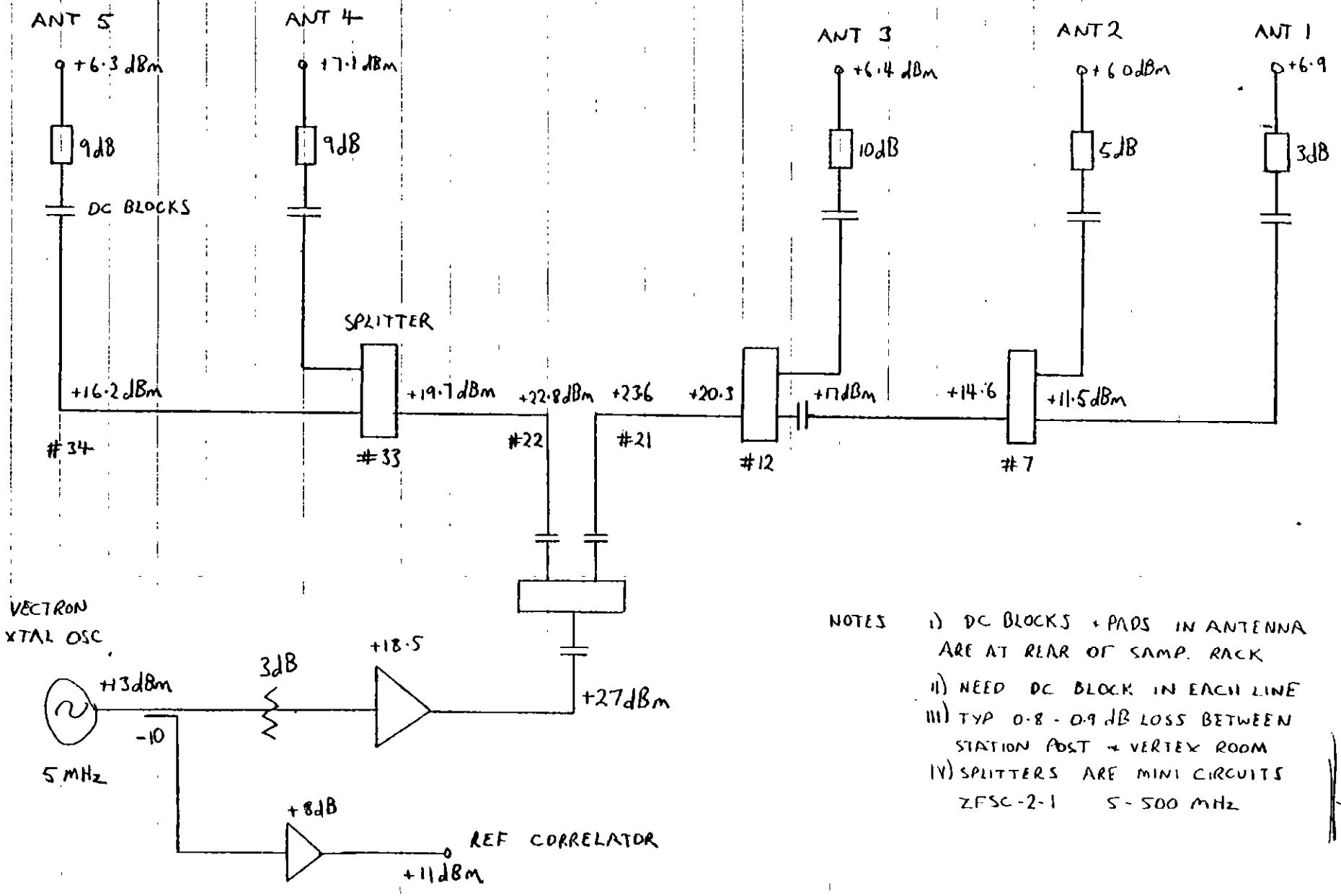
SEE SGM SERIES PRINTED BOARD HOLE PATTERN PAGE FOR CONNECTOR VARIANT CONTACT HOLE POSITIONS

MATERIAL: GLASS FILLED DIALLYL PHTHALATE PER MIL-M-14 TYPE SDG-F

DIMENSIONS ARE IN INCHES (MILLIMETERS)
ALL DIMENSIONS SUBJECT TO CHANGE

5 MHz L.O. DISTRIBUTION

RG 4/3/90



NOTES
i) DC BLOCKS + PADS IN ANTENNA ARE AT REAR OF SAMP. RACK
ii) NEED DC BLOCK IN EACH LINE
iii) TYP 0.8 - 0.9 dB LOSS BETWEEN STATION POST + VERTEX ROOM
iv) SPLITTERS ARE MINI CIRCUITS ZFSC-2-1 5 - 500 MHz