



39.1/1009

# Phase Transfer System

## TECHNICAL MANUAL

### Design/Construction:

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Gerry McCulloch  
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### Documentation:

Narrabri Electronics Group  
Allan Young  
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S/N 000



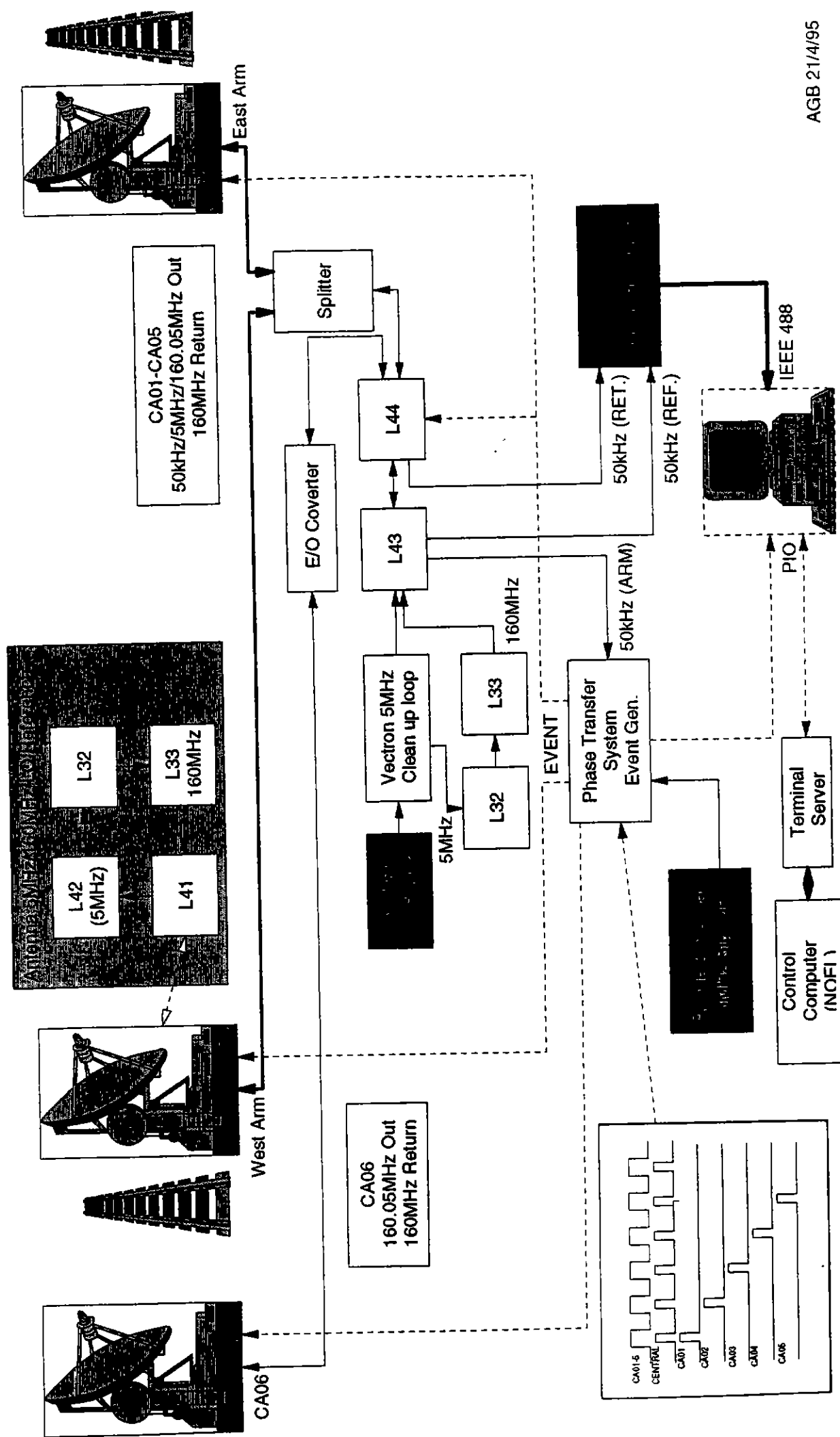
## INTRODUCTION

This manual is aimed at giving an overall picture of the Phase Transfer system at the Compact Array. The phase transfer system is aimed at maintaining a long term frequency stability across the array (or at least a knowledge of the phase/frequency relationships). This is done by periodically transferring a reference signal from the central site (currently a 5MHz HP Rubidium frequency standard) to each antenna via coax (or fibre to CA06) and periodically measuring a returned signal from each antenna. Any variations measured here can then be corrected for by the phase rotators in each antenna at the next integration cycle.

Note that this system does not maintain constant short term phase noise characteristics across the array (i.e. the noise power spectrum between antennas will be uncorrelated approximately 10% of the time). This is because of the requirement to transmit each antennas phase information back to the central site. Also note that the transferred phase information only has a 50kHz bandwidth, being limited by the sampling rate of the PLL in each antennas L42 module.

The following page shows a schematic of the overall Phase Transfer System, the remainder of this manual gives a description of how & why the phase transfer system was designed the way it was, and its performance.

# Phase Transfer System





## DESIGN PHILOSOPHY

Allan Young & Gerry McCulloch

The aim of the Phase Transfer System is twofold- to **phase-lock** the Vectron 5MHz VCXO in each of the antennas to the 5MHz Rubidium station reference in the Central Building, and to **measure phase changes between the antenna reference and the Central Building reference** caused, for example, by cable variations. These changes can then be either eliminated or allowed for by some means. In the Australia Telescope system, a high frequency and a very low frequency are sent out to the antennas via buried coaxial cable, and these are used to phase lock the oscillator in the antenna. Another high frequency signal is sent from the antenna back to the central building, and this is used to measure the phase changes between the antenna and the central building.

Refer to Thompson et al., section 7.2<sup>1</sup> for a detailed discussion of the philosophy of designing a phase transfer system. It is perhaps worthwhile, though, to briefly summarise here, the main conclusions which can be drawn from [1]. For the system where two signals, of different frequencies, are sent in opposite directions along a cable, their difference in frequency should be as small as possible, since errors do not track with frequency. Along the cable, there will be multiple reflections from many sources, and the magnitude of the reflection from each of these should be kept as small as possible. The coax cable should be as lossy as possible, to attenuate the reflected signal components. This last condition influences consideration of the frequency to be used for the high frequencies. For a length of coax cable, the attenuation increases with frequency, and so one way of effectively increasing the loss of the cable is to use higher frequencies. Using high frequencies enables the fractional difference between the two frequencies to be very small, making losses and phase effects almost identical in both directions. However, the loss still has to be low enough so that sufficient signal-to-noise is available at the far end, to enable the electronics to work reliably.

The AT uses a two-way system with different "out" and "back" frequencies present on the cable. These frequencies are around 160MHz. This frequency was chosen as a compromise between the angular precision required in the controlling process and the attenuation in the cable. The specification for local oscillator stability is 1 degree per GHz. This figure originated at the VLA and is well documented in Ekers et al<sup>2</sup>. This is about a factor of ten better than the atmospheric variations at the VLA site and it was assumed that the VLA site atmosphere was better in this respect than Culgoora.

The figure of  $1^\circ$  at 1GHz equates to  $0.16^\circ$  at 160MHz and  $0.005^\circ$  at 5MHz. Phase detectors in the AT have a typical sensitivity of 5millivolts per electrical degree. From these figures, it is evident that the higher the frequency used for the phase comparison between the antenna reference and the central reference, the better and more accurate the measurement is likely to be. There is a second benefit in using a higher frequency for the phase comparison. If, for example, the antenna's 5MHz reference oscillator has a tuning sensitivity of  $1^\circ$  for 3millivolts of control voltage, then, if the 5MHz is multiplied up to produce 160MHz, the phase change is also multiplied up, to become  $32^\circ$  for the same 3millivolts. On the other hand, if the 5MHz is divided down to 1MHz the phase change is also divided down, to be  $0.2^\circ$  for 3millivolts. Thus, the higher the multiplication factor between the controlled oscillator and the frequency of the phase comparison, the more sensitive the phase

<sup>1</sup> Thompson, A.R., Moran, J.M., and Swenson, G.W., "Interferometry and Synthesis in Radio Astronomy", Wiley, New York, 1986.

<sup>2</sup> Napier, Thompson and Ekers, "The Very Large Array: Design and Performance of a Modern Synthesis Radio Telescope." Proc. IEEE, Vol. 71, No.11, November 1983.

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correction circuit will be. However, technology imposes an upper limit, since it is difficult to design good phase detectors at higher frequencies.

For the type of cable used at Culgoora, the attenuation is of the order of 10dB at 5MHz, 50dB at 160MHz and 500dB at 1GHz. If there is low attenuation in the cable, then there will be multiple reflections present due to imperfections throughout its length. The phase correction circuit in an antenna will then respond to the vector sum of these multiple signals, resulting in a phase error.[1] If there is too high an attenuation in the cable, then the signal level at the furthest end of the cable will be very small. If this occurs, then noise from the electronics will add significantly to the composite signal fed into the phase detector. This will result in noise being transferred to the phase locked loop, and also to the returned phase measurement. It appeared that the best region for our system lay somewhere between 100MHz and 500MHz. Both 160MHz and 320MHz were possibilities, as they were available in the antennas. Finally, 160MHz was chosen, as the cable loss was a little less, making it more certain that there would be sufficient signal at the ends of the cable (commensurate with an acceptable power into the cable at the central building). In the system implemented, 160.05MHz is sent up the cable from the central site and 160.0MHz is sent back from the antenna. To overcome coupling and interference problems, time multiplexing of these signals is used. For use in other parts of the system, 5MHz and 50KHz are also distributed along the cable at Culgoora.

It is necessary to recognise that the comparison-correction circuit used in the phase transfer system, is an offset phase locked loop. The phase errors are effectively measured at 160MHz, although the phase comparison is actually made at 50KHz. Making this comparison at 50KHz has several advantages. Because the 160.05MHz signal picked off the coax cable has a low signal to noise ratio, it would be desirable to use a narrow band filter to reduce the noise level. However, sufficiently narrow bandwidth filters are not easy to make at 160MHz, and, in any case, a narrow bandwidth filter at this frequency would be likely to have a phase response which was very temperature sensitive. For these reasons, the filtering is done at the 50KHz IF, where filters hundreds of hertz wide are easy to make. Using 50KHz as a comparison frequency has another advantage. Because a reference 50KHz has to be distributed along the same coax cable from the central site, cable length variations result in only a fraction of a degree variation at this frequency as compared with variations at 160MHz. Additionally, good phase detectors can be readily made at this frequency.

In the central building, the 160.05MHz is phase locked to the site's frequency reference. In the antenna, the 5MHz VCXO is locked to this reference. The antenna's VCXO is multiplied up to 160MHz, and is then mixed with the 160.05MHz on the cable, to produce a 50KHz IF. The resulting 50KHz signal contains the phase error of the antenna VCXO. This 50KHz IF is compared with the reference 50KHz which is sent from the central site along the cable. The resulting error signal is used to phase lock the local VCXO to the central 5MHz. Note, though, that the VCXO still has a phase error (relative to the site's frequency reference) due to the cable delay and errors in the PLLs. The frequency multiplication within the antenna makes the correction system extremely sensitive, as this function is much more effective than attempting to directly force the antenna's 50KHz to have the same phase as the 50KHz coming down the line from the central site. The net effect is that phase errors in the final LO frequencies are multiplied up from only 160MHz and not from 50KHz.

A third signal at 5MHz, is also sent out from the central site along the cable. In the antenna, this is phase compared with the antenna 5MHz in a 5MHz phase meter. In the system described above, there is an integral number of 160.0MHz cycles during one 50KHz period. Therefore, it would be possible for the 160.0MHz to slip one or more cycles, and still be properly in lock. Because the 160MHz is derived by multiplying lower frequencies, the slipping of 160MHz by one cycle would result in the lower frequencies (20MHz, 40MHz, 80MHz etc.) slipping by less than one complete cycle. As these frequencies are also used in the antenna, this would cause phase changes throughout the local oscillator system. It is not easy to ensure that such a slippage will never occur. So, in the AT, the phase of the antenna's 5MHz is measured with respect to the phase of the central building's 5MHz, as distributed along the array. Although the phase of the building's 5MHz will change due to cable variations, this measurement is only looking for gross changes (in the order of  $18^\circ$  or more), and any cable variations will be much less than this. The result of this phase measurement is sent back to the

central building, where its value is monitored. If a large change in value is detected, then the array is recalibrated.

### Detailed analysis.

A free-running oscillator has a spectral density as shown in figure 1.

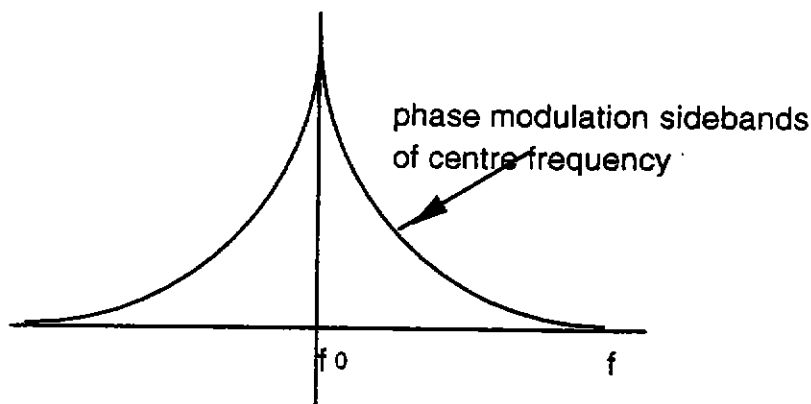


Fig. 1

The deviation from  $f_0$  results from the inherent phase noise of the oscillator and is actually phase modulation sidebands of the carrier at  $f_0$ . By comparing the local oscillator with a reference we reduce the phase noise spectrum to that shown in figure 2 where  $\omega_m$  is the bandwidth of the phase locked loop.

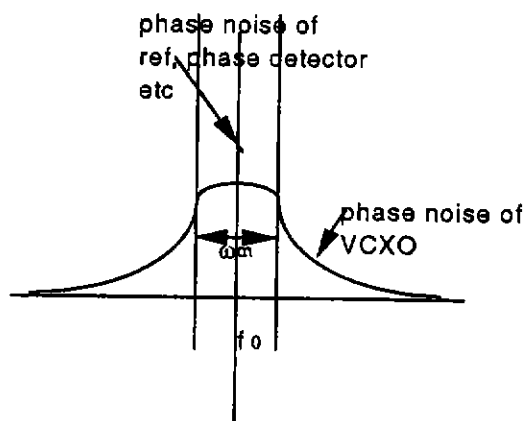


Fig. 2

If the loop bandwidth is too small then there is still a lot of phase noise. If we make the loop bandwidth too wide we can reduce the phase noise but due to the phase-locked-loop op-amp's gain falling off we get a phase roll-off which changes the loop characteristics causing instabilities. Thus  $\omega_m$  is a compromise. Because of the remaining phase noise there is always a finite possibility that the oscillator will skip one wavelength. If this happens, the loop will continue on as if nothing had happened. The 160MHz coherence is not affected, but all the lower frequencies derived from it will



# **160.05MHz/50kHz Reference Module L43**

## **TECHNICAL MANUAL**

### **Design/Construction:**

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Gerry McCulloch  
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Ross Gardyne  
??

### **Documentation:**

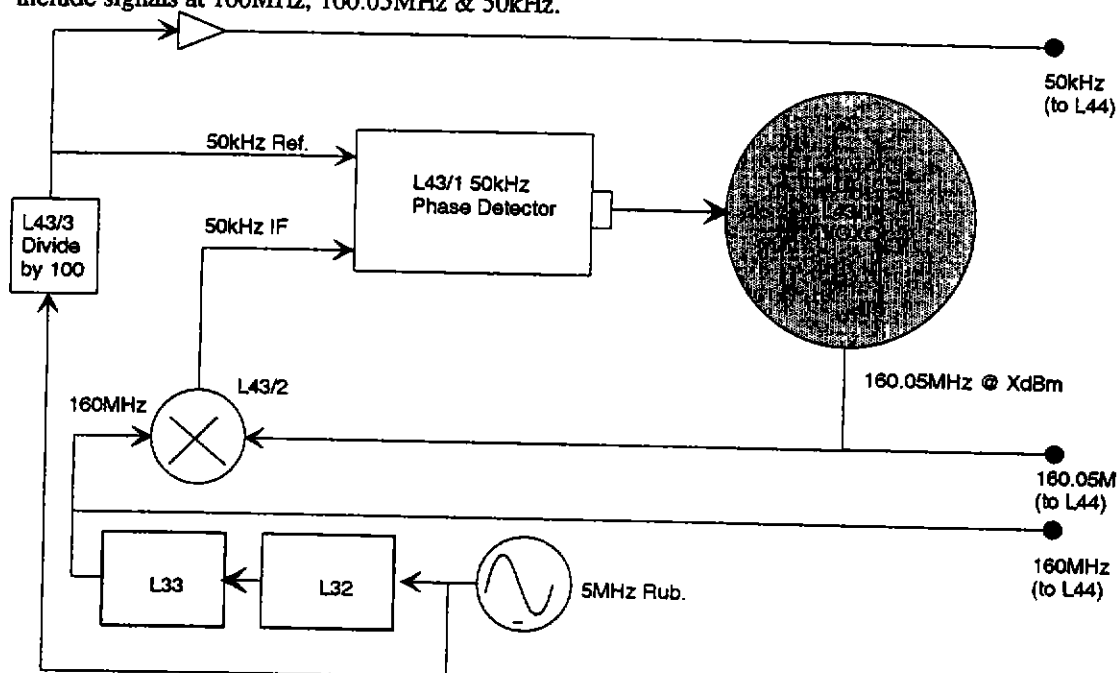
Narrabri Electronics Group  
Allan Young  
Gerry McCulloch

**S/N 000**

## MODULE FUNCTION

The L43 Module is located in the central building (in the screened room). The purpose of this module is to provide 50kHz and 160.05MHz signals to the phase transfer system. The 50kHz is derived simply by dividing down the 5MHz signal (done by the L43/3 module). The 160.05MHz signal is obtained by means of an offset phase locked loop circuit using a 160.05MHz Vectron oven controlled crystal oscillator as the VCXO. The VCXO control voltage is obtained from the L43/1 50kHz phase detector module. This module detects the difference in phase of the 50kHz from the divider (L43/3) and the 50kHz output of the L43/2 (160.05MHz loop module). This module is used to mix the 160.05MHz and 160MHz signals together to give a 50kHz signal.

This module has as inputs the station reference 5MHz, and 160MHz from an L32, L33 chain. Outputs include signals at 160MHz, 160.05MHz & 50kHz.



L43 MODULE FUNCTION

## SUBASSEMBLIES

### L43/1 50kHz phase detector

#### Overview

#### Description

#### Interface

#### INPUTS:

OUTPUTS:  
CONTROL  
ACCESS -





## MONITOR

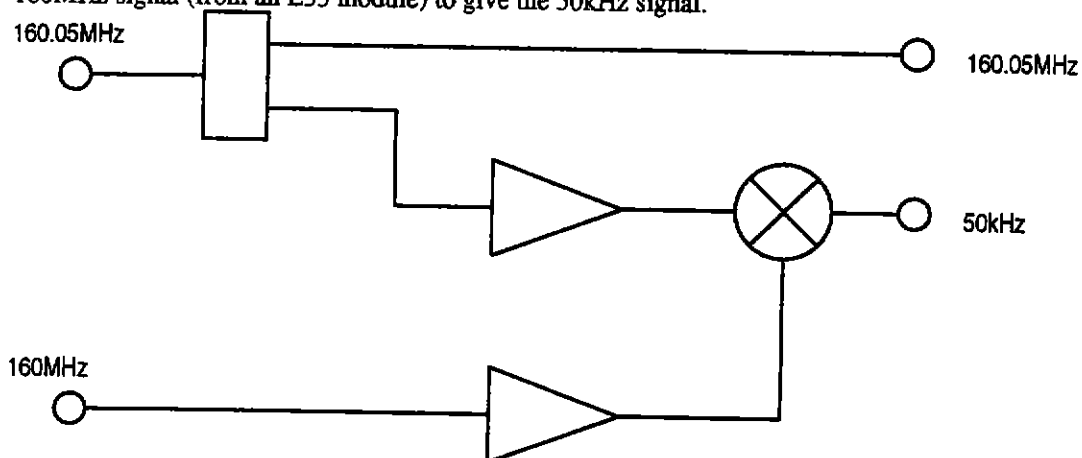
ACCESS -EXTERNAL ACCESS:

**L43/2 160.05MHz Loop.**Overview

This module is used to extract the 50kHz signal from the 160.05MHz VCXO in order to lock the VCXO to the Rubidium 5MHz (divided down to 50kHz using the L43/3) using an offset PLL technique.

Description

The module uses a 2 way splitter (a MCL PSC-2-1) to extract 160.05MHz from the main signal. This signal is then attenuated and amplified (to provide isolation) and then mixed with a 160MHz signal (from an L33 module) to give the 50kHz signal.

**L43/2 160.05MHz Loop**Interface

## INPUTS:

160.05MHz (from Vectron VCXO).

160MHz (from L33).

## OUTPUTS:

160.05MHz (line).

50kHz (IF to L43/1 - 50kHz Phase Detector).

## CONTROL

None.

## MONITOR

## POWER.

+15V

Gnd.

?

?

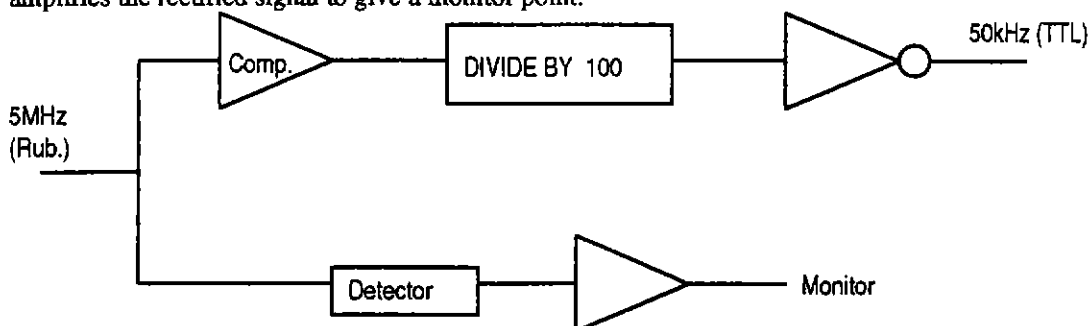
**L43/3 DIVIDER**Overview

This module consists of two parts, a comparator and a divide by 100 counter circuit to give 50kHz from the Rubidiums 5MHz. And a monitor to look at the level of the 5MHz signal.

Description

The comparator divider circuit consists of an Am686 comparator chip to square up the 5MHz signal, this is then simply fed into a cascaded pair of decade counters (a 74LS390), and then through an inverting buffer (a 74LS04). There is also a +/-5V regulator on board to provide power for the Am686

The 5MHz monitor rectifies the 5MHz signal using a simple diode detector type circuit, and then amplifies the rectified signal to give a monitor point.

**L43/3 DIVIDER**Interface

## INPUTS:

5MHz (from Rubidium)

## OUTPUTS:

50kHz TTL (to L43/1 - phase detector).

## CONTROL

None

## ACCESS -

None

## MONITOR

5MHz level

## POWER

+9V, -9V, +15V, -15V, GND

**L43/4 Vectron 5MHz VCXO**Overview

This is a self contained double oven ultra stable VCXO

## DESCRIPTION

As per the data sheet: CO-2475510-VWL2 @ 5MHz with SMA connector

Alignment/Locking/Installation

Before operation the Vectron should be powered up for several hours to allow oven stabilization. Note that the specifications suggest 30min. However in practise this is not necessarily the case.



If the Vectron will not lock (i.e. "out of range" and "out of lock" are on) then, providing there is no other problems, the Vectron has most likely aged to the point where it needs a frequency adjustment. This can be done by monitoring the 50kHz TTL signal levels to U5 in the 50kHz PLL circuit whilst adjusting the tuning screw on the Vectron. By adjusting the tuning screw to a middle point between where the TTL signals are slipping one way and the other the Vectron should lock up.

When this is done the integrator output signal (pin 6 on U11) should be monitored and the Vectron adjusted until this level is approximately 0VDC. At this point the Vectron should be realigned with the frequency of the Rubidium.

If the VCXO integrator out signal is reading high (greater than a magnitude of several volts). The Vectron's oscillation frequency can be adjusted by installing the L42 on an extender module and monitoring pin #10 of the 100 pin connector whilst adjusting the Vectron via the tuning screw to give an output of approximately 0V. Care should be taken however to ensure that the Vectron has warmed up (in its position in the rack).

## Interface

### INPUTS:

24V supply.

### OUTPUTS:

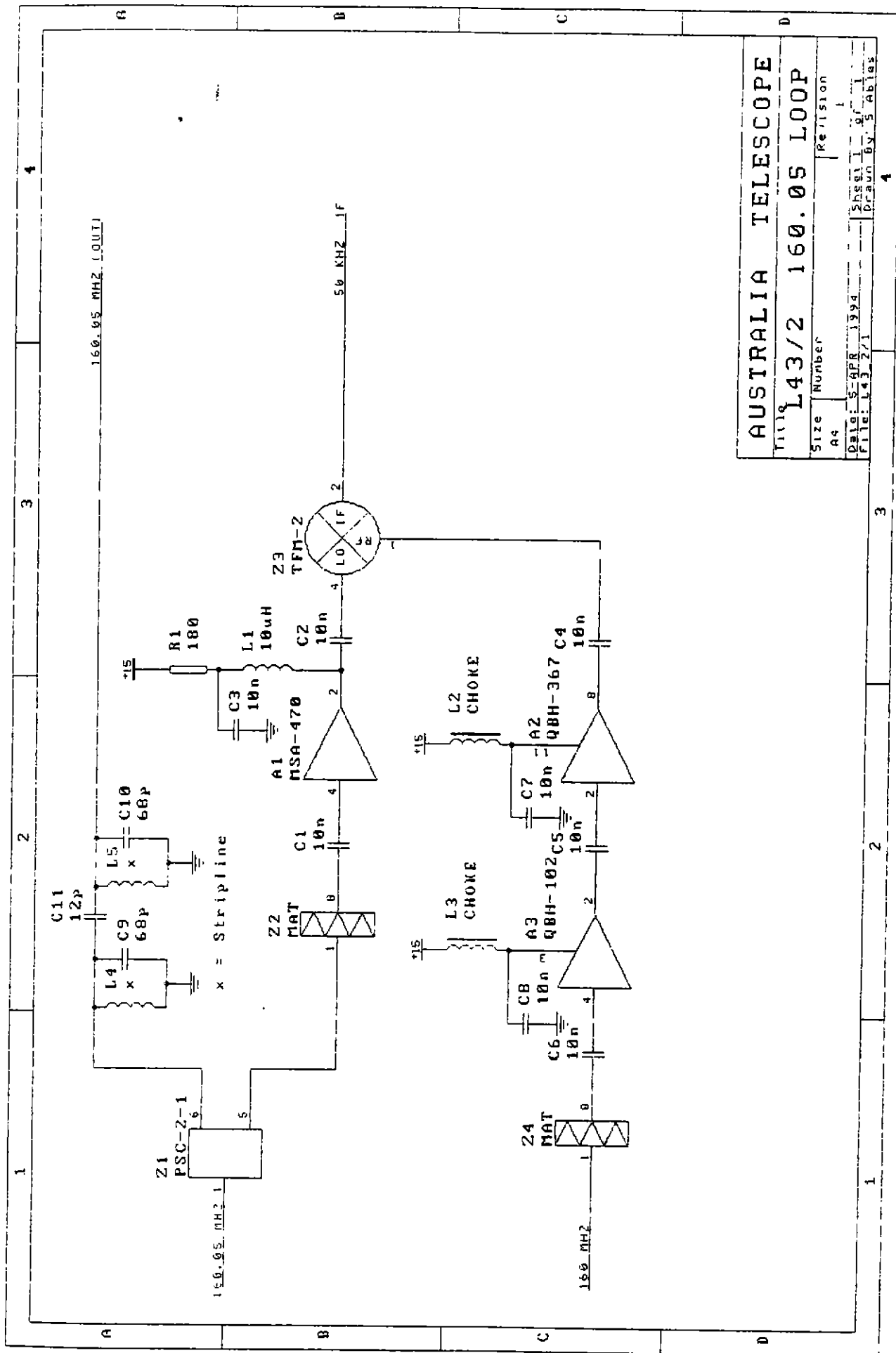
10-14dBm 5MHz signal

### CONTROL/MONITOR

Bias from Phase Detector module (L42/1).

Temperature Monitor.





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L43/2 160.05 LOOP

Size Number Revision

As

Date: 5-APR-1994

File: L43/2/1

Sheet 1 of 1

Drawn by: S. Ables



# **Low Phase Noise 5MHz PLL Module L42**

## **TECHNICAL MANUAL**

### **Design/Construction:**

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### **Documentation:**

Narrabri Electronics Group  
Allan Young  
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**S/N 000**

## MODULE DESCRIPTION

This purpose of this module is to provide the 5MHz reference signal for each of the individual antennas' Local Oscillator systems.

Because of the phase tracking requirements of the Compact Array, this local reference must be locked to a central reference signal to provide tracking across the array. This is done by phase locking the antenna's reference oscillator (a 5MHz "Vectron" VCXO oscillator) which has extremely low phase noise (see specs.) to the central site 5MHz. Because of signal transmission instabilities the central reference signal is transmitted in two components, one at 160.5MHz and the other at 50kHz. The L41 module derives two 50kHz signals from a combination of these and a locally derived 160MHz signal, these two signals are used in the L42 module to complete the phase locked loop, as shown in figure 1.1

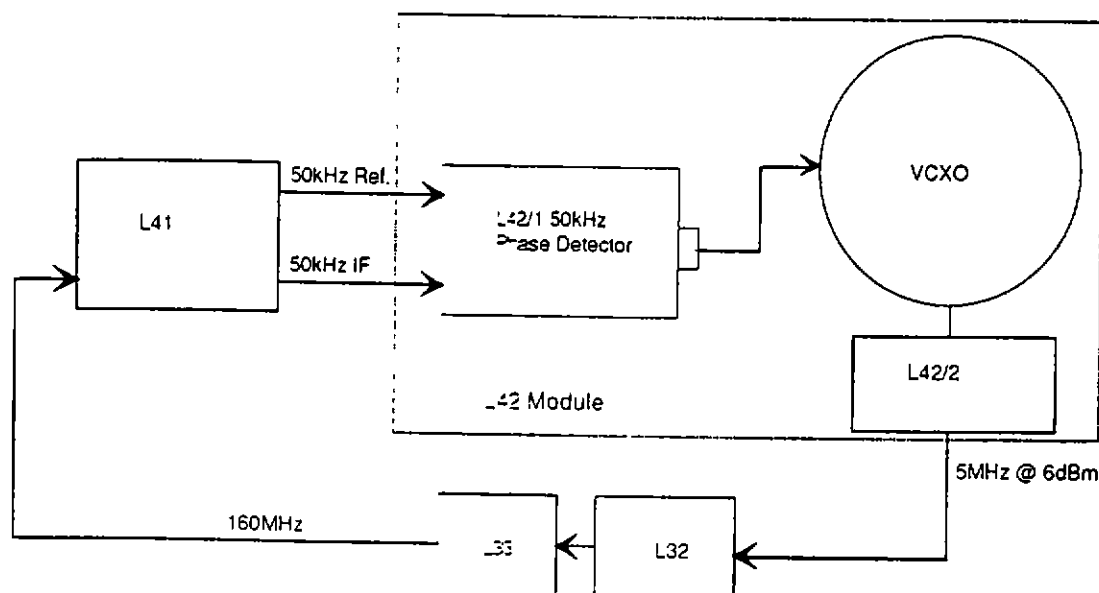


Figure 1.1. MODULE FUNCTION

## SUBASSEMBLIES

### L42/1 50kHz Phase Detector

#### Overview

A standard 'AT' phase detector board operating at 50kHz.

#### Description

The purpose of this module is to compare the phase of the 50kHz reference coming from the Central Site (via the L41 module) and produce a driving voltage to control the VCXO to ensure accurate phase tracking of the reference signal. The module itself consists of the following parts:

The input/conditioning stage is made up of two LM311 comparator circuits (U1 & U2 and their associated parts) which condition the I.F. and reference signals to produce two ideally digital signals. These two signals are then compared using an MC4044 digital Phase-Frequency Detector (U5). The output of this IC is then integrated using a combination of U6 & U7 which form a filter with a response as shown in figure 2-1.

The rest of this module consists of monitoring circuits (see for 'OUTPUTS'), and a hold circuit consisting of U8, which sets up a constant preset level onto the Integrator output signal to ensure that the VCXO remains at the same frequency when there is no reference signal present.

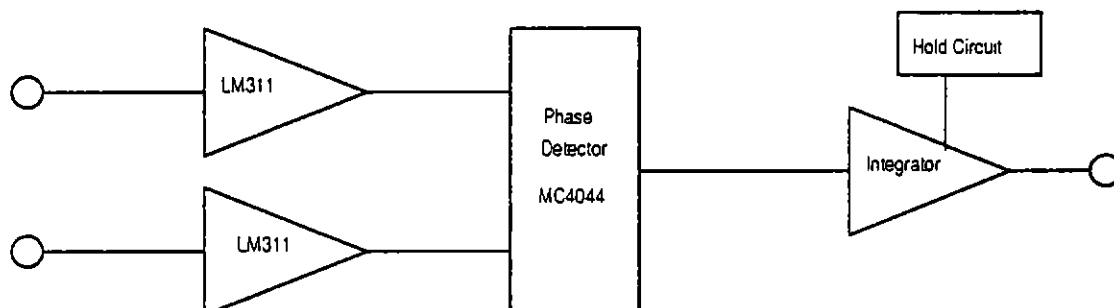


Figure 2-1. PHASE DETECTOR

#### Interface

##### INPUTS:

IF & REF. signals at 50kHz

##### OUTPUTS:

Integrator output (to Vectron controller board).

##### CONTROL:

Control Hold.

'A'/'B'

##### MONITOR:

###### Analog:

Angle Error.

Integrator Output.

REF. & IF. Levels.

###### Digital:

Out of Range. ( Display & Dataset)

Out of Lock. ( Display & Dataset)





## L42/2 5MHz Splitter

### Overview

The 5MHz splitter module uses a combination of a 2-way and a 4-way splitter to produce three 5MHz signals (of 0, 6 & 15dBm) and two series decade counters to divide the signal down to give a TTL 50kHz output. This 50kHz output is not used however.

### Description

This module takes as its input the (+12dBm ??? +10dBm) from the 5MHz Vectron VCXO. This signal is then split using a 2 way 0° splitter to give a 5 MHz reference signal (used in the L32) and another signal which is attenuated, then amplified and split again. This second signal is split 4 ways using a Mini-Circuits PSC-4-3 splitter.

Of the outputs from the 4 way splitter, none are actually used. One goes through a AM686 comparator and two cascaded decade counters (a 74LS390) to give a TTL 50kHz signal. The next output is for the 5MHz phase meter in the L41 module (which doesn't exist). The next is simply terminated to a 50  $\Omega$  resistor. The final output is just a spare (at +15dBm).

### Interface

The L42/2 module has no external interface.

#### INPUTS:

5MHz (SMA)

#### OUTPUTS:

50kHz TTL SMA

5MHz for Meter - SMA connector

5MHz (spare)

5MHz (reference) - SMA connector

CONTROL/MONITOR: None.

POWER: +15V, +5V, -5V, GND.

## L42/3 Vectron 5MHz VCXO

### Overview

This is a self contained double oven ultra stable VCXO

#### DESCRIPTION

As per the data sheet.

CO-2475510-VWL2 @ 5MHz with SMA connector

### Interface

#### INPUTS:

24V supply.

#### OUTPUTS:

10-14dBm 5MHz signal

#### CONTROL/MONITOR

Bias from Phase Detector module (L42/1).

Temperature Monitor.

### Alignment/Locking/Installation

Before operation the Vectron should be powered up for several hours to allow oven stabilization. Note that the specifications suggest 30min. However in practise this is not necessarily the case.



If the Vectron will not lock (i.e. "out of range" and "out of lock" are on) then, providing there is no other problems, the Vectron has most likely aged to the point where it needs a frequency adjustment. This can be done by monitoring the 50kHz TTL signal levels to U5 in the 50kHz PLL circuit whilst adjusting the tuning screw on the Vectron. By adjusting the tuning screw to a middle point between where the TTL signals are slipping one way and the other the Vectron should lock up.

When this is done the integrator output signal (pin 6 on U11) should be monitored and the Vectron adjusted until this level is approximately 0VDC. At this point the Vectron should be realligned with the frequency of the Rubidium.

If the VCXO integrator out signal is reading high (greater than a magnitude of several volts). The Vectron's oscillation frequency can be adjusted by installing the L42 on an extender module and monitoring pin #10 of the 100 pin connector whilst adjusting the Vectron via the tuning screw to give an output of approximately 0V. Care should be taken however to ensure that the Vectron has warmed up (in its position in the rack).

## Temperature Monitor.

### Overview.

The temperature monitor is a small board which measures the internal ambient temperature of the module. It was not intended as an exact temperature monitor. Rather, it was intended to give some indication of the temperature, and to be able to monitor temperature changes. It was thought that this might be useful for tracking down any problems which seem to be temperature related.

The output is an analogue voltage of +100mV/°C, with 0V at 0°C.

### Description

This circuit is taken from the Precision Monolithics Inc. (PMI) databook. This circuit shows two trim pots, and some carefully chosen resistor values. For our purposes, we decided that the voltage trimming pot was unnecessary, and that we could obtain sufficient accuracy and linearity using only the remaining pot, and standard value resistors.

The temperature sensor is the PMI voltage reference, REF-02CJ. The CJ version was chosen because it was a good compromise between cost and the accuracy of the internal reference output. As well as having a +5V voltage reference output, it also has a temperature output of 2.1mV/°C.

At 0°C, the output voltage of the sensor is 580mV. Thus, the op-amp and its associated components must perform two functions - they must "buck-off" this 580mV, to give 0V at 0°C, and they must provide sufficient gain to amplify the 2.1mV/°C of the sensor, to 100mV/°C for the output. These two functions are accomplished with three resistors, and the trim pot for adjustment.

The setting of the trim pot affects both the indicated value at the calibration point, and the slope of the output voltage over the full temperature range. (For our application, both of these are not so important. We are only interested in a small temperature range between about 20°C and 35°C, and relative changes were more important than absolute temperatures.)

The combination of R4, R6 and VR1 give a sample of the reference voltage equal to the sensor output voltage at 0°C. This is about 580mV. This voltage is then applied to the inverting input of the opamp, and the sensor voltage is applied to the non-inverting input. Thus, the opamp is taking the difference between these two voltages and, regardless of the gain of the opamp, the output voltage should be 0V at 0°C.

Feedback is then added to the opamp, so that the 2.1mV/°C of the sensor is amplified to 100mV/°C for the output. The opamp gain is approximately  $(1 + R6/(R4 + VR1))$ , and should be about 47. R3 is to protect the opamp from damage should its output be shorted to ground, or accidentally applied to any other voltage.

As can be seen, the value of VR1 is common to both the offsetting and the gain, explaining the necessary compromise.



### Adjustments.

The circuit is adjusted by putting a Fluke temperature probe on the case of the REF02CJ, and setting the trimpot so that the output voltage agrees with the temperature as measured by the Fluke. Therefore, the output is calibrated at one room temperature point only, and no attempt is made to check or adjust the slope of the output voltage.

### Schematic.

see circuit diagram L--/047/01.

### **Regulator Board.**

The L42 module uses a Mark 5 regulator board, with the additional regulator being at +24V.

### **Address Board.**

#### Description

In this module, the address board is used to enable the dataset to read the module's serial number and version code, to implement the Bin Wired OR function ("monitor out of lock" feature of the phase detector).

The eight bit serial number read via the bus consists of two parts- the six bit serial number of the module, and a two bit version number. The serial number is set by drilling out links on the PCB, and is intended to be permanent. The version number is set by links on headers, and is easily changed. All modules initially had "0" as the version number.

Dataset signals, which enter the module via the 100 pin connector, have been grouped in a way which allows a 26 conductor ribbon and mass termination connectors to be used for the dataset bus and Bin Wired OR wiring. This ribbon begins at the 100 pin connector and, in this module terminates at the address board.

There are no adjustments, although the serial number and version number of the particular module must be encoded.

#### Operation

The dataset address bus has six bits. In line with LO system convention, the lower four bits (BADD0...3) are used to set the address of a module's position along a bin, and the upper two bits (BADD4,5) are used to address registers within a module. In this module, BADD4 and BADD5 are not used. The code for a particular position along a bin is hardwired into the rack wiring, and consists of links between particular pairs of pins on the 100 pin connector. When a module is placed in the rack, this code forces some of the "B" inputs of U1 (74LS85) to be grounded. The "A" inputs are connected to the BADD0...3 of the dataset. Resistors in the RP2 SIP package are pull-up resistors on all the inputs of U1. When the code from the dataset on the address lines, and the code wired into the 100 pin rack connector match, U1 pin 6 goes HI. This is then ANDed with the STrobe from the dataset in U2B, to give a signal called Decoded STrobe. U2C is a simple inverter. U2 (74LS03) are open collector gates, so two resistors in the RP2 SIP package are the output pull-up resistors.

To read the serial number, U3 (74ALS541) is taken out of the high impedance mode when the RD/WR line (pin 1) and the Decoded STrobe (pin 19) are both LO. This then impresses the code present on the input side of U3 across the data lines, where it is able to be read by the dataset. SIP package RpP1 are pull-up resistors on all the inputs of U3.

When the Address Board was manufactured, all serial number bits were connected to ground, giving a serial number of "00H". Links on the two headers were also installed to give a version number of "0H". The serial number code should not ever need changing.

The remaining two gates of U2 are used by the Bin Wired OR circuit. In this module, only one of these two inputs is used. The arrangement of the PCB is such that the unused input has been ground by a link in the power supply wiring. The used input is from the OUT OF RANGE monitor output on the Phase Detector Board. When a level error occurs, the bin Wired OR input is HI???, which sets U2's output LO, indicating a fault condition.



### VCXO Control Board.

This board is mounted on the back of the Vectron mounting panel and is used to interface the Vectron VCXO with the power supply, 100 pin ITT Cannon Connector, and the Phase Detector integrator output.

### Front Panel.

The L42 uses a standard Mark 1 Front Panel board.

"e" is a red LED used to indicate an out of lock condition, while "r" is an orange LED used to indicate an out of range condition. All the resistors are 470  $\Omega$ .

### Dataset Interface

This module communicates to the ACC via dataset 29 and has the following interface points:

Name	Dataset input	Form	Address (on Dataset 29)	Type C=Control M=monitor
Hold				C
Out of Lock	11	Single Bit Digital	75	M
Out of Range	14	Unbalanced Analog	22	M
Angle Error		Unbalanced Analog		M
Integrator Output	12	Unbalanced Analog	20	M
REF. Signal Level	10	Unbalanced Analog	18	M
IF Signal Level	11	Unbalanced Analog	19	M
Module Temperature	15	Unbalanced Analog	23	M
VCXO Temperature.	16?	Unbalanced Analog	24?	M
Version Number				M
Serial Number	0	A08 (address bus)	96	M

### Other Parts

Apart from the listed modules, the L42 module contains a standard ground board.

### L42 Performance



# **Low Phase Noise Narrow Band 5MHz PLL Module L46**

## **TECHNICAL MANUAL**

**Design/Construction:**

Andrew Bish

**Documentation:**

Narrabri Electronics Group

Andrew Bish

**S/N 000**

## MODULE DESCRIPTION

The main purpose of this module is to reduce the close-in phase noise from the 5MHz Phase Transfer System. This is done by phase locking a 5MHz Vectron oscillator which has extremely low phase noise (see specs.) to the central site 5MHz (typically a Rubidium Standard Clock). The module also comes with the option of a 4-way splitter which can be configured to give output levels of up to 10dBm.

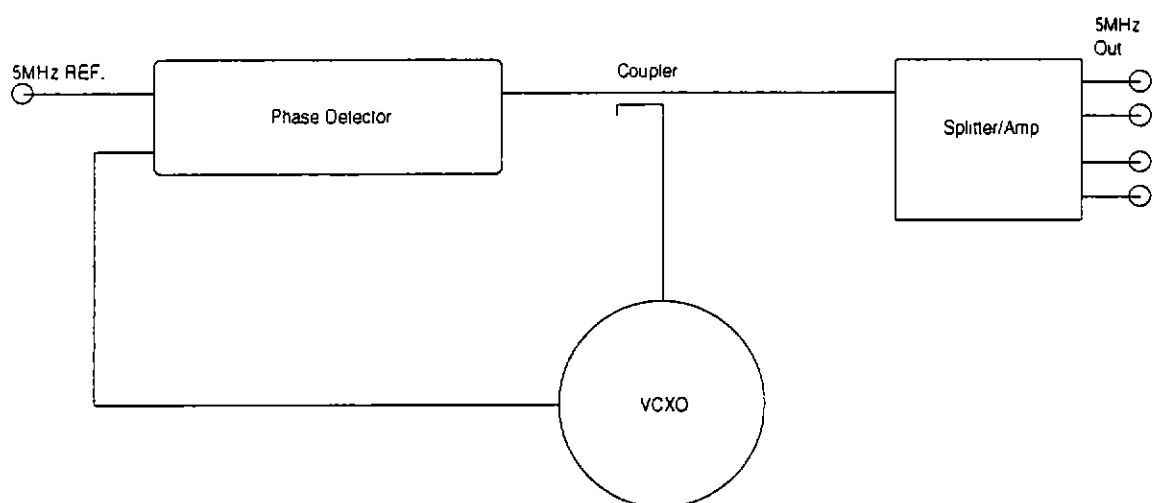


Figure 1-1. MODULE FUNCTION

## SUBASSEMBLIES

### L46/1 5MHz Phase Detector

#### Overview

A standard 'AT' phase detector board operating at 5MHz.

#### Description

The 5MHz phase detector is based on the standard A.T. design, using an MC12040 as the phase detector. See the detailed description of the phase detector in the LO System Manual for a full description of this circuit. What follows are points specific to this phase detector.

The printed circuit board for this detector uses the same component designations and placements as other Mk. 6 phase detector boards, although the input circuit is unique to this circuit.

The IF input to the phase detector is the output of the Vectron VCXO module (coupled off the main signal path by a ZFDC-20-3 Mini Circuits coupler).

On the input circuit, the 47Ω resistor and the single bead choke act as high frequency terminations for the mixer. C4, C6 and L2 form a 7.5MHz low pass filter. The amplifier A1 has been removed as it is not necessary given the reference input signal has no input comb signals.

As etched, the board sets U2 for maximum gain, by joining pins 2 & 7. However, this provides too much gain, and so the link between these pins has been cut, and the gain setting resistor (3k9) soldered across the top of the IC. Because this circuit doesn't require the hold & inverting lock circuits, these have been removed.

The only other major change from the standard board is the fact that the L46 PLL has a bandwidth of only several Hz. Hence the integrator circuit has R71 & C41 modified.

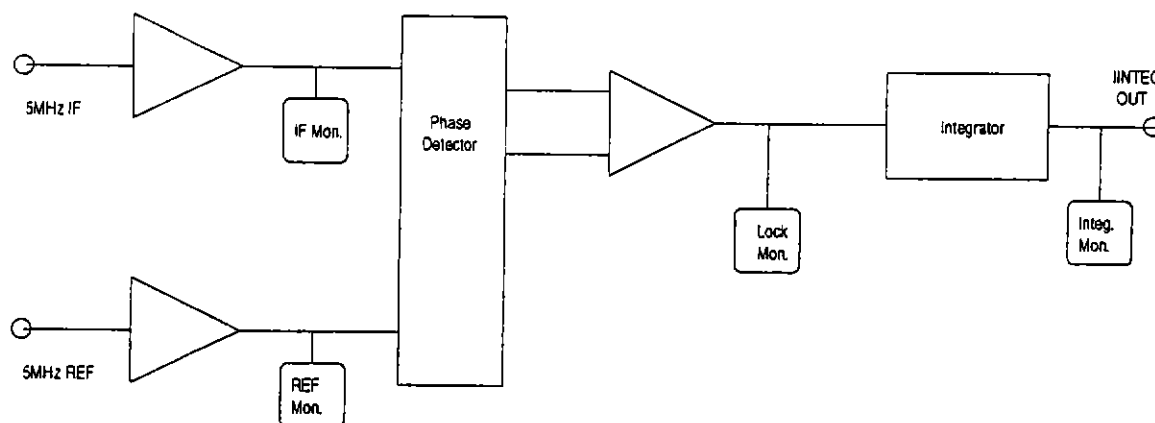


Figure 2-1. PHASE DETECTOR

#### Interface

##### INPUTS:

IF & REF. signals at 5MHz

##### OUTPUTS:

Integrator output (to Vectron controller board).

##### CONTROL:

-

##### MONITOR:

###### Analog:

Angle Error.

Integrator Output.

REF. & IF. Levels.

###### Digital:

Out of Lock. ( Display & Dataset)

Out of Range. ( Display & Dataset)

### L46/2 5MHz Splitter

#### Overview

This module only exists in L46 S/N001 & 3 and is used to provide a distributed 5MHz signal.

#### Description

Standard Splitter module, this one requires a 6dBm input signal and can be configured (using externally mounted attenuator to give outputs of up to around 10dBm. Typical configuration is with 3 6dBm outputs & 1 10dBm output.

This module takes as its input the 5MHz (6dBm) signal from the 5MHz Vectron VCXO.



### Interface

The L46/2 module has no external interface.

#### INPUTS:

5MHz (SMA)

#### OUTPUTS:

5MHz @6dBm SMA

5MHz @6dBm SMA

5MHz @6dBm SMA

5MHz @ 10dBm SMA

CONTROL/MONITOR: None.

POWER: +15V, +5V, -5V, GND.

## **L46/3 Vectron 5MHz VCXO**

### Overview

This is a self contained double oven ultra stable VCXO

#### Description

As per the data sheet.

CO-2475510-VWL2 @ 5MHz with SMA connector

### Interface

#### INPUTS:

24V supply.

#### OUTPUTS:

10-14dBm 5MHz signal

#### CONTROL/MONITOR

Bias from Phase Detector module (L46/1).

Temperature Monitor.

### Alignment/Locking/Installation

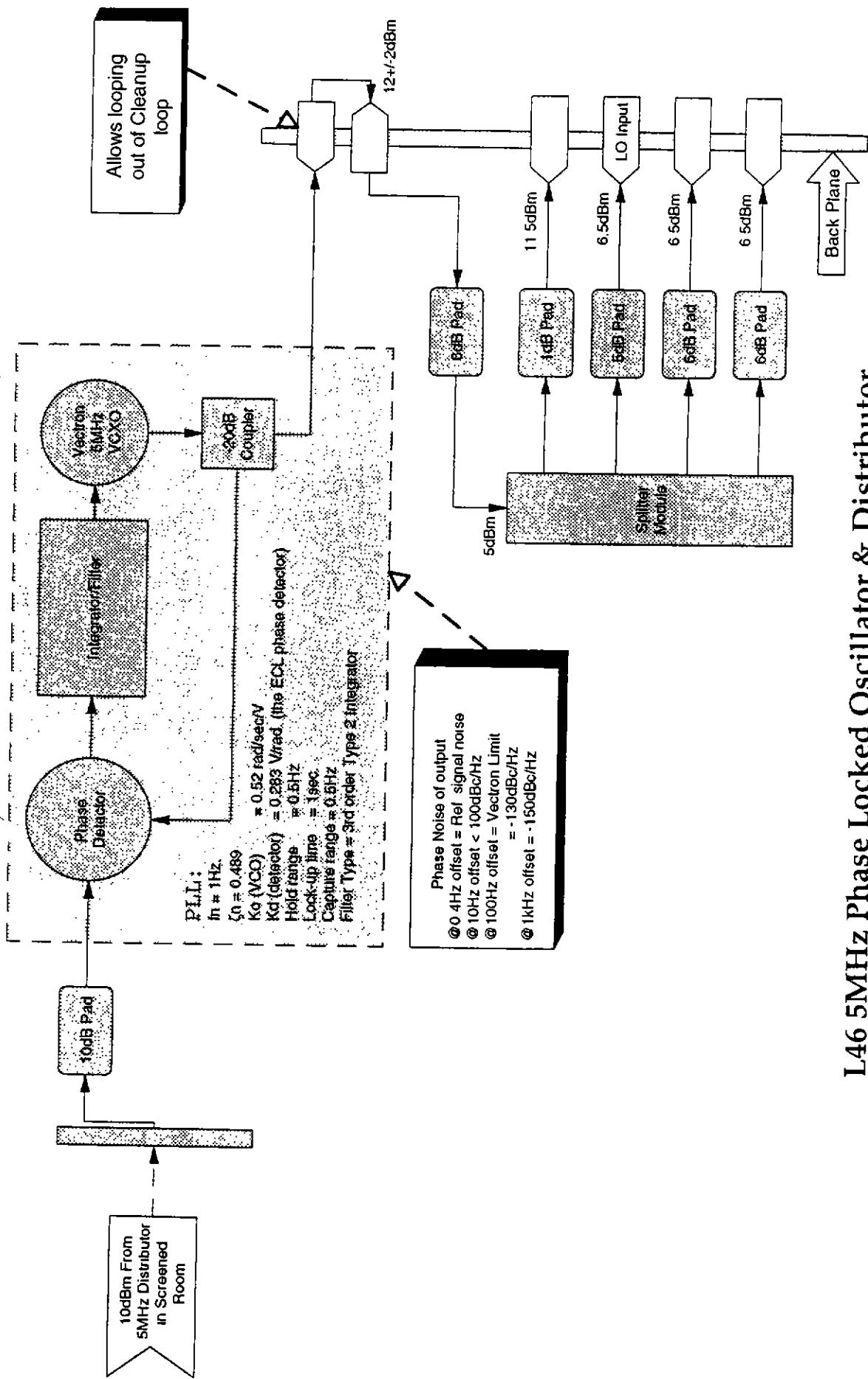
Before operation the Vectron should be powered up for several hours to allow oven stabilization. Note that the specifications suggest 30min. However in practise this is not necessarily the case.

If the Vectron will not lock (i.e. "out of range" and "out of lock" are on) then, providing there is no other problems, the Vectron has most likely aged to the point where it needs a frequency adjustment. This can be done by monitoring the 50kHz TTL signal levels to U5 in the 50kHz PLL circuit whilst adjusting the tuning screw on the Vectron. By adjusting the tuning screw to a middle point between where the TTL signals are slipping one way and the other the Vectron should lock up.

When this is done the integrator output signal (pin 6 on U11) should be monitored and the Vectron adjusted until this level is approximately 0VDC. At this point the Vectron should be realligned with the frequency of the Rubidium.

If the VCXO integrator out signal is reading high (greater than a magnitude of several volts). The Vectron's oscillation frequency can be adjusted by installing the L46 on an extender module and monitoring pin #10 of the 100 pin connector whilst adjusting the Vectron via the tuning screw to give an output of approximately 0V. Care should be taken however to ensure that the Vectron has warmed up (in its position in the rack).





L46 5MHz Phase Locked Oscillator & Distributor



**MOTOROLA**

**MC12040/  
MC12540**

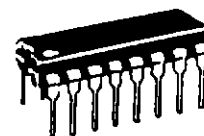
### PHASE-FREQUENCY DETECTOR.

The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

Operating Frequency = 80 MHz typical

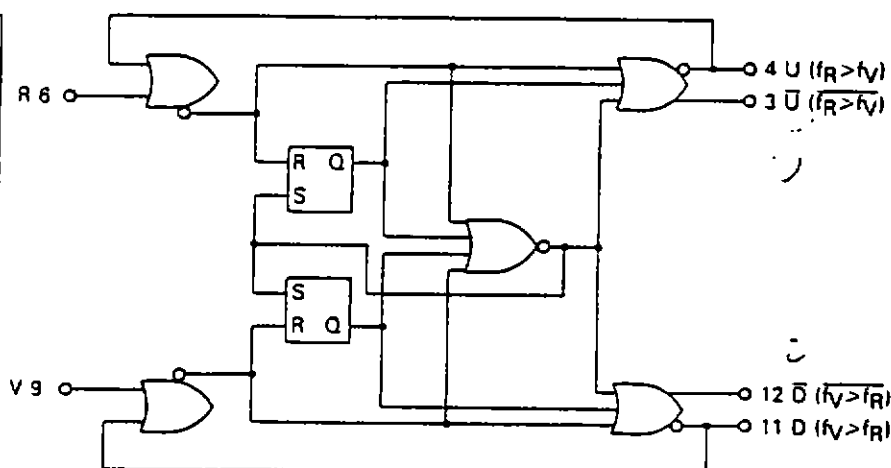
### PHASE-FREQUENCY DETECTOR

P SUFFIX  
PLASTIC PACKAGE  
CASE 648



L SUFFIX  
CERAMIC PACKAGE  
CASE 632-02

### LOGIC DIAGRAM



VCC1 = Pin 1  
VCC2 = Pin 14  
VEE = Pin 7

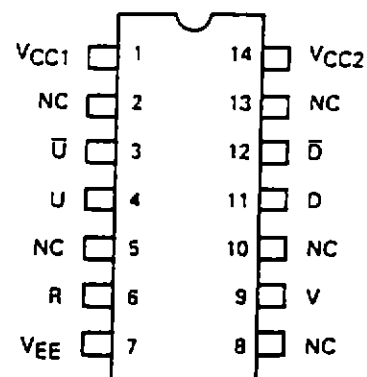
### TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

INPUT		OUTPUT				
R	V	U	D	$\bar{U}$	$\bar{D}$	
0	0	X	X	X	X	
0	1	X	X	X	X	
1	1	X	X	X	X	
0	1	X	X	X	X	
1	1	1	0	0	1	
0	1	1	0	0	1	
1	1	1	0	0	1	
1	0	1	0	0	1	
1	1	0	0	1	1	
1	0	0	0	1	1	
1	1	0	1	1	0	
1	0	0	1	1	0	
1	1	0	1	1	0	
0	1	0	1	1	0	
1	1	0	0	1	0	

X = Don't Care

### PIN ASSIGNMENT



NC — No Connection

## APPLICATIONS INFORMATION

The MC12040 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of  $\pm 2\pi$  radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 1), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 1), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle — that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage-controlled oscillator can be developed. A circuit useful for this function is shown in Figure 2.

Proper level shifting is accomplished by differentially

driving the operational amplifier from the normally high outputs of the phase detector ( $\bar{U}$  and  $\bar{D}$ ). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched "1" levels from the phase detector). The  $\bar{U}$  and  $\bar{D}$  outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R-C filtering imbedded within the input network (Figure 2) may be very beneficial since the very narrow correctional pulses of the MC12040 would not normally be integrated by the amplifier. General design guides for calculating R1, R2, and C are included in the MC4044 data sheet. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplifier, mismatching of nominally equal resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16 mV offset voltage in the amplifier would cause an error of  $0.016 / 0.16 = 0.1$  radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 2). Phase error over temperature depends on how much the offsetting parameters drift.

FIGURE 1 — TIMING DIAGRAM

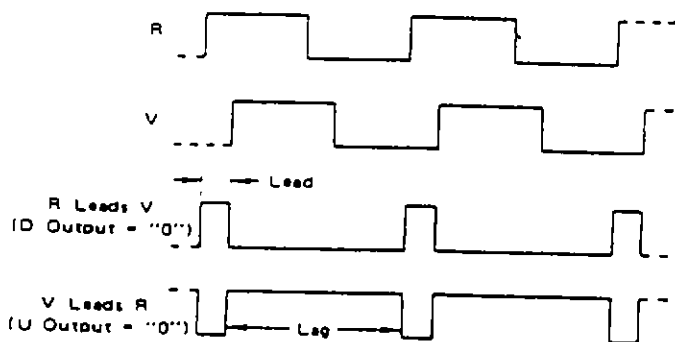
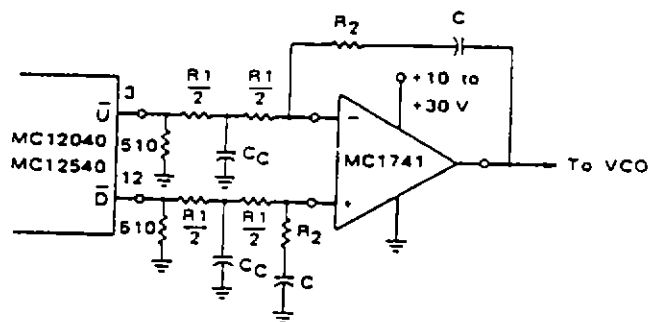


FIGURE 2 — TYPICAL FILTER AND SUMMING NETWORK





**TOROLA**

**MC4344/  
MC4044**

## PHASE-FREQUENCY DETECTOR

The MC4344/4044 consists of two digital phase detectors, a charge pump, and an amplifier. In combination with a voltage controlled multivibrator (such as the MC4324/4024 or MC1648), it is useful in a broad range of phase-locked loop applications. The circuit accepts TTL waveforms at the R and V inputs and generates an error voltage that is proportional to the frequency and/or phase difference of the input signals. Phase detector #1 is intended for use in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired. Phase detector #2 can also be used to indicate that the main loop, utilizing phase detector #1, is out of lock.

Input Loading Factor: R, V = 3

Output Loading Factor (Pin 8) = 10

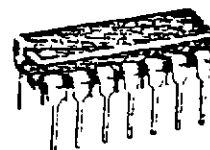
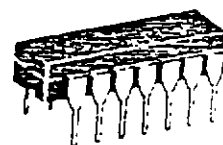
Total Power Dissipation = 85 mW typ/pkg

Propagation Delay Time = 9.0 ns typ  
(thru phase detector)

## PHASE-FREQUENCY DETECTOR

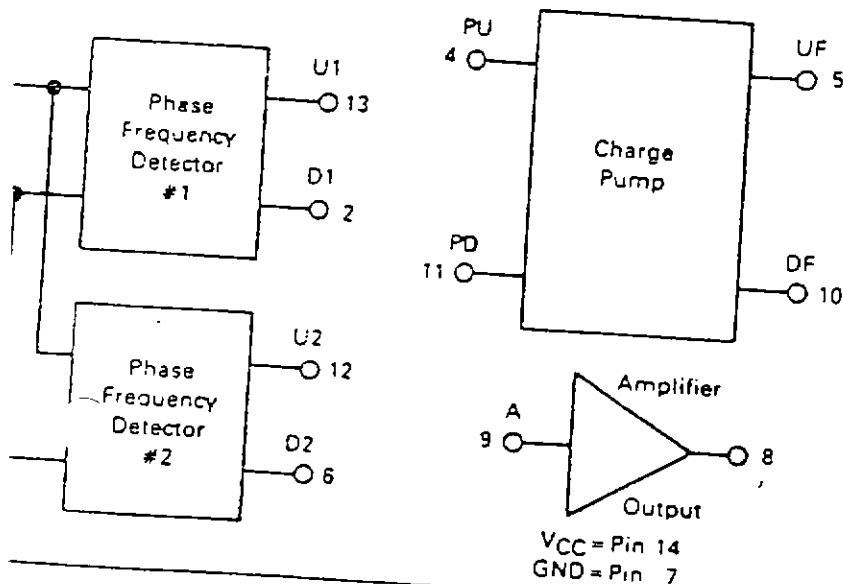


L SUFFIX  
CERAMIC PACKAGE  
CASE 632  
(TO 116)

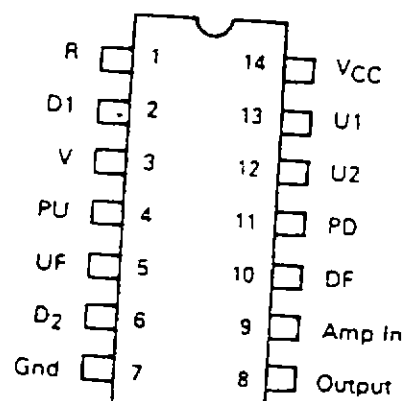


P SUFFIX  
PLASTIC PACKAGE  
CASE 646  
MC4044 only

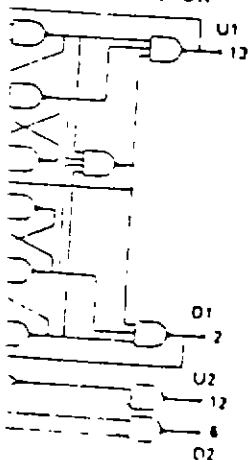
## LOGIC DIAGRAM



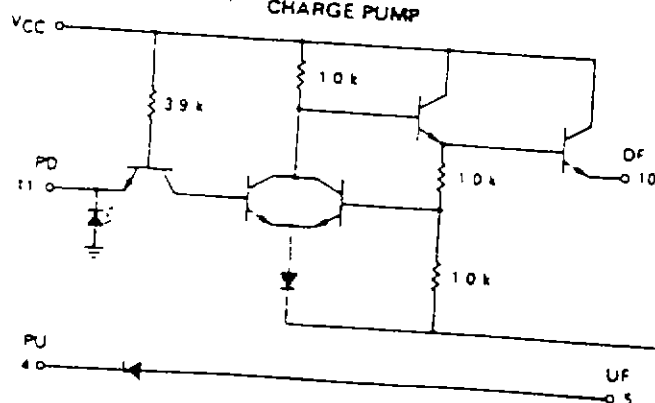
## PIN ASSIGNMENT



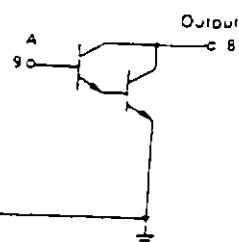
## PHASE DETECTOR



## CHARGE PUMP



## AMPLIFIER

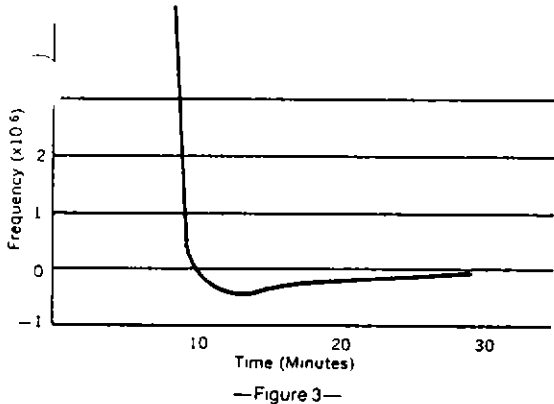




## Controlled Crystal Oscillators

### Warmup

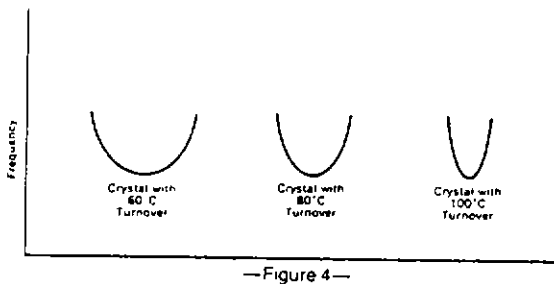
When an oscillator is initially turned on at room temperature the frequency is extremely high relative to the output frequency after the oven stabilizes, typically by  $30 \times 10^{-6}$ . This is simply due to the fact that the frequency of an AT cut crystal is considerably higher at room temperature than at its upper turnover temperature. As the oven warms up, the crystal frequency rapidly decreases. In standard Vectron oscillators, the oven balances in 10-15 minutes but the crystal displays a rubber-band effect and overshoots its final frequency per Figure 3, prior to stabilizing. Typically, relatively high degree of stability is achieved within 30 minutes after turn-on, this time can be reduced to less than 5 minutes in special fast warm-up designs.



### Turnover Temperature

The oven operating temperature (crystal turnover temperature) must be several degrees higher than the highest ambient temperature in which the oscillator is to operate in order that the oven may maintain good control (considering the internal heat rise generated by the oscillator itself).

However, there are disadvantages associated with high oven temperature operation. First, the crystal's frequency vs. temperature characteristic is sharper with higher turnover crystals resulting in more sensitivity to minute changes in oven temperature as shown in Figure 4.

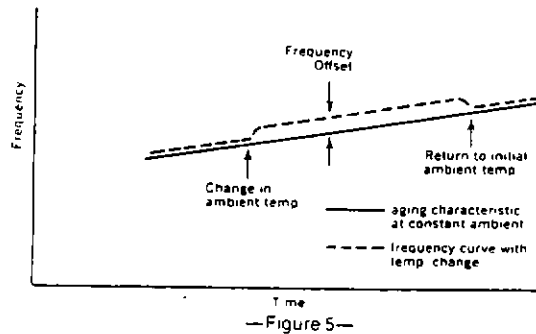


Second, and more important, crystal aging (discussed below) degrades with increasing temperature. Therefore, in designing an oven controlled crystal oscillator, one is faced with a compromise in determining the desired oven operating temperature, it should be as low as practicable, but it must be high enough to provide good control at the maximum ambient operating temperature.

### Stability

**A Aging**—Aging refers to the continuous change in crystal oscillator frequency with time, all other parameters held constant. Prior to delivery, each Vectron oven controlled oscillator is pre-aged until it achieves its specified aging rate. Aging rate is often used synonymously with the word stability; thus, an oscillator with an aging rate of one part in  $10^8$  per day ( $1 \times 10^{-8}$ /day) is sometimes referred to as a one part in  $10^8$  oscillator. This is incorrect terminology, as aging rate (long term stability) must be referred to time, and represents only one facet of oscillator stability.

**B Temperature Stability**—As previously noted, because no oven control system is perfect, a change in ambient temperature causes a small change in output frequency. The frequency shift is an offset from the oscillator's aging curve. This deviation from the normal aging characteristic is not related to time, but is a fixed offset. Thus, the frequency offset vs temperature (temperature stability), for a given temperature change is, for example,  $5 \times 10^{-9}$ , not  $5 \times 10^{-9}$ /day. This characteristic is shown below.

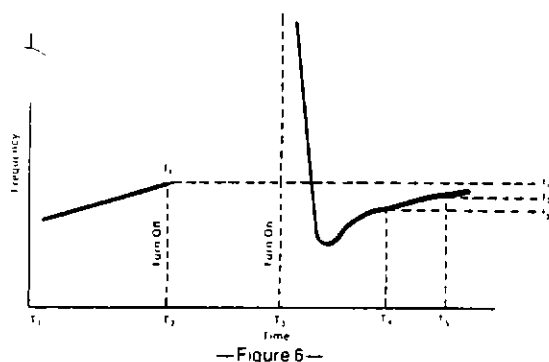


Ambient temperature changes do not produce hysteresis effects; that is, if there is a change in ambient temperature followed by a return to the original temperature, the final frequency will be essentially that which would have resulted had there been no ambient temperature change.

When the required temperature stability is beyond that which can be achieved with a standard proportionally controlled oven, a double oven system can be employed in which the standard oven is housed within a second oven. The outer oven then buffers the ambient temperature changes to the inner oven, which contains the oscillator circuit.

**C Restabilization And Retrace**—When a crystal oscillator is turned off for a period of time and then turned on again (as occurs when the unit is shipped), the crystal requires a restabilization period. The characteristic is similar to the initial factory aging characteristic, but high stability is achieved significantly more quickly because the crystal has been factory pre-aged.

In most applications, oven controlled crystal oscillators are continuously energized. This being the case, aging is the critical characteristic with turn-off/turn-on characteristics being of little or no significance. However, certain applications require that oven controlled crystal oscillators be frequently de-energized and re-energized (a practice which should be avoided whenever possible). When applications require frequent turn-off, an additional series of characteristics should be considered.



In Figure 6, assume that an oscillator is energized until time  $T_2$  when it is turned off for a period of time and then turned on again at time  $T_3$ . Three characteristics may then be of significance:

1. How close does the oscillator return to the output frequency at turn-off, a specified time after turn-on. This is called the retrace characteristic. Retrace error at  $T_4 = f_1 - f_2$ .
2. How much will the frequency change over moderate periods of time (hours) after the oven has stabilized. This is called the restabilization, or warm-up, characteristic. Restabilization rate from  $T_3$  to  $T_5 = (f_3 - f_2)/(T_5 - T_4)$ .
3. How long does it take the oscillator to achieve its specified aging rate following a specified off period.

Many factors affect the retrace, restabilization and reaging characteristics. Proper circuit design and component selection minimize their effects, leaving (1) the crystal and, (2) the length of off-period prior to oscillator turn-on as the prime factors. There is significant variation in these characteristics from crystal to crystal and they should only be specified when absolutely required and then only to the degree needed, as "tight" specifications in this area can have a major impact upon oscillator cost due to low yield. These characteristics are of little consequence in oscillators which are energized continuously.

## Double Rotated (SC and IT Cut) Crystals

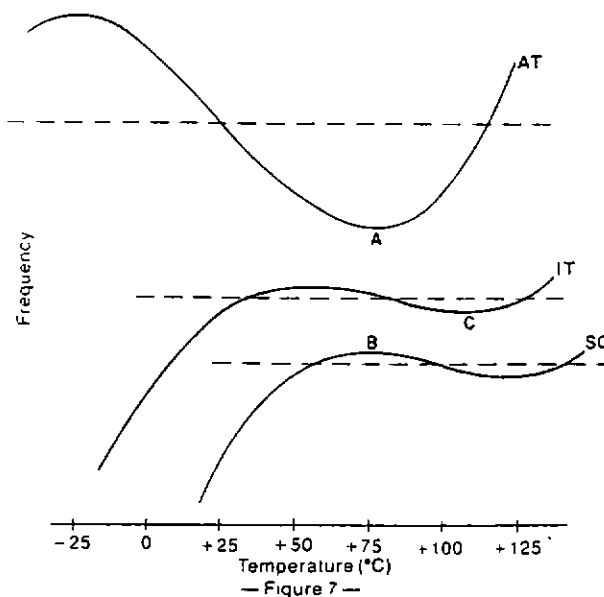
While most high stability crystal oscillators use AT Cut Crystals, SC and IT Cut Crystals are gaining usage in the highest stability HF oven controlled models.

An SC Cut Crystal is one of a family of double rotated AT Cut crystals (quartz crystals cut on an angle relative to two of the three crystallographic axes). Others in the family include the IT Cut and FC Cut, but the SC Cut represents the optimum double rotated design as its particular angle provides maximum stress compensation, hence the name.

Following is a comparison between double rotated (referred to simply as SC for convenience) and AT crystals.

### Advantage of SC Crystals:

1. **Improved Aging.** For a given frequency and overtone (e.g. 10 MHz, third overtone), the SC crystal provides 2:1 to 3:1 aging improvement relative to AT crystals.
2. **Warm-up.** In oven controlled oscillators with a given oven design and turn-on power, the SC crystal achieves its "final frequency" in considerably less time than does the AT crystal.
3. **Phase Noise.** For a given oscillator design, crystal frequency and overtone, the SC crystal provides higher Q and associated improved phase noise characteristics. This improvement only applies close to the carrier as the noise floor is determined by circuit design rather than the crystal.
4. **High Operating Ambient Temperature.** Figure 7 shows the relative frequency-temperature characteristics of AT, IT and SC crystals. The upper temperature turn-over point of the AT crystal ("A" in Figure 7) and lower temperature turn-over point of the SC crystal ("B" in Figure 7) are optimally in the



## Oven Controlled Crystal Oscillators

70°C to 90°C temperature range. Based upon (a) the desired 10°C difference between the highest operating ambient temperature and the crystal turn-over temperature, and (b) the manufacturing tolerance of crystal turn-over temperatures, these crystals are best suited for maximum operating ambient temperatures of 50°C to 75°C. However, the upper temperature turning point of the IT crystal ("C" in Figure 7) is well suited to higher temperature operation and thus the IT crystal is a logical choice for high stability oven controlled oscillators having a maximum operating temperature in the 85°C to 95°C range. Note that while the SC and IT crystal curves are relatively flat at elevated temperatures, their frequency falls off rapidly at low temperatures. Thus, while they serve well in high stability HF oven controlled oscillators, they are generally not well suited for other types of stable crystal oscillators.

**Orientation Sensitivity (tip-over).** When the physical orientation of an oscillator is changed, there is a small frequency change (typically not more than several parts in  $10^{-9}$  for any 90 degree rotation), due to the change in stress on the crystal blank resulting from the gravitational affect upon the crystal supports. Tip-over is expressed in  $10^{-9}/g$  where one g represents one half of a 180° orientation change. The SC crystal is less frequency sensitive to orientation change than is the AT. However, the tip-over difference between AT and SC crystals is not consequential for most applications and this characteristic is usually not a specification consideration.

**6. Spurious Under Vibration** When a crystal oscillator is subjected to vibration, spurious frequencies are generated, offset from the frequency of oscillation by the frequency of vibration. The amplitude of these spurious outputs is related to the amplitude of vibration, the mechanical design of the crystal support, and the mechanical design of the oscillator. The SC crystal produces lower amplitude spurs under vibration than does the AT; however, this characteristic is determined more by the mechanical designs of the crystal and oscillator than by the crystal cut.

### Disadvantages of SC Crystals:

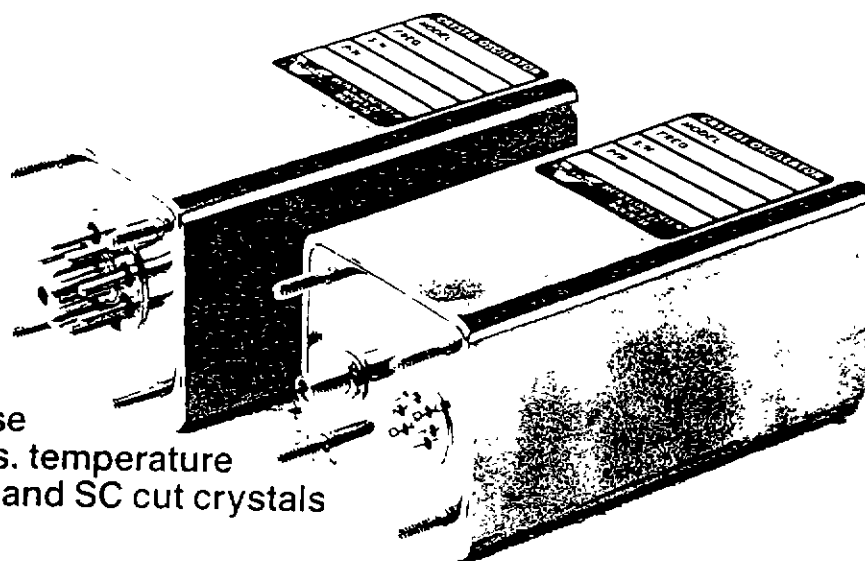
1. **Cost** Because of difficulties associated with tightly-controlled angle rotations around two axes in the manufacture of SC crystals vs one axis for the AT, the SC crystal is several times the cost of an AT of the same frequency and overtone.
2. **Pullability** The motional capacitance of an SC crystal is several times less than that of an AT of the same frequency and overtone, thus reducing the ability to "pull" the crystal frequency. This restricts the SC crystal from being used in conventional TCXOs and VCXOs, or even in oven controlled oscillators requiring the ability to deviate the frequency of oscillation by any significant degree.

In summary, the suitability of double rotated crystals for use in crystal oscillators is essentially restricted to those oven controlled applications where the improved aging, warm-up, and close-in phase noise characteristics justify a significant cost increase.



# **HF Oven Controlled Crystal Oscillators**

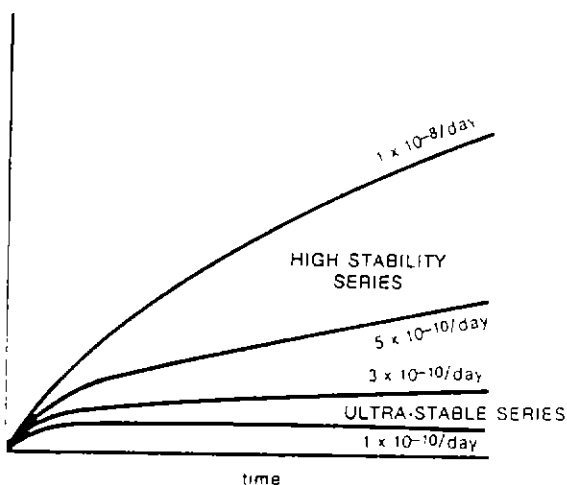
(to 25 MHz)



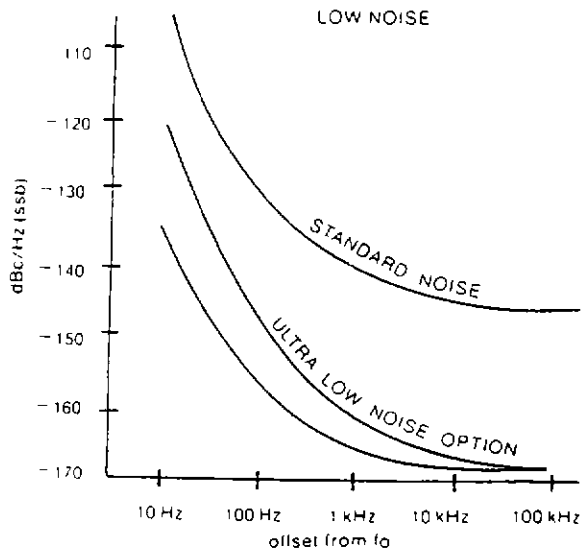
## FEATURES

- Low aging rate
- Low phase noise
- High stability vs. temperature
- Models with AT and SC cut crystals

LOW AGING RATE

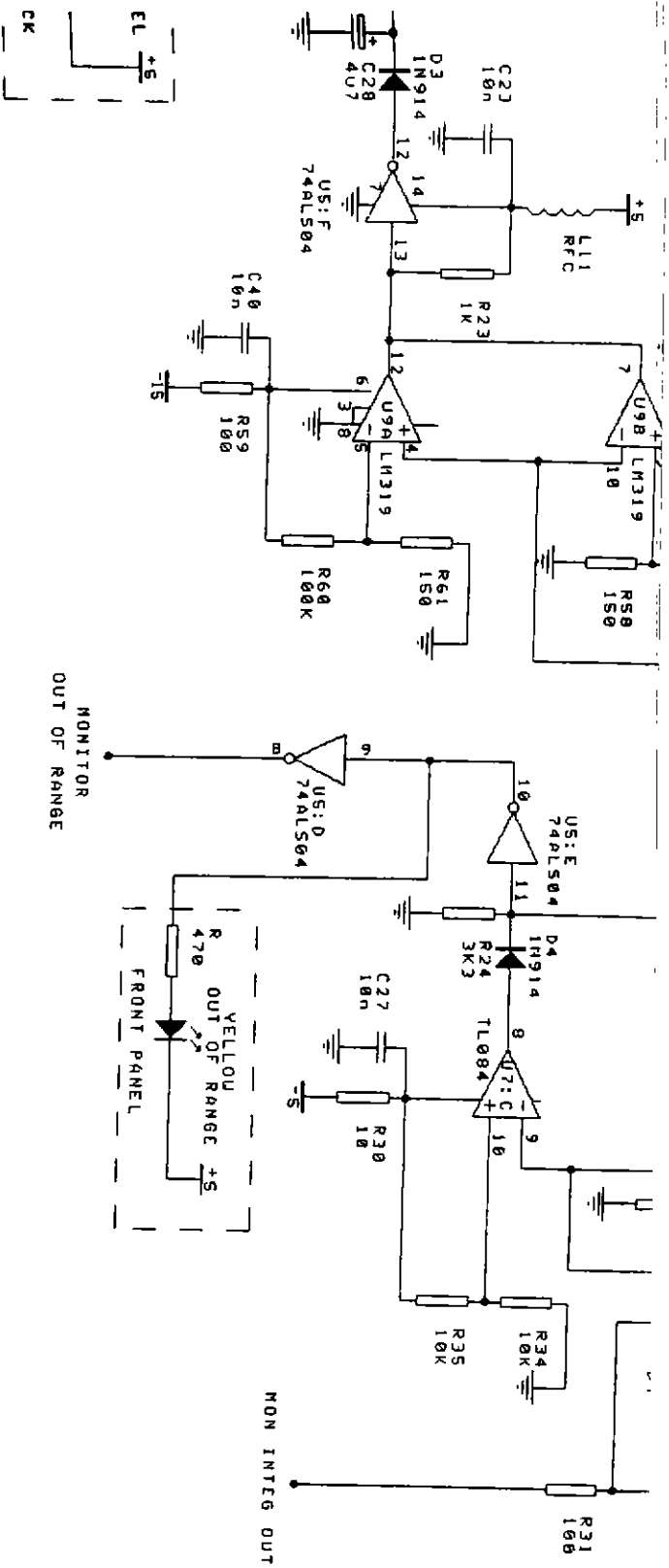


LOW NOISE



 **Turn page for  
Specifications...**





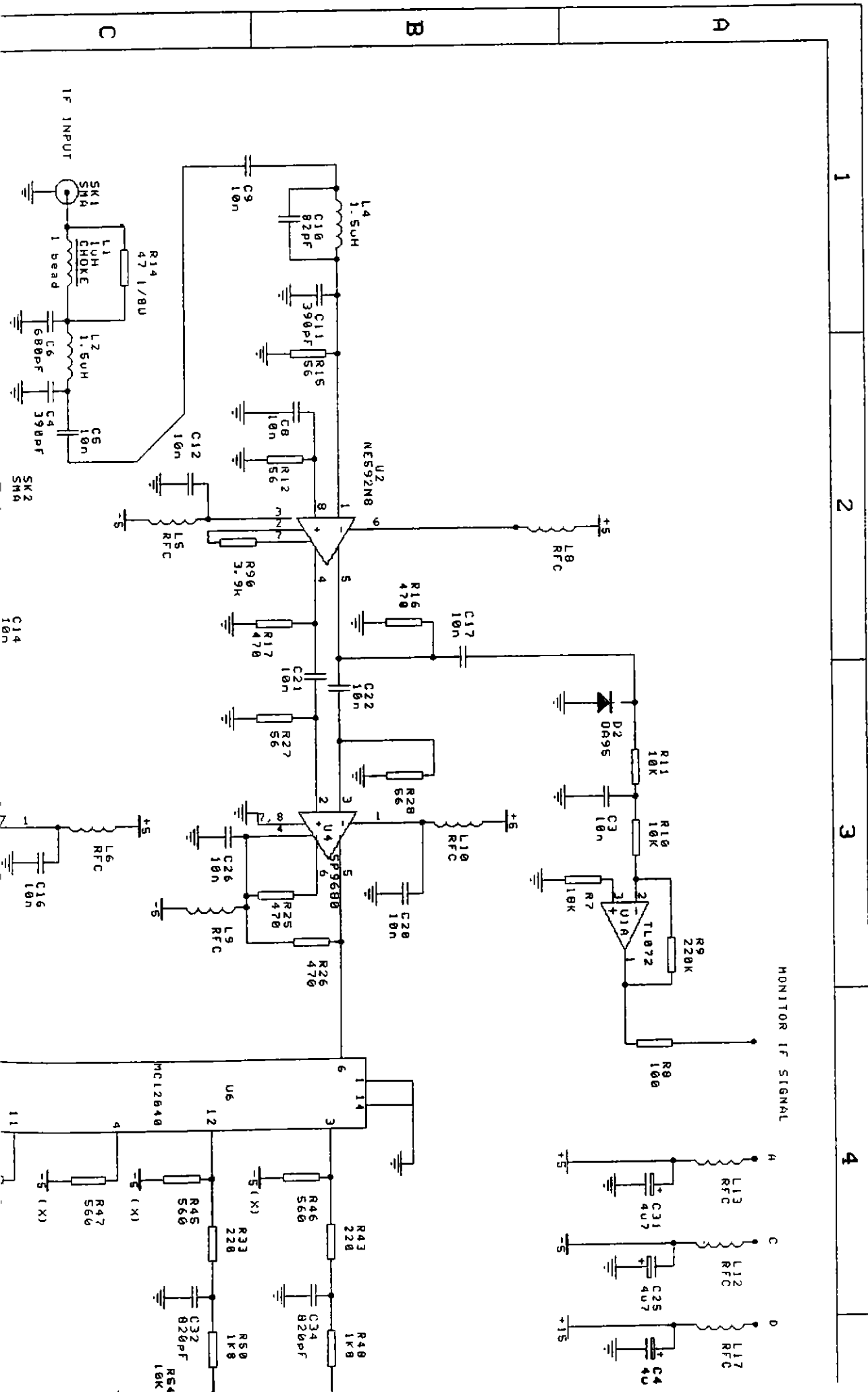
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L46/1 5MHz N/B PHASE DETECTOR	
Size	Number
A2	
Revision	
Date: 20-3-1994	Sheet 1 of 1
File: PDSMHZ/1	Drawn By: SHEPHERD

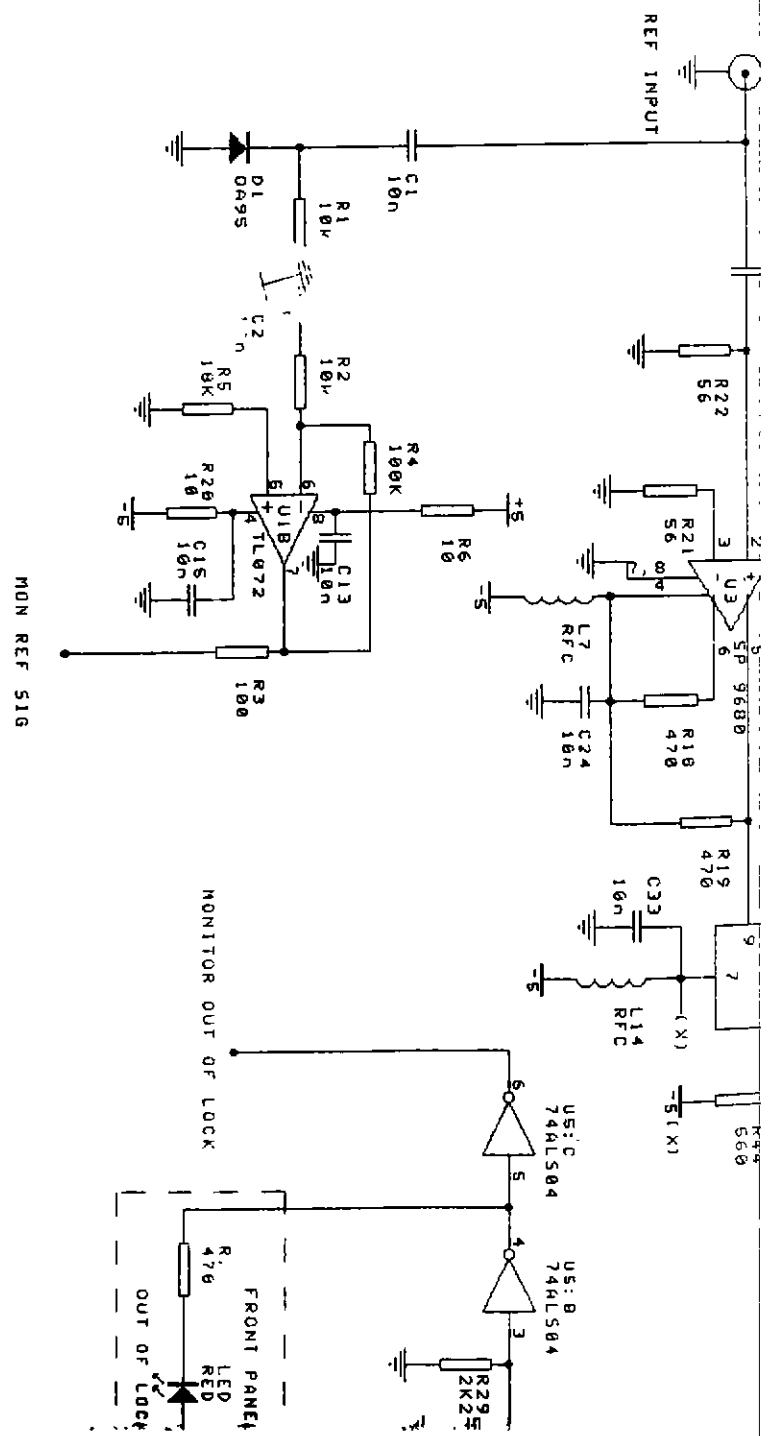
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