LO line stabilisation and the integration clock

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1. LO-line stabilisation.

Fundamental to the operation of the Compact Array is the LO line stabilisation: the machinery which will allow us to maintain constant the relative phases of the LOs at all the antennas. The current design is shown in figure 1.

At the central site there is a 5 MHz oscillator. Its output is multiplied up to 160 MHz for transmission out to the antennas.

At each antenna we have an identical system: 5 MHz oscillator and multiplier. In addition, we have a phase-lock loop, locking the 160 MHz output to the 160 MHz signal transmitted from the central site.

Two phase monitors are used to provide the stabilisation:

1. we transmit the antenna's 160 MHz back to the central site, and measure the phase difference between the central site's 160 MHz and the 160 MHz from the antenna. ($\Delta\phi_{160}$).

2. we transmit the central site's 5 MHz out to the antennas, and measure the phase difference between the antenna's 5 MHz and the transmitted 5 MHz. ($\Delta\phi_5$).

The two quantities, $\Delta\phi_{160}$ and $\Delta\phi_5$, are then used to provide phase corrections to the fringe rotators, samplers and the integration clock start pulses. (In effect, we stabilise the LO line in software).

Suppose the transmission line were to increase its length by ΔL. At the central site we would observe a phase difference :

$$\Delta\phi_{160} = 2\pi\frac{2\Delta L}{\lambda} \qquad \text{(Central site - antenna)}$$

$$\lambda = \frac{c}{160\text{Mhz}}.$$

Tracking $\Delta\phi_{160}$

The thermal coefficient of the LO cable is in the range of 10^{-4} to 10^{-5}/ degree C. Thus there is a possibility that $\Delta\phi_{160}$ may change by more than one turn. This means that we

will need to monitor the long-term trend of $\Delta\phi_{160}$ - a running mean of sin ($\Delta\phi$) and cos($\Delta\phi$), averaged over the previous hour or so will probably suffice.

The 5 MHz phase monitor is needed to keep a check on the 5 - 160 multiplier: there are (160/5 = 32) possible settings of the phase-lock loop; we need to monitor $\Delta\phi_5$ in order to check that a setting jump has not occurred. In effect, we check that

$$\Delta\phi_5 = (\Delta\phi_{160})_{\text{long term average}}/32$$

where $(\Delta\phi_{160})_{\text{long term average}}$ is the software-smoothed average observed by the system. A setting jump is a tragedy: there is no simple cure; a recalibration will be required. It is fervently hoped that no setting jumps will be observed.

An increase in length (ΔL) means that a delay $\Delta\tau = \Delta L/c$ has occurred; we therefore need to advance the LO and samplers by this amount.

Once ΔL has been measured we can correct the fringe rotator and sampler phases:

$$\Delta\phi_{(LO)} = 2\pi f_L \Delta\tau$$

$$= \left(\frac{\Delta\phi_{160}}{2}\right)\left(\frac{f_L}{160\ \text{MHz}}\right)$$

where f_L is the LO frequency, (defined more completely in AT/23.4/012).

similarly,

$$\Delta\phi_{(\text{sampler})} = 2\pi f_s \Delta\tau$$

$$= \left(\frac{\Delta\phi_{160}}{2}\right)\left(\frac{f_s}{160\text{MHz}}\right)$$

where f_S is the sampler frequency. (512, 256 or 128 MHz for 1-, 2-, or 4-bit sampling).

We also need to make some corrections to the Integration clock: the "start pulse" machinery needs to be aware of $\Delta\phi_{(\text{sampler})}$. The scheme which is currently favoured for implementing the start pulses will use a frequency 128 MHz. We will proceed in two steps: choose the start pulse which is correct, modulo the 128 MHz sampling frequency, then adjust the number of samples that the correlator will skip before starting to load samples into the FIFO. This matter is elaborated in section 2.

2. Integration Clock.

This section is a revision of AT/23.4/013 . The reader should consult W.Wilson's document AT/23.4.1/015, which contains the authorised version of the machinery. This note covers the computational (control) requirements.

A. Conceptual Overview of the timing operation.

1. Let the start of an integration period be T (CAT).

2. At each antenna the samplers and LO are started at T - Δ, where Δ is small, several millisecs; this early start will allow these units to have settled down and to be running correctly by the time the integration starts.

3. However, while the sampler will be producing sampling pulses in the interval (T - Δ) to T, no data will be transmitted down the fibres: the data stream will consist of zeroes. (Required by the correlator).

4. On the first valid sample pulse after T the synchronizing pulse train will be sent:- this is a special code that the correlator will recognize as signalling the start of data. Valid data will follow the 4 bit synchronizing pulse train.

Attaching the synchronizing pulse to the correct sampling pulse is difficult - yet it is vital: we cannot afford even a single pulse slippage.

B. Implementation.

1. There are two oscillators, both locked to the LO system: a sampler clock (512, 256 or 128 MHz, for 1-, 2-, or 4-bit sampling), and an Integration clock, at 128 MHz.

The integration clock provides a steady stream of timing pulses. These we count down to provide accurate 5 second markers.

2. In principle, the synchronizing pulse problem is trivial: we simply inhibit the sampling pulses until the 5 second marker, then accept the first sampling pulse to arrive. There are, however, several complications to this scheme:

a. Suppose the marker and the sample pulse both occur at about the same time. If there is any jitter in the system, then we could have a one sample error - of either sign.

b. There will be an offset between the two pulse trains; that is, a delay, ε, will be measured between the edge of the 5 second marker and the nearest sampler pulse when the requested delay is set to zero. This delay is the sum of two effects: a fixed component due to phaseshifts in the 2 oscillator chains; and a (slowly) variable contribution imposed to counter the changes in the phase of the LO itself (the LO-line stabilisation problem).

$$\varepsilon = \varepsilon_F - \Delta\tau$$

where $\Delta\tau$ is the advance required to counter the LO line length increase:

$$\Delta\tau = \frac{\Delta\phi_{160}}{(2.2\pi.160.10^6)}$$

c. The tracking requirements of the array add a further delay (τ) to the sample stream.

At the antenna we use the 5 second counter (the integration clock) to establish the start of the data stream (ie. establish the origin of time); at the central site we specify to the correlator FIFO the number of samples to discard in order that the correlated signals be wavefront-aligned.

The algorithm:

1. Calculate the raw delay: τ_0. This contains the geometric and instrumental delays.

2. Add the FIFO offset T. (cf, AT/23.4.1/012, appendix 3).

3. Add the fixed and LO delays: (ε)

4. Convert the total delay to 128 MHz samples:

$$M_{128}\tau_{128} + \delta\tau = \tau_0 + T + \varepsilon$$

5. The FIFO count is given by :

$$n_{FIFO} = M_{128}\left(\frac{4}{\text{bits/sample}}\right)$$

6. The first sample in the data stream (occurring $\delta\tau$ after the 5 second marker) is identified in the following manner:

we arrange for the 5 sec. counter to produce two outputs: the 5 second clock advanced by 1/4 period ($\tau_{128}/4$); and the 5 sec. clock delayed by 1/4 period. (The "early" and "late" start pulses). We use thesee signals to gate the sample train, choosing "early" or "late" on the basis of $\delta\tau$.

Use the "early" pulse as gate when $0 \leq \delta\tau \leq \tau_{128}/2$

Use the "late" pulse as gate when $\tau_{128}/2 \leq \delta\tau \leq \tau_{128}$

Two additional notes.

1. The integration clock is now not as fixed and inexorable as indicated in AT/23.4/013 . The basic 5 second cycle remains; however, it will be possible to

introduce an occasional offset if it is ever the case that we need to have an integration start at a specific instant. At the start of every integration period the sampler sync. counter is pre-loaded with a number such that after 5 seconds the counter will make the transition from all ones to all zeroes. If the basic clock is 128 MHz, we need a 30 bit counter, pre-loaded with 3 166 460 000 (octal) in order to roll-over after 6.4×10^8 counts. We can thus shift in time the synchronising cycle by using a different pre-load value. It may also be possible to maintain a cycle of period other than 5 seconds, but such requests are to be deprecated.

2. The problem of measuring ϵ is much as described in AT/23.4/103. It must be remembered that the quantity measured is the sum of both the instrumental (fixed) and the LO-stabilisation component (variable).

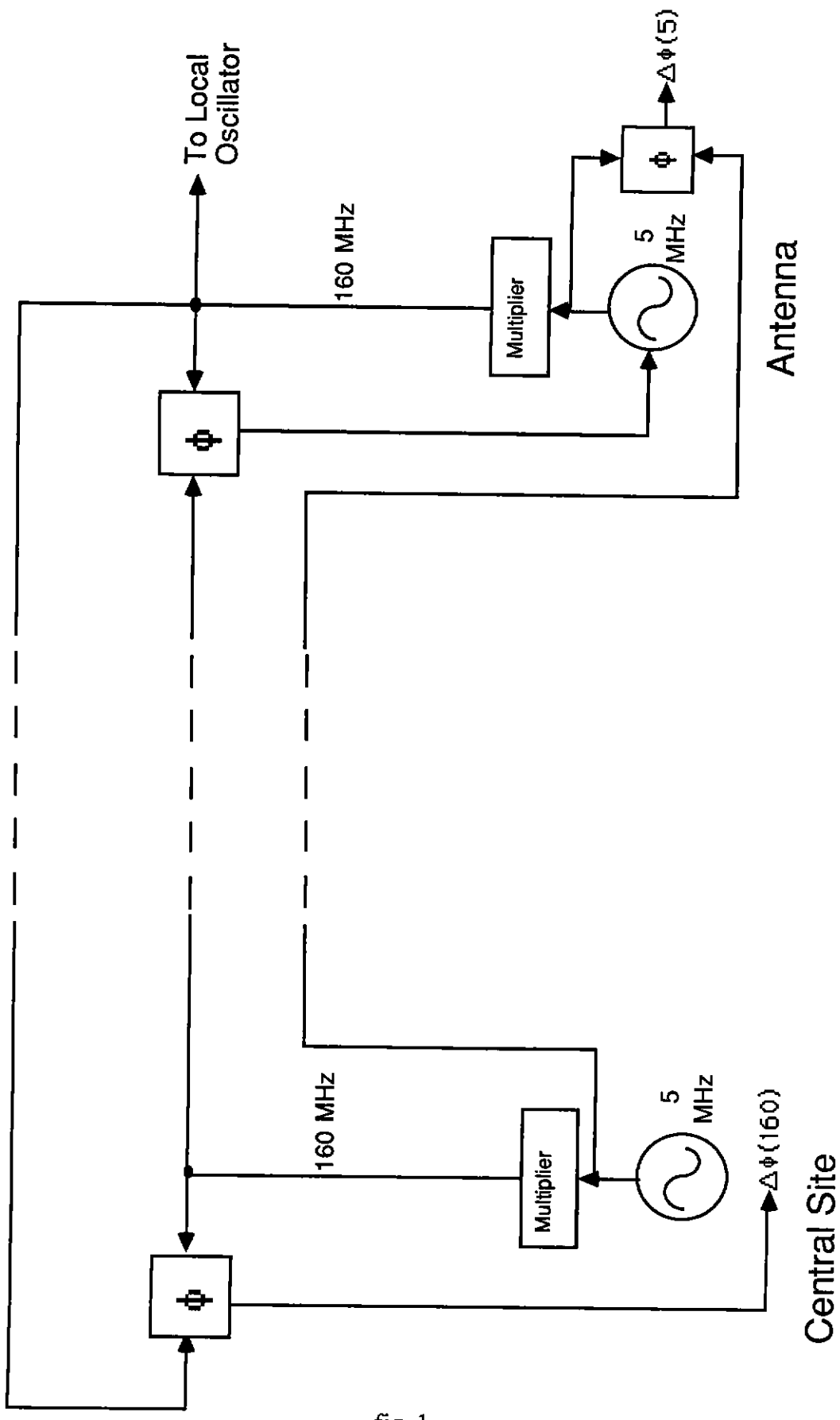
To Local Oscillator
160 MHz
Multiplier
5 MHz
Δφ(5)
Antenna
160 MHz
Multiplier
5 MHz
Δφ(160)
Central Site

fig. 1