AT File

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THE AUSTRALIA TELESCOPE NATIONAL FACILITY

PHASE JUMPS IN THE AT PHASE ROTATOR MODULES

Andrew Bish

INTRODUCTION

In the Australia Telescope (AT), as in all synthesis radio telescopes using interferometer pairs, the rotation of the earth means that the arrival time of a wave front to a particular antenna will vary with respect to any other antenna. To counter this effect, a technique of 'phase rotation' is generally used which removes the resulting variations in phase. At the Australia Telescope, phase rotation is implemented with a digital logic circuit that uses a clocked counter system to rotate the local oscillator and the sampler clock phases.

Currently in the AT a problem exists whereby the phases of incoming signals do not always have the proper phase/delay corrections applied, the result of this being that the correlated output signal often has a noticeable spike in its phase. This is observable either directly when pointing at a strong source such as a calibrator, or indirectly through the cross products of the 'A' & 'B' polarizations.

THE ORIGIN OF THE PHASE ERRORS

The problem discussed here was first noticed because of a very definite spike of 17^{o} between the 'AB' or 'CD' cross products of a receiver. However, further investigations showed a common phase spike at 11.5^{o}, as well as a very large (but not so common) one at around 180^{o}. There were also noticeable jumps of around 3^{o} and 5^{o} with many at a lower level (see figure 1 below). From figure 1, it appears that a phase error of greater than 2^{o} occurs on average once in eight integration cycles over the entire array. There are also a large number of phase errors of a lower level.

It was suggested by Gerry McCulloch that the 17^{o} phase jumps were caused by the phase rotator modules (i.e., the 'L21' & 'L22' modules). To investigate this, an existing control program was modified to drive the modules and load them with a start phase, cycling from 0^{o} - 360^{o}, in increments of 0.18^{o}. Now, in order

Now, in order to facilitate testing, the phase rotator modules have built in phase reference and phase comparator circuits to give relative phases, which are returned by the module (see figure 2). The program simply stored the returned phase if it was in error by a predetermined amount.

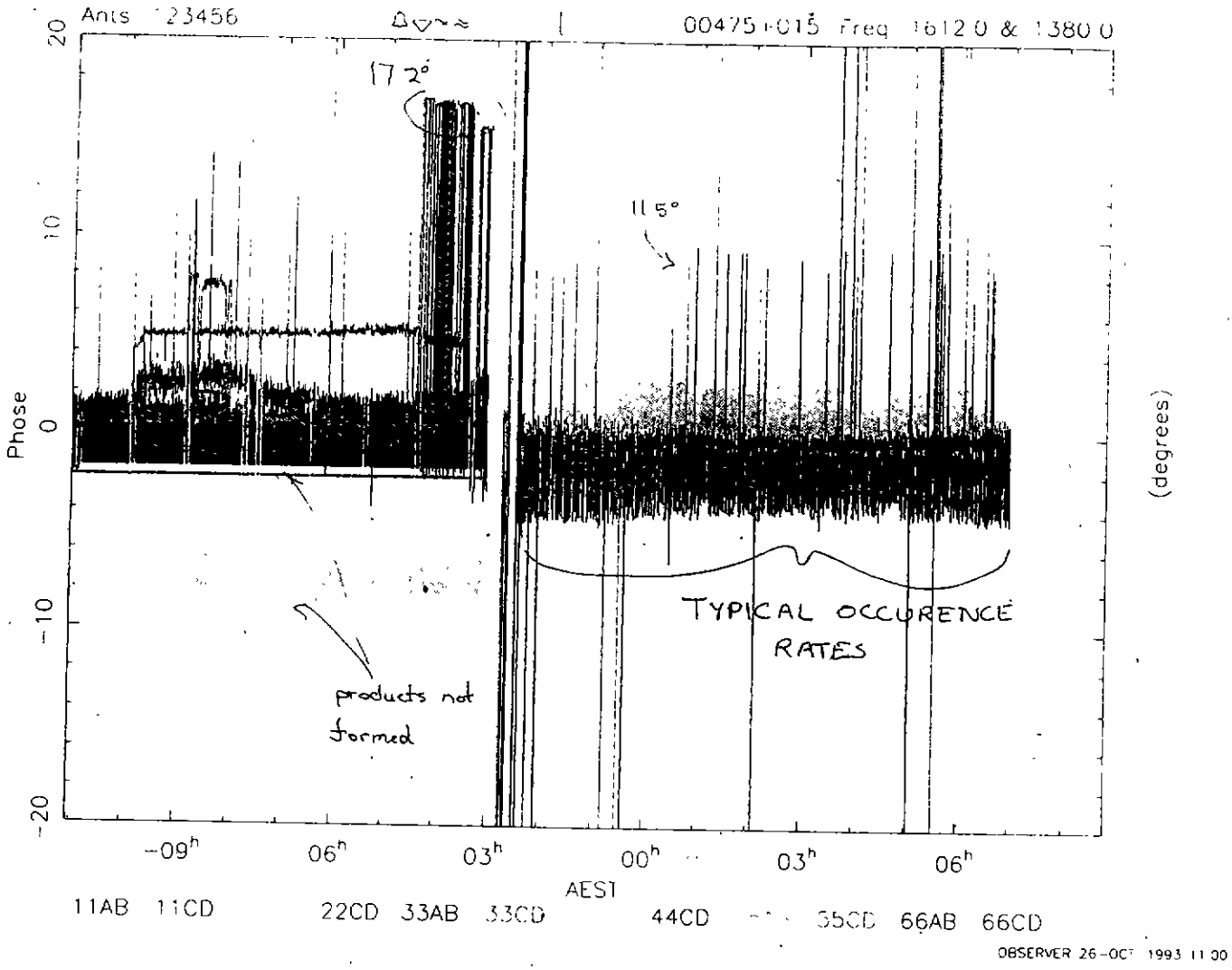

Figure 1 : Errors in start phases caused by the L21/L22 Modules

Nearly all the 'spikes here result from incorrect start phases, however those in the region extending from -11h to -3hr include some artifacts resulting from the correlator not forming the 'AB' products In the 'typical' region, there appears to be quite are large number of low level phase jumps (of the order of 1-2 degrees), as well as one of > 5 degrees every 6 minutes

After recording several of these 360^{0} loops, the errors were analyzed, and it was noted that an 11.5^{0} phase error occurred quite regularly. This error corresponded to a particular combination of bits, namely the lowest 6 bits being

set (111111). Some analysis eventually showed that this resulted when the first clock pulse at the start of an integration cycle did not properly clock a series of three 4-bit counters (74ALS168's). That is, the most significant counter (counter 'C' in figure 2 below) was not clocked whilst A & B were.

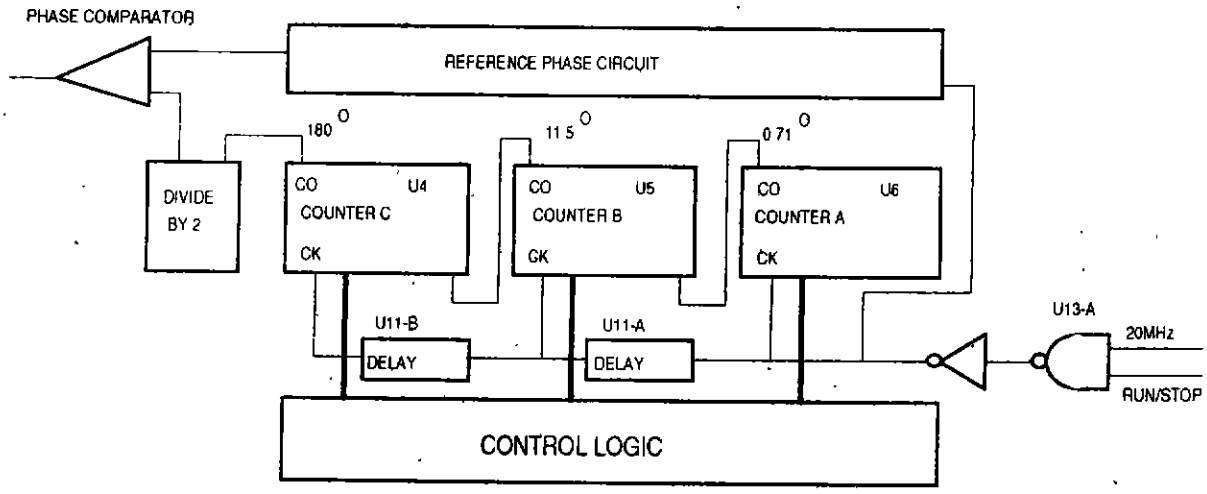

Figure 2: Divide by 2000 loop in L21/L22 Modules

A noticeable error occurs when a counter is fully loaded and receives a clock pulse which triggers it but not the next (more significant) counter This means all the previous counts are lost when CO (the carry look ahead) goes low The angles shown are those that result in a carry-look-ahead being set for the next counter

This meant that when the carry-look-ahead of the second counter was set, then reset by the clock, this pulse would not clock into the most significant counter (C). This resulted in 64 counts being dropped, or that the start phase was incorrect by 64 x 0.18^{o}=11.5^{o}.Further investigation showed that this was because the 20MHz signal that clocked the counters was asynchronously NANDED with the event generator line. Hence at the beginning of an integration cycle the initial clock pulse could be very narrow (a glitch) which caused incorrect clocking of the rest of the circuit (see figure 3 below).

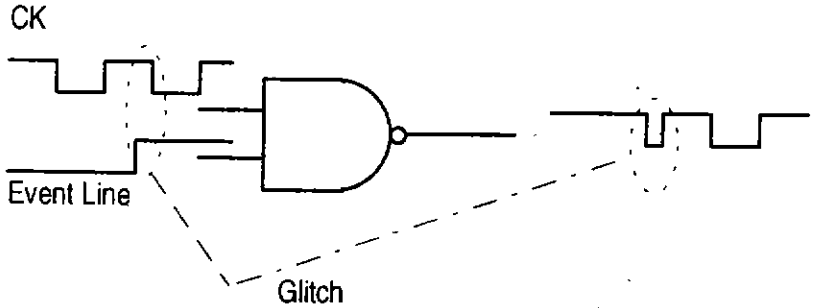

Figure 3: Asynchronous NAND Gate showing Glitch

The reason for such a glitch causing an error is because the clocking rates of the counters, and the operating speeds of the delay circuits are violated, causing

them to be unstable. The result of this is that some of the counters may be clocked while others aren't. This caused a number of detectable errors: a test run of 10 loops of all start phases (20,000 tests all up) for a 'L21' phase rotator module gave the following set of errors:

Error(^{o})	0.71^o	1.41^o	2.82^o	5.72^o	8.6^o	11.5^o	~180^o
Occurrences:	272	6	3	1	1	11	1

Table 1: Phase Errors

Here, the 0.71^o,11.5^o & 180^o errors result from a carry look-ahead pulse being missed (0.71^o ≅ 4x0.18^o, 11.5^o = 64x0.18^o ; 180 ≅ 1024x0.18). The other errors appear to result from errors in the operation of internal divider flip flops (1.4^o ≅ 8 x 0.18^o , 2.82^o ≅16x0.18^o, 5.7≅ 32x0.18^o). Note that the approximate nature of the above values results from an uncertainty of at least 0.09^o in the measured phase. This is the limit of the analog phase meter used to return the difference between the set phase and a reference phase (as indicated in figure 2).

In the case of the L22 modules, these phases are transferred directly to the UHF local oscillator, and thus occur on the final output with the same phases as described above. In the 'L21' modules (which are used to phase rotate the sampler clocks) a start phase error means that the sampler clock will be delayed by:

$$\Delta t = \frac{\text{start phase}}{360^o} \times \text{sample interval} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Since the delay corresponds to the phase versus frequency slope across the signal bandwidth, any initial delay error will result in a total phase change of:

$$\phi(f) = f \times \Delta t \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

The phase errors mentioned above occur at an operational frequency of 128MHz. In the case of the typically used 128MHz bandwidth, the sample rate is twice this (256MHz) corresponding to double the 128MHz start phase error. For example an 11.5^o phase error at 128MHz becomes a 23^o phase error at 256MHz. This means that at a sample rate of 256MHz (a sample interval of 3.9ns) an 11.5^o glitch in the start phase of an 'L21' module will cause a sampling delay of:

$$\Delta t = \frac{23^o}{360^o} \times 3.9ns \qquad \text{.....(3)}$$
$$= 0.25ns$$

For the 128MHz bandwidth, which extends from 128-256MHz, the phase error varies from 11.5^0 to 23^0 (from (2)). The average phase change is that at the center of the band (192MHz), i.e. 17.3^0, as shown in the diagram below:

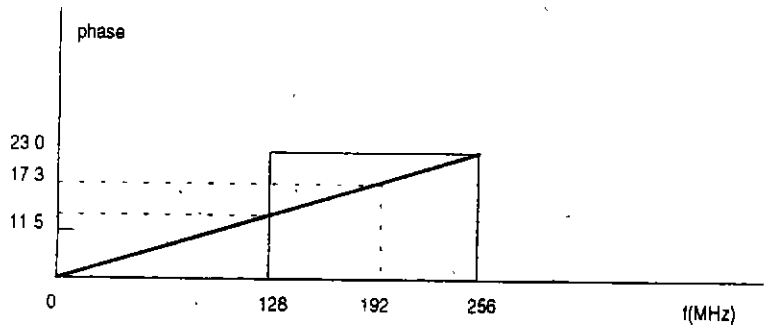

Figure 4: Phase vs. Frequency Relationship
The average phase for the 128-256MHz bandwidth is 17.3 degrees.

To demonstrate this, in figure 5 all the 17^0 glitches correspond to a correlator delay glitch of 0.25ns as predicted by (3). The 11.5^0 glitches do not have any corresponding change of delay, since a wrong start phase on the UHF oscillator only causes a correlator phase error.

The effect on the correlated phase of the errors displayed in Table 1 as applied to an L21 module will be a translation by a factor of:

$$\frac{\varphi_{L21}}{\varphi_{L22}} = \frac{\text{Sample Rate}}{128\text{MHz}} \times \frac{f_{AVERAGE}}{f_{MAX}} \qquad \text{.....(8)}$$

$$= 1.5 \text{ (256MHz sampling at a bandwidth from 128 - 256MHz)}$$

Error(^{0}) - L22	0.71^0	1.41^0	2.82^0	5.72^0	8.6^0	11.5^0	~180^0
Error(^{0}) - L21	1.07^0	2.11^0	4.23^0	8.58^0	12.9^0	17.3^0	270^0

Table 2: Equivalent Resulting Phase Errors in L21/L22 Modules
The correlator phase error resulting from an L21 module is one and
A half times that for an L22 module.

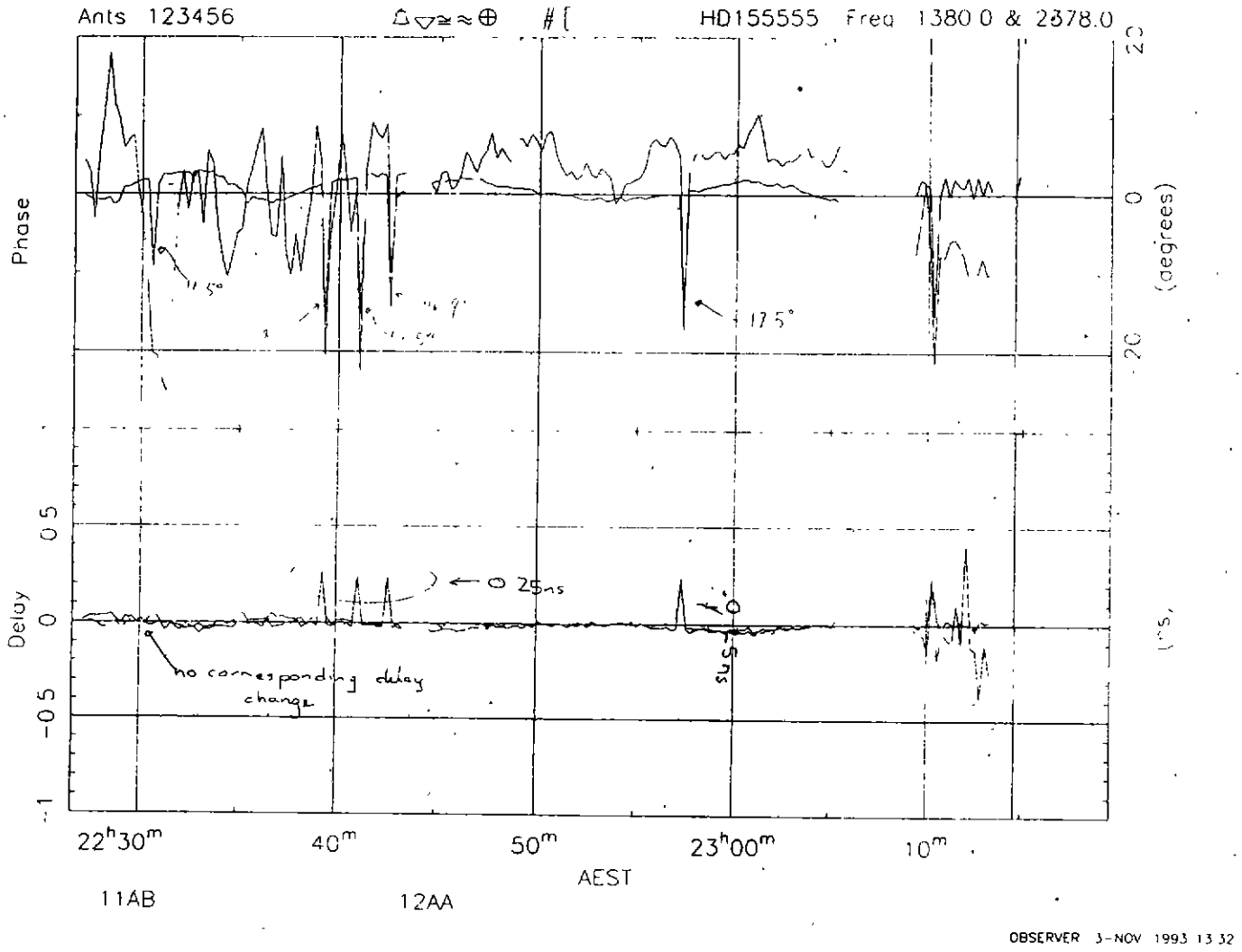

Figure 5:Delay corresponding to 17 degree jump.

OVERALL SYSTEM EFFECTS

With the knowledge of the cause of the 17^{O} phase glitches (amongst others), some estimation as to their effects and occurrence rates can be made.

Given that a glitch in the clock will definitely occur when the event (R/S) line rises in the last 5ns of a 20MHz clock cycle, the probability of a glitch occurring will be:

$$P_{\varphi ERROR} = \frac{5ns}{50ns} \qquad \text{.....(9)}$$
$$= 10\%$$

There are 64 L21/L22 modules in the array this means that on average, six will give an incorrect start phase for each new integration cycle. Of course, most of these errors will be quite small (less than 1^{o}) and will have no measurable effect. From table 1 above, an error of 0.71^{o} or greater will occur approximately 1.5% of the time (i.e. on average one error of greater than 0.7^{o} will occur for every integration cycle). This assumes that the start phases are approximately random over a larger period of time, but the event line (R/S) and the 20MHz clock are derived from the same source. This means that the gradual variations in the relative delays between these two signals will cause them to gradually move with respect to each other. Thus at times the problem doesn't demonstrate itself at all, whilst at other times it occurs regularly.

The main effect of these errors on the overall astronomy is an increase in the effective sidelobes of the synthesized beam resulting in a corresponding loss of dynamic range and an effective smearing of the image. This would be most noticeable when imaging an area containing both strong and weak sources.

Another potential problem has to do with the second derivative section of the phase rotator module. This section is driven by the same clock circuit that caused the start phase errors, and has the same configuration and counter IC's as the start phase section (except that it has twice as many). Given that the second derivative stage changes the phase rate, this section has potential to cause large errors, particularly for the case of sensitive VLBI measurements where it is to be used. However, this facility is not currently used and only will be if high fringe rates are required in VLBI work.

FINAL SOLUTION – A HARDWARE MODIFICATION

The problem discussed above results from the logic being asynchronous, and can be fixed by making the system synchronous. The suggested solution is to use a pair of clocked D-type flip-flop to synchronize the run/stop with the 20MHz (see figure 6 below). This removes the glitching problem of the NAND gate in figure 2, but metastability will now occur when the run/stop signal violates the setup & hold times of the first D type flip flop. However with a system of D type flip flops as shown here this metastability will have to last for a clock cycle (minus the various delay times of the flip-flops) before it will effect the output of the NAND gate on the rising edge of the next clock cycle (figure 3). This reduces the problem of metastability to negligible amounts. Implementing this solution on the L21 module tested above removed the problem entirely (i.e., there no start phase errors after implementing this solution).

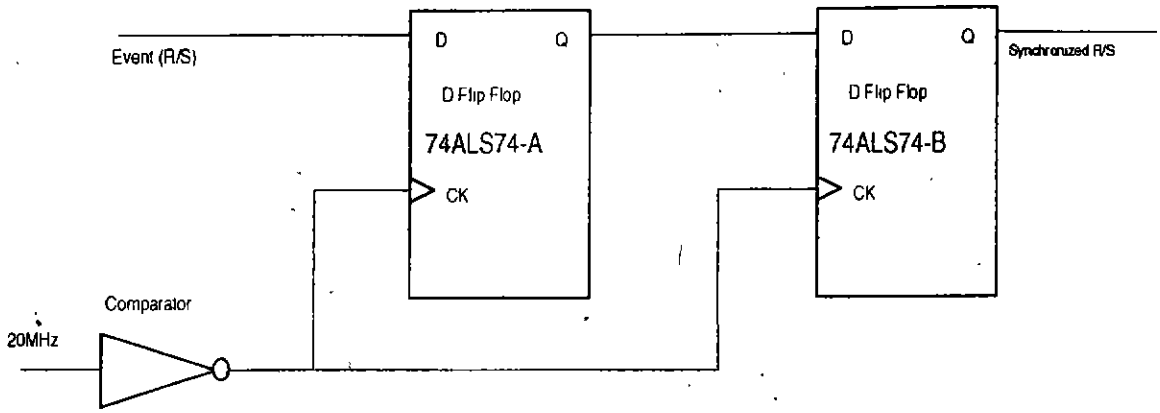

Figure 6: Synchronizing Circuit for the Event (R/S) Line

A calculation of the Mean Time Between Failure (MTBF) for this solution [ref. ALS/AS Logic Data Book, Texas Instruments,1986], gives:

$$MTBF_{MODULE} \approx 1900\,years$$

With 64 modules on the array this becomes:

$$\text{MTBF}_{\text{ARRAY}} \approx 1900\,years \div 64$$

$$\approx 30 \text{ years} \qquad \text{.....(10)}$$

Note that the original specifications were for FAST logic devices (i.e., 74F74's), which would have increased the MTBF to a level that would require only one flip-flop to ensure glitching would not occur. However it was difficult to source these components in the given time frame.

Implementing this solution will require mounting the flip flop IC onto the interface board with a small surface mount PCB incorporated into the L21/22 modules. This will involve cutting the R/S track on the interface board, and soldering several wires to various IC's and resistors. The schematic for this modification is shown in the appendix. The implementation cost for this modification will be approximately $200, and it is anticipated that the time required to do this will be 2-3 man weeks.

The only resulting effect on the system by using this technique is that the entire array will now start each integration cycle 75-100ns later than without this fix. This will not cause any obvious problems as the delay is uniformly applied across the array. Particularly since there are already existing undefined delays that occur in the L21/L22 modules. Even so, before implementing this as a final solution it will be necessary to test out the repair on at least one A-B pair on an antenna.

OTHER SOLUTIONS INVESTIGATED

Initially it was thought that by ensuring the software did not demand a start phase that would result in the 11.5^{0} error, the problem would be effectively removed. However, because of the many more low level errors, and the threat to the proper operation of the system, most parties involved decided against this approach.

An alternative solution investigated was to synchronize the event line (run/stop) by bringing it into a L31 module and clocking it there, before distributing it to the L21/L22 modules. However, according to Gerry McCulloch, this would only partly solve the problem as there is no definite phase relationship between the L31 and L21/L22 modules.

CONCLUSION

From an engineering perspective these phase jumps are quite noticeable and require attention. However from an astronomical perspective (for current uses at least), their effect is rather ambiguous. The main problem appears to be in the loss of dynamic range of the system. From the probabilities of these phase errors occurring, it appears that the dynamic range of the array would be degraded.

If the array is used as a tied array for VLBI, the problem may be more significant, this is especially so if the '2nd derivative' feature of the phase rotators was used. The problem may also have greater effect on observations involving polarization measurements.

For continuing operation these phase errors could be ignored (or corrected with software) with little effect on the Astronomy at the AT. However, in the interests of future operation of the AT a decision has been made to correct the problem properly with a hardware solution.

ACKNOWLEDGEMENTS

Considerable help in the analysis and solution to this problem was given by Russell Gough, who provided guidance and ideas too numerous to mention. Also, the help of Gerry McCulloch is acknowledged, as is almost everybody else in the Electronics Group at Narrabri.

APPENDIX -- SCHEMATIC FOR HARDWARE MODIFICATION