The Sampler Synchronising Cycle - our understanding as of 25 September 1986.

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- 1. The samplers at the antenna will be hardware locked to a 5 (five) second cycle derived from the line stabilised LO.
- 2. The sampler synchronising pulse sent to to the correlator will be locked to this cycle.
- 3. The basic data taking cycle is locked to this cycle. Integration periods equal to 5m seconds (m integer) will be allowed, with the intermediate 5 second synchronising pulses omitted.
- 4. Sub-cycles (<5seconds) are also allowed, provided that the delay requirements do not change from one sub-cycle to the next. That is, since no resynchronising will occur, we must have continuity in the sampler phase and phase rate.
- 5. The hardware (LO) clock is reset from time to time. The hope is that it is no more frequent than once per array reconfiguration.
- 6. Once set, the cycle is defined. Thereafter, the data taking has no freedom in choosing start times - they MUST operate on a predetermined 5 second (BAT) cycle.
- 7. (Unhappily, while it is technically possible to synchronize 6 antenna clocks from one central clock, the converse is not).
- 8. Consequences for the computing.
- a. The observing task must choose the start times for all integrations to fit the cycle; on the hour, and every five seconds thereafter are the only allowed times. Note that this is BAT. The vax. unhappily, will be UTC.

Synchronization of the AT operations mik 23 July 1986

A series of timing pulses are required to synchronize the activities of the local oscillators, samplers, noise sources, phase switches and the correlator. Figure 1 shows schematically the relationship of the various pulses.

1 At the antenna

1.1 Before an integration can start the local oscillator fringe rotator and the sampler delay tracker need to be loaded with the initial phase, phase rate and its second derivative. This happens in the 10-20 msec blanking period before the start of the integration interval.

A START pulse triggers three events:

The LO starts fringe rotating;

The sampler oscillator starts delay tracking:

The sampler itself is armed, and then it issues the SYNC pulse at the appropriately accurate (1/256 μ sec) instant: it then starts sampling.

The intention is that the START be synchronous over the entire array. Thus, if the expected start time is $T_{\rm start}$, then the event trigger will be requested for a pulse at

 $^{\mathrm{T}}$ start $^{-}$ $^{\mathrm{t}}$ trans. Where $^{\mathrm{t}}$ trans is the transmission time from the central site to the antenna.

The LO and samplers will be stopped $t_{
m blank}$ (~ 10 msecs) before the start of the next integration interval.

1.2 The switching waveforms (noise source and phase switches) need to be triggered in advance of $T_{\rm start}$ in order to ensure that the waveforms from different antennas are in phase <u>after</u> the delay lines. Thus we will request that the waveforms start at:

Tstart - tdelay - ttrans

where $t_{\mbox{delay}}$ is the delay that will be inserted at the correlator delay lines.

A STOP pulse will also be required. ($T_{stop} - t_{delay} - t_{trans}$)

2. At the central site

2.1 The correlator needs a START pulse to arm it in preparation for the arrival of the SYNC pulse. We ask for a pulse at $^{\rm T}_{\rm start}$

The correlator expects to be told the length of the

integration interval:

This should be expressed as a cycle count:

$$N = (T_{stop} - T_{start}) 16E6$$

2.2 The demodulators (phase and amplitude) need a start and stop pulse: at $T_{\mbox{start}}$ and $T_{\mbox{stop}}$.

3 Activity during the 20 msec blanking period

Communication from the Antenna Control Computer to the outside world via a dataset is not rapid - of order 2 msecs/transaction (assuming 38.4 Kbaud transmission rate). Therefore, only a limited amount of information can be transmitted during the blanking period. Clearly, wherever possible control settings should be prepared ahead of time: the equipment should be armed, so that when the timing pulse arrives, the change can be made with no further reference to the ACC required.

file : [mjk.time]synchro.rno

