

Design and Testing of a 3 Octave GaAs MMIC LNA

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Overview

A 1-7 GHz MMIC LNA was made with a view to gaining experience in broadband, integrated LNA design for SKA applications. It was manufactured in TRW's 0.15 μm GaAs Power HEMT process and tested on wafer at CSIRO. The first stage oscillates at 41 GHz, consistent with an odd mode in the input transistor pair. This oscillation renders the circuit unusable. However, the performance of the second and third stages matches simulation well. Finally, a stabilisation network is suggested along with other possible follow up work.

Design

Design Philosophy

Specifications for SKA LNAs are still loose. For the Luneburg Lens approach we nominally desire an uncooled LNA with $T_e \sim 25\text{K}$ over a 0-10 GHz range and sufficient gain to dampen the noise contributions of prior system elements [1]. A robust integrated approach (i.e. MMIC design) is also desired such that mass production of circuits with uniform behaviour will be possible.

Bands covering up to 2 GHz are likely to be well serviced by improvements in commercially available transistors and MMICs. SiGe in particular shows good prospects for covering this band without the need of lossy matching components. Its noise performance should track transistor improvements well whether it be applied in a discrete or an integrated approach [2].

The goal of this design is to cover a higher portion of the relevant band, from 1 GHz to 8 GHz, with a single GaAs MMIC LNA. Lower frequencies are not attempted, partially due to the above reasoning and also due to the fact that they require larger passive matching components with low losses. Apart from using up expensive MMIC real-estate, such components are not readily manufacturable in present commercial processes.

An earlier circuit covering a similar band was designed in the same process at CSIRO. Its name is CSIR6_LBHGLNA_01A and it consists of two eight finger, 400 μm periphery HEMT stages. It covers 2-8 GHz with over 20 dB gain; has both S_{11} and S_{22} lower than -13dB; and a noise figure better than 3.5 dB. The design presented in this report attempts to achieve a higher gain, a lower noise figure, and a broader bandwidth.

Design Methodology

The performance characteristics of CSIR6_LBHGLNA_01A were taken as a starting point as it covers an SKA relevant band and was manufactured in the same process employed here. The TRW 0.15 μm GaAs Power HEMT process was selected for this work due to the fact that there was space available on an existing CSIRO run. This process is suitable as an uncooled GaAs LNA's noise figure in the band of interest will be limited by ohmic losses in the input matching network. Using TRW's low noise process would yield a better noise figure for the individual transistors involved, but the overall circuit's noise performance would not be significantly improved.

A large periphery device was chosen as they make for an easier simultaneous noise and power match in a 50 Ω system [3]. Although, there is the drawback of their increased power consumption. The 400 μm HEMT was chosen in particular as it is the largest periphery device with a standard linear model in the intended process.

From here a linear model for an eight finger, 400 μm HEMT was imported to MMICAD for some explorative simulation. Passive components were assumed to be perfect and the effects of biasing networks were not considered. The following baseline specification was based on the knowledge gained from these idealised simulations.

Bandwidth	3 Octaves at 3dB points (nominally 1-8 GHz)
Gain	> 25dB with < 2dB ripple peak to peak
NF	< 1.5 dB (120K) in band (3 octaves)
S₁₁	< -10dB in band
S₂₂	< -10dB in band

Table 1. Initial specifications for the design.

General Characteristics of the Final Design

The layout of the final design is shown in Fig. 1. Three gain stages were required to achieve the specified gain. Both the input and output are matched to 50 Ω using simple discrete L-networks. Distributed transmission line inductors are used for both source degeneration and high frequency choking in the bias lines.

The first gain stage consists of two 400 μm HEMTs in parallel yielding an 800 μm HEMT equivalent. This eases the conflicting requirements of noise and power matching at the input. It allows a relatively smaller series input inductor than would be required for matching to a single 400 μm HEMT. This stage could be replaced by a single HEMT of optimum periphery. The reason for not doing this was a desire to stick to standard models.

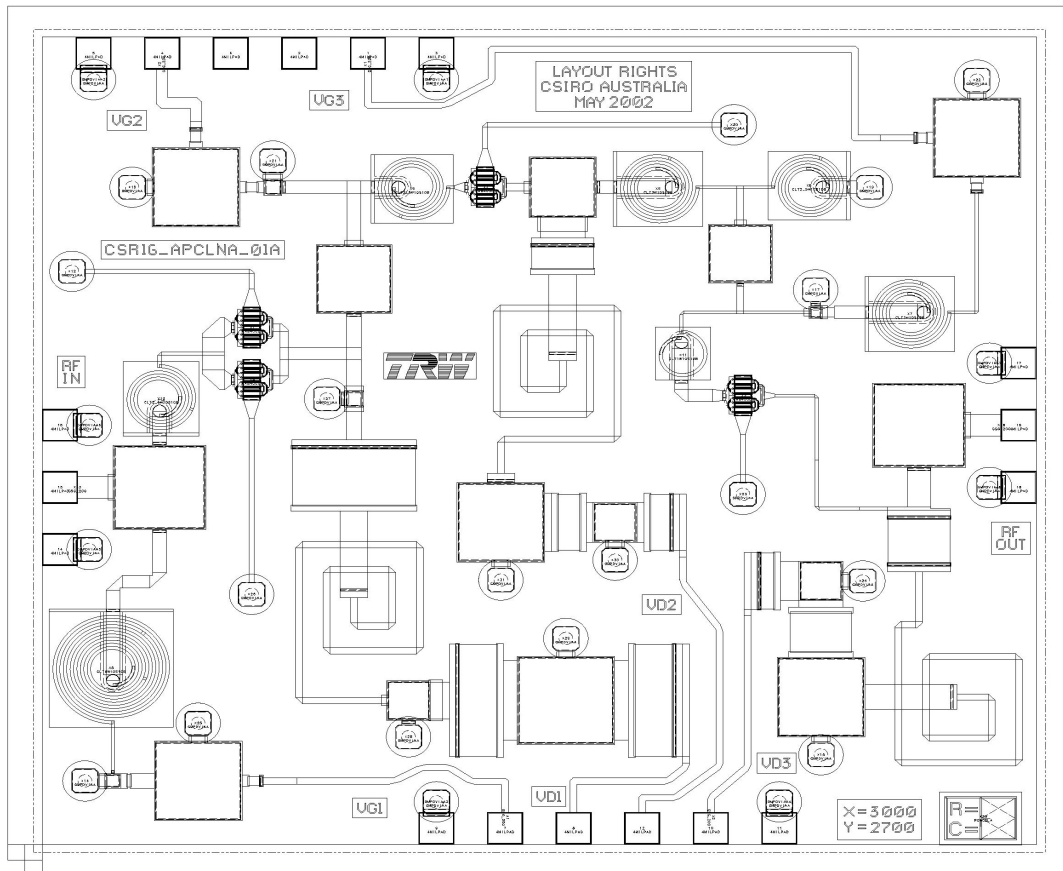


Fig 1. Final design layout.

It was intended to provide a solution that requires minimal off-chip circuitry. All biasing and matching is performed within the MMIC. A gain equalisation network is included between the second and third gain stages. Although, after global optimisation, its function is somewhat aided by the various DC biasing, blocking and bypassing components. Although this approach makes for a rather "busy" layout, care was taken to keep at least 100 μm (one substrate thickness) separation between components whose coupling is not modelled.

The final circuit evolved out of a continuous iteration between optimisation and constraint through manual layout. Table 2 on the following page summarises the expected performance of the final design as simulated in LIBRA. Comparison with the original targets in Table 1 shows that they are met over the majority of the passband.

Bandwidth	3 octaves at 3dB points (0.9-7.4 GHz)
Gain	28.5 dB with 1.7 dB ripple peak to peak
NF	<1.7 dB (140 K) for 1.5-7.5 GHz (2.3 octaves) <1.5 dB (120 K) for 1.7-7.1 GHz (2 octaves)
S₁₁	< -10dB in band
S₂₂	< -10dB in band except for 9.7-7.7 GHz where it is < -6.5 dB

Table 2. Simulated parameters of the final design.

Simulated S-Parameters of the Final Design

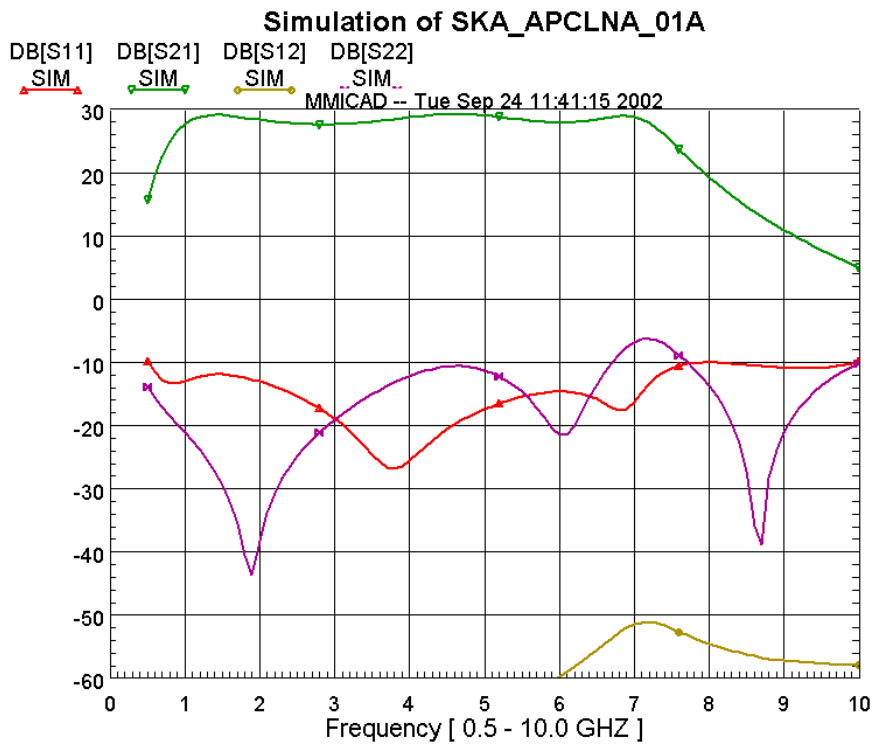


Fig. 2. Simulated S-Parameters for the LNA design

Simulated Noise Figure of the Final Design

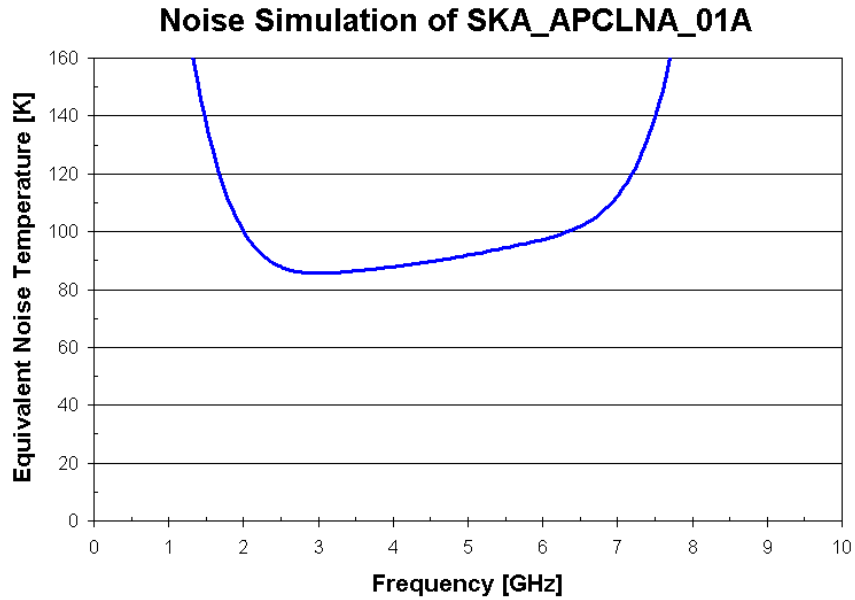


Fig. 3. Simulated equivalent noise temperature.

Nominal Biasing Conditions of the Final Design

Stage	Periphery	$V_D = V_{DS}$	I_{DD}	$V_G = V_{GS}$
1	0.8 mm	2.0 V	90 mA	-0.5 V
2	0.4 mm	2.0 V	45 mA	-0.5 V
3	0.4 mm	2.0 V	45 mA	-0.5 V

Table 3. Nominal biasing conditions for the final design.

Test Results

Micrograph

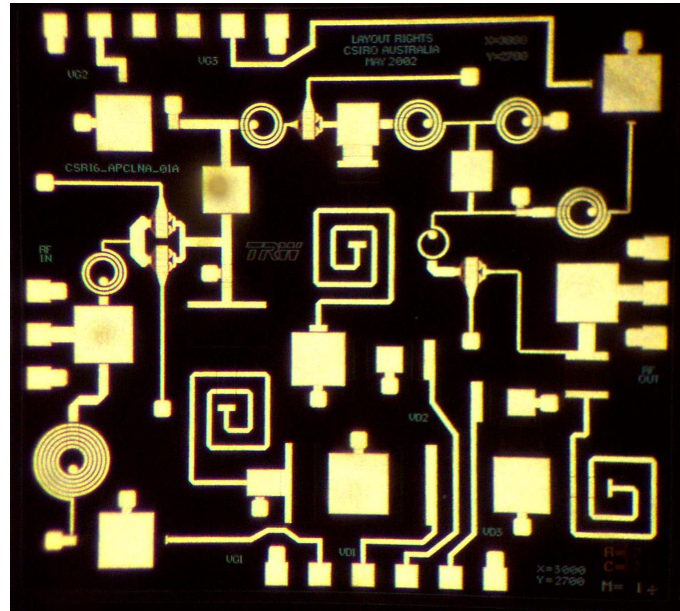


Fig. 4. A micrograph of the circuit. Only the gold top metal can be seen. Distortions are due to the coupling between the camera and the eyepiece of the microscope.

Test Biasing Conditions

The biasing conditions for the initial on wafer tests are given in the following tables.

Stage	Periphery	V_{DD}	I_{DD}	I_D	$I_{D/w}$	R_D	$V_D = V_{DS}$
1	0.8 mm	8.5 V	50 mA	25 mA	62.5 mA/mm	110 Ω	3.0 V
2	0.4 mm	6.6 V	47 mA	47 mA	117.5 mA/mm	102 Ω	1.8 V
3	0.4 mm	6.0 V	24 mA	24 mA	60.0 mA/mm	165 Ω	2.0 V

Table 4. Drain bias parameters for initial testing

Stage	V_{GG}	I_{GG}	I_G	R_G	$V_G = V_{GS}$
1	-0.54 V	+1.96 mA	+0.98 mA	118 Ω	-0.77 V
2	-0.60 V	-0.06 μ A	-0.06 μ A	210 Ω	-0.60 V
3	-0.76 V	-0.10 μ A	-0.10 μ A	143 Ω	-0.76 V

Table 5. Gate bias parameters for initial testing

It can be seen that stage two is almost exactly at its design bias point. Stage three is biased slightly lower on the I_D - V_{DS} curve. The power supply used for its drain could not exceed 6 V whereas 9.4 V is required for the designed bias point. More concerning was the first stage which displayed a gate current in the order of a milliamp. In addition, its bias was not easily controlled. It seemed to have a "preferred" bias point which was difficult to coax it away from without pinching off the transistor or sending the gate current through the roof. To explore this further, gate current was measured as a function of drain voltage. The results are recorded in Fig. 5 below.

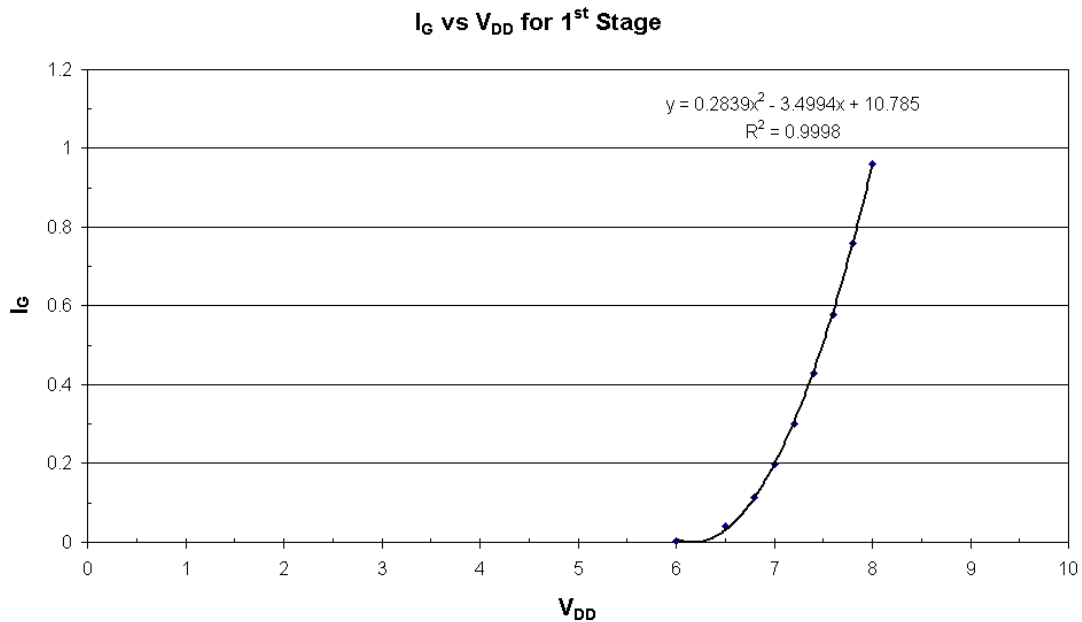


Fig. 5. I_{GG} vs. V_{DD} for the first stage of the LNA. The measured points are joined by the second order polynomial of best fit.

S-Parameters

A network analyser (HP8510) combined with 0-67 GHz probes (Picoprobe 67A-GSG-200-P) were used to measure the S-parameters of several circuits on wafer. A few different instances of the circuit were measured on each of two wafers. The results were repeatable and thus only a single set of S-parameters was initially recorded, namely those for CSIR16_1401_073_SKA_APCKNA_01A_070100. They are plotted below in Fig. 6.

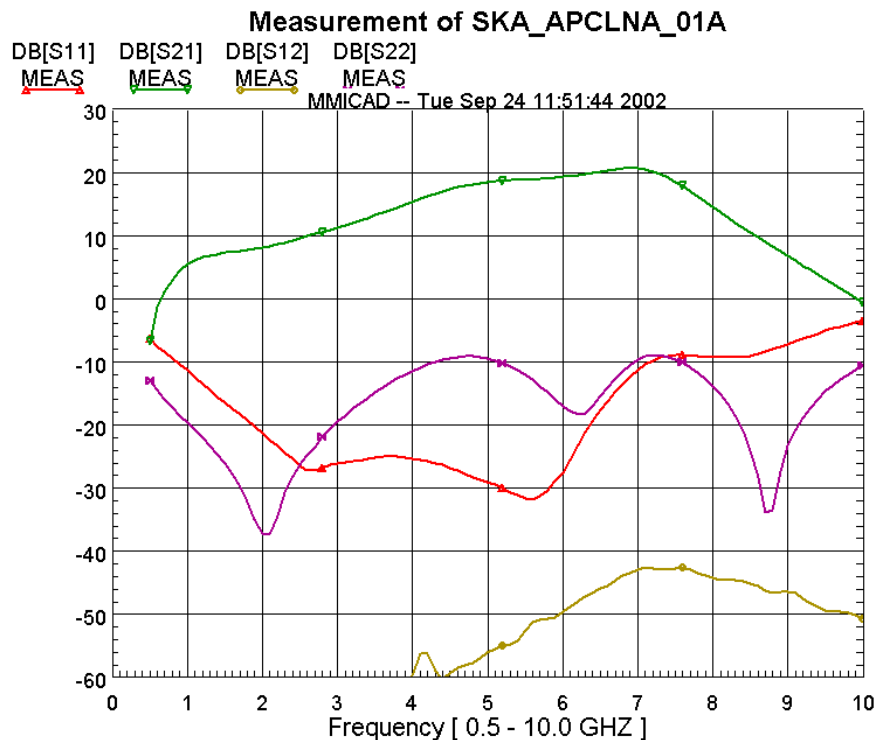


Fig. 6. S-parameters of 1401_073_SKA_APCKNA_01A_070100 as measured on 4 September 2002. The bias conditions for this measurement are given in Tables 4 and 5 for the drain and gate respectively.

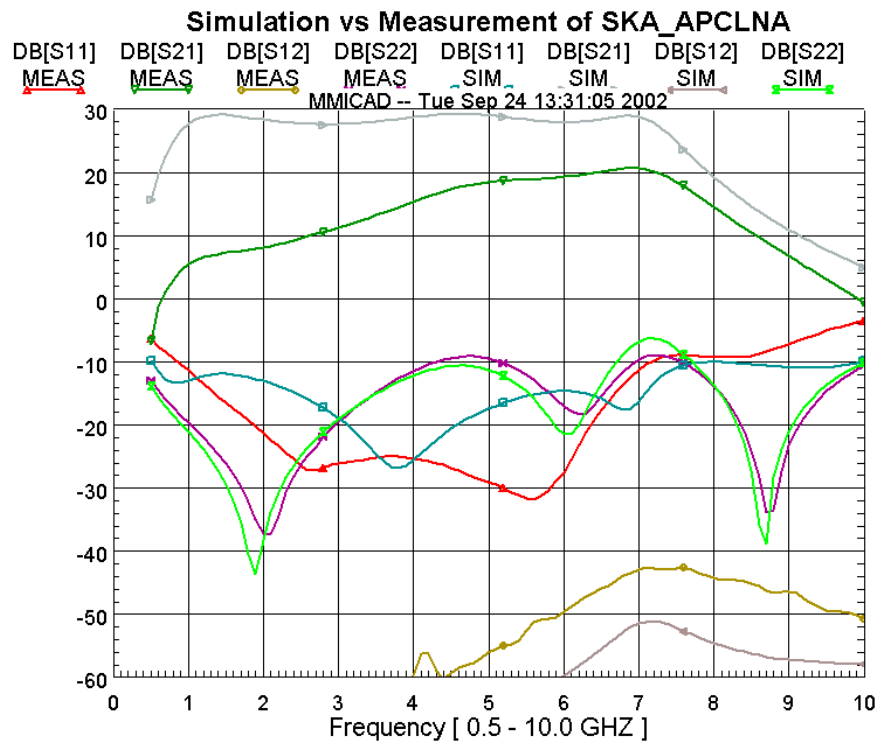


Fig. 7. The simulation of Fig. 2 and the measurement of Fig. 6 plotted on the same axis for comparison.

Some initial observations can be made from the comparison between simulation and measurement in Fig. 7 above. The measured gain shape matches the simulation very well in its break points, ripple structure and final slope. However, the gain is 8.2 dB lower than expected at the top of the band and 22.2 dB lower than expected at the bottom. This may be summarised as a constant 2.5 dB/GHz gain slope across the entire passband.

S_{11} measured better than predicted, remaining below -20 dB over two thirds of the band as opposed to the design goal of -10dB. However, its shape is significantly different to that simulated. It appears to be the most poorly modelled attribute. S_{22} on the other hand matches the simulation exceedingly well.

Finally, S_{12} matches the simulation well in shape, but is nevertheless about 9 dB greater than expected across the band.

Power

In order to test for possible oscillations, a power meter was used to measure the RF power emanating from the circuit's input and output terminals. This test was performed with the alternate terminal both open and terminated in a 50 Ω load. As soon as the first stage is moved out of pinchoff, the output power rose by 3 dB. More strikingly, when the

first stage was turned on, the power level at the input rose tremendously to a level of order 0 dBm. This result points towards an oscillation in the first stage.

Spectrum

Subsequently, a spectrum analyser was used to search for the frequency of the suspected oscillation. An external harmonic mixer in conjunction with the analyser's frequency identification function were used to identify an oscillation mode at 41.2 GHz.

Analysis of Test Results

The on-wafer test results are consistent with an odd mode oscillation in, and consequently no gain from, the first stage. This scenario is discussed here, while a number of other possibilities that were mostly ruled out are discussed in Appendix B.

Odd Mode Oscillation

The anomalous biasing behaviour of the first stage appears to coincide with the 41 GHz oscillation mode in the first stage. Odd mode oscillations are observed in power amplifiers employing parallel transistors in similar topologies to that encountered in this circuit's input stage. Such an oscillation could cause the transistor pair to self-bias in a similar fashion to that observed and would not be predicted by standard $K>1$ & $B>0$ stability constraints.

To investigate this possibility, the unified analysis of MMIC power amplifier stability proposed by Freitag [4] was applied to this circuit. The following notational convention was added to Freitag's analysis for ease of reference.

$$E = z_{ei} + z_{eo}$$

$$O = z_{oi} + z_{oo}$$

Hence, Freitag's conditions for oscillation translate to

$$\begin{aligned} \operatorname{Re}\{E\} < 0; \text{ and} \\ \operatorname{Im}\{E\} = 0 \quad (\text{even mode}) \end{aligned}$$

$$\begin{aligned} \operatorname{Re}\{O\} < 0; \text{ and} \\ \operatorname{Im}\{O\} = 0 \quad (\text{odd mode}) \end{aligned}$$

That is, if these condition's are satisfied at frequency f then the circuit will oscillate at that same frequency. The real and imaginary parts of E and O for the amplifier under study were investigated from 0.5 GHz to 125 GHz. Odd mode oscillations were predicted at both 39 GHz and 122 GHz. No even mode oscillations are predicted as was the case with

the traditional stability analysis at design time. The plots used for this analysis are collated in Appendix A.

The observed oscillation at 41 GHz is sufficiently close to the first predicted odd mode at 39 GHz to build support for this hypothesised source of instability. It should also be noted that the odd mode stability analysis was performed before measuring the oscillation frequency and thus was not biased by its knowledge.

No Gain from the First Stage

The oscillation in the first stage could cause it to have little or no gain, and hence cause the anomalous gain slope observed in the S-parameter measurements. This was explored by replacing each first stage transistor with a short circuit in the relevant LIBRA schematic. The resulting simulated S-parameters are shown in Fig. 8.

The simulated gain for this scenario is much closer to that which is measured. It is almost a perfect match at the low end of the band and is only 4 dB out at the top end. S_{12} is also a better match with it being only 4.8 dB as opposed to 8.8 dB out at its peak. Intuitively, S_{11} is not modelled well by this approach and S_{22} remains the best modelled parameter.

There is thus a reasonable degree of support for the hypothesis that the first stage is yielding little to no gain. This line of thinking alone does not prove that the absence of gain is due to the oscillation, although it is likely.

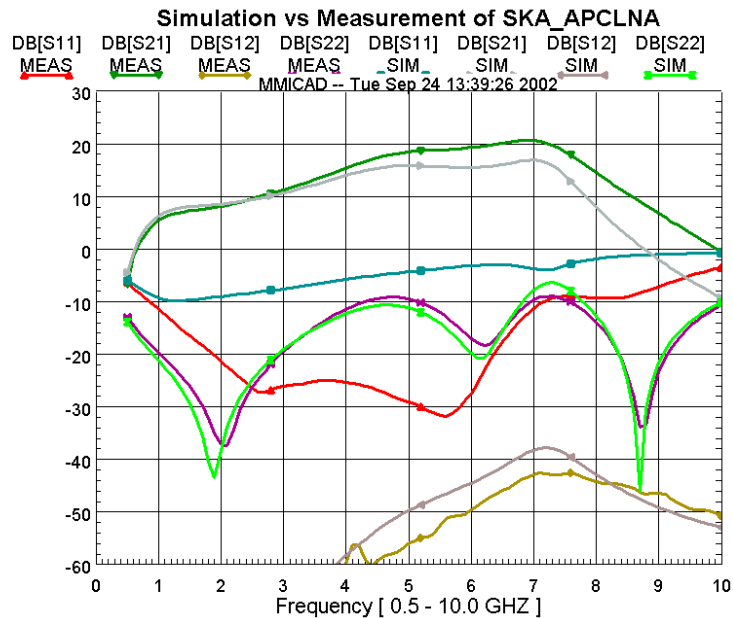


Fig. 8. Measured S-parameters of the circuit and simulated S-parameters for short-circuited transistors in the first stage.

A Possible Stabilising Network

The stabilising network shown in Fig. 9 was explored during the previous odd-mode stability analysis. R_{OP} was found to dampen the 122 GHz odd mode oscillation and R_{OS} was found to dampen the 39 GHz oscillation. For odd mode stability the following restrictions apply to the stabilising network component values

$$R_{OP} < 5 \text{ k}\Omega; \text{ and}$$

$$R_{OS} > 7 \Omega.$$

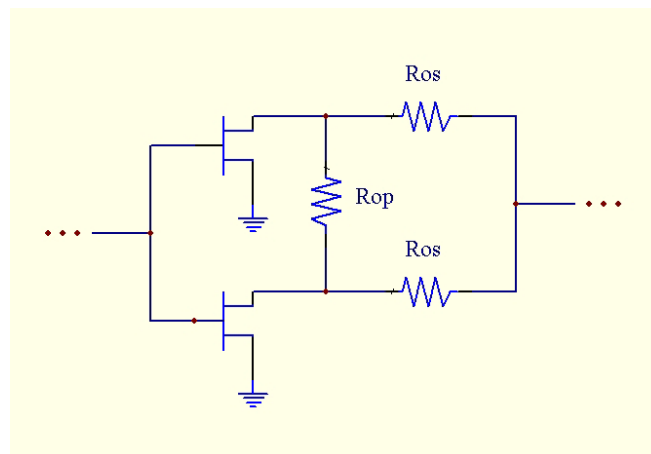


Fig. 9. Possible stabilising network for first stage transistor pair.

Conclusions

Due to the first stage oscillation, the amplifier appears unusable. However, the odd mode oscillation frequency was predicted to within 5%, suggesting that a suitable method of analysing this problem has been found. Further, the close match between the measured S-parameters and those simulated for no first stage gain hint that all is well apart from this oscillation. Thus, the design of the second and third stages of the amplifier along with the interstage gain equalisation network may be deemed successful. The input power and noise matching could not be explored due to the oscillation. However, a stabilising network has been suggested should further iterations of this design be desired.

Future Work

Possible future work includes:

- isolating one of the input transistors and to produce a stable circuit, albeit with poorer input match and noise performance;
- reiterating the existing design with the inclusion of a suitable stabilisation network;
- reiterating the existing design with a single transistor in the first stage; and
- taking the lessons learned to a completely new design.

Acknowledgements

Great thanks are due to Russel Gough (CSIRO ATNF) for his great knowledge of MMIC design and the patience with which he shares it. Peter Hall and Warwick Wilson are also thanked for this excellent opportunity to learn about MMIC design.

References

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4. R.G. Freitag, "A Unified Analysis of MMIC Power Amplifier Stability," *IEEE MTT-S Digest*, 1992.
5. P. Roberts, CSIRO Australia Telescope National Facility, private communication, September 2002.
6. S. Giugni, CSIRO Telecommunications and Industrial Physics, private communication, September 2002.

Appendix A: Even/Odd Mode Stability Plots

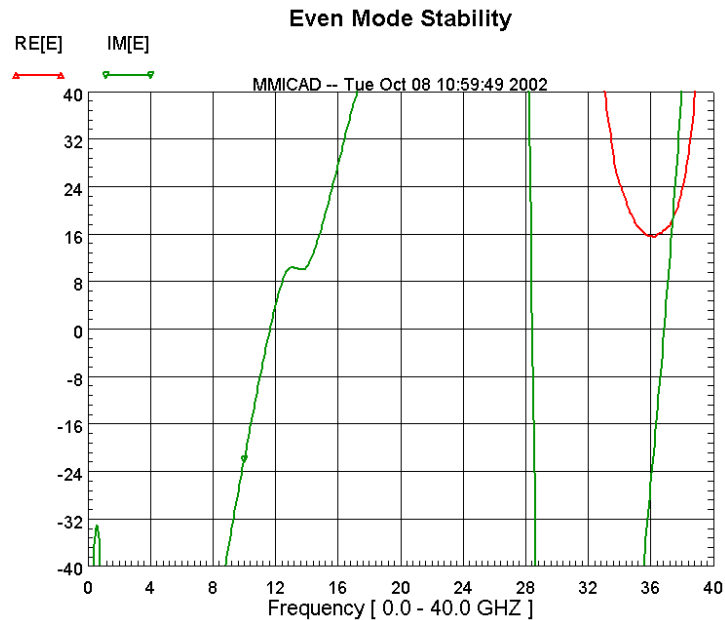


Fig. A1. Even mode stability parameters for the 0-40 GHz model. Here each inductor is modelled using measured S-parameters. No even mode oscillations are predicted.

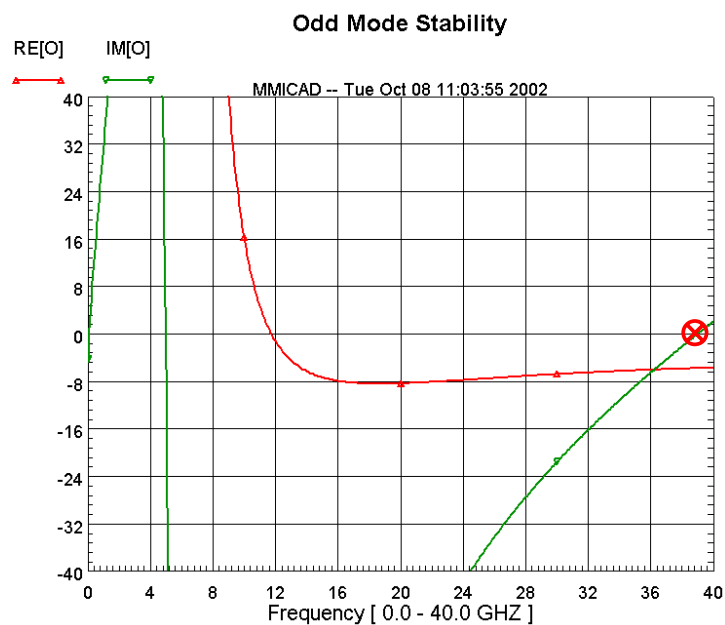


Fig. A2. Odd mode stability parameters for the 0-40 GHz model. Here each inductor is modelled using measured S-parameters. An odd mode oscillation is predicted at 39 GHz as marked.

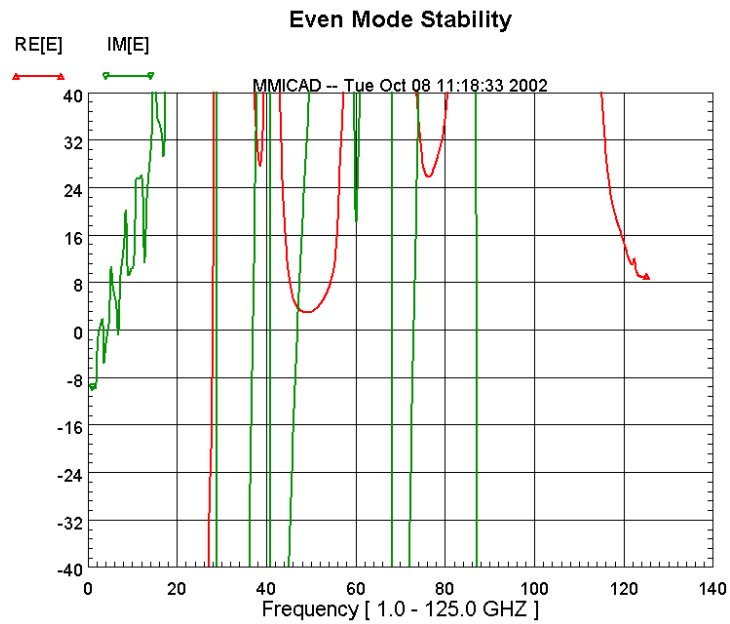


Fig. A3. Even mode stability parameters for the 40-125 GHz model. Here each inductor is modelled by EM simulation, except the shunt input inductor for which an equivalent lumped circuit is used. No even mode oscillations are predicted above 40 GHz. The model is invalid below 40 GHz.

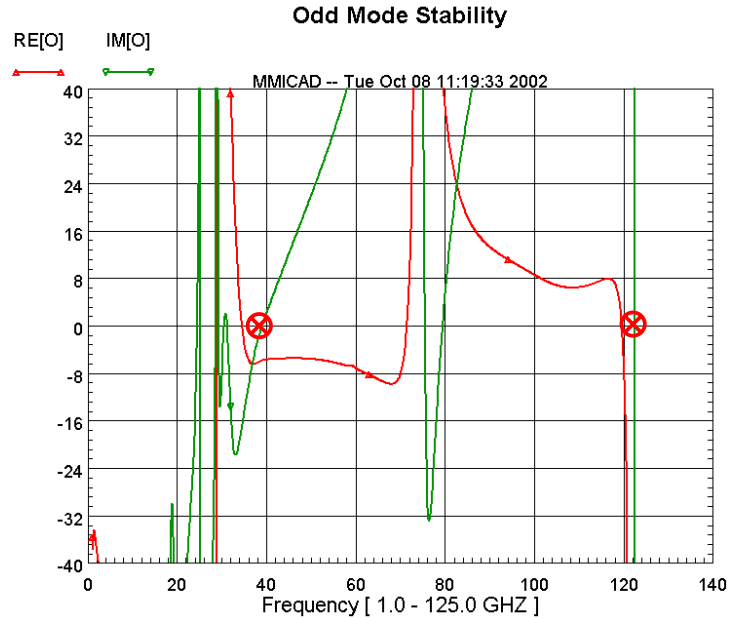


Fig. A4. Odd mode stability parameters for the 40-125 GHz model. Here each inductor is modelled by EM simulation, except the shunt input inductor for which an equivalent lumped circuit is used. Odd mode oscillations are predicted at 39 GHz and 122 GHz. Further oscillations are predicted at lower frequencies, although the model is invalid below 40 GHz.

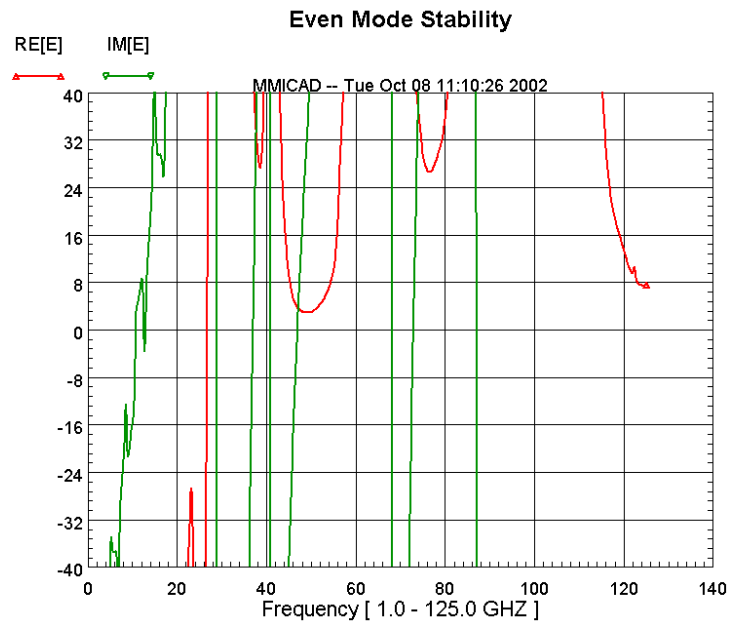


Fig. A5. Even mode stability parameters for the 40-125 GHz model. Here each inductor is modelled by EM simulation, although the shunt input inductor uses parameters simulated for a lower inductance than applied in the real circuit. No even mode oscillations are predicted above 40 GHz. The model is invalid below 40 GHz.

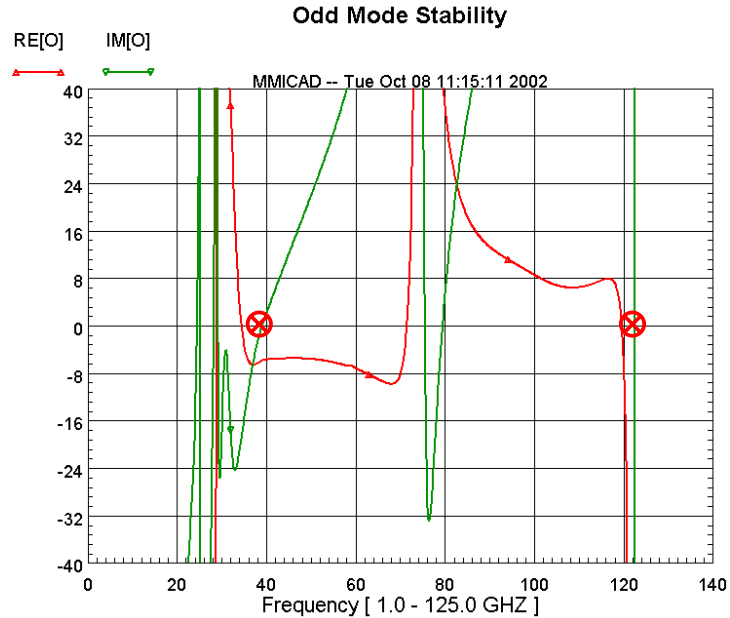


Fig. A6. Odd mode stability parameters for the 40-125 GHz model. Here each inductor is modelled by EM simulation, although the shunt input inductor uses parameters simulated for a lower inductance than used. Odd mode oscillations are predicted at 39 GHz and 122 GHz. Further oscillations are predicted at lower frequencies, although the model is invalid below 40 GHz.

Appendix B: Less Likely Causes of Anomalous Performance

An unaccounted series capacitance

The gain slope looks similar to that which we would expect if there was an unaccounted capacitance in series with the circuit. However, this would not explain the strange biasing conditions in the first stage. It should also affect the final gain slope after the high frequency cut-off of the gain equalisation filter but does not.

Transistors biased differently to the models used for simulation

It is plausible that the gain of the first stage transistors, and hence the gain shape of the entire circuit, may be in error due to the fact that they were biased differently to the conditions assumed in the linear transistor models. This was investigated by generating S-parameters for the actual bias points from the new TRW semiphysical HEMT models (TRW_HEMT_BETA_2_0). However, as can be seen in Fig. B1, this did not affect the circuit sufficiently to explain the observed effects. It only reduced the overall gain by about 1.8 dB and did not impart any noticeable gain slope. There is a significant difference in S_{11} , but it is no closer to the measured S_{11} . As could be expected, there is something more sinister occurring.

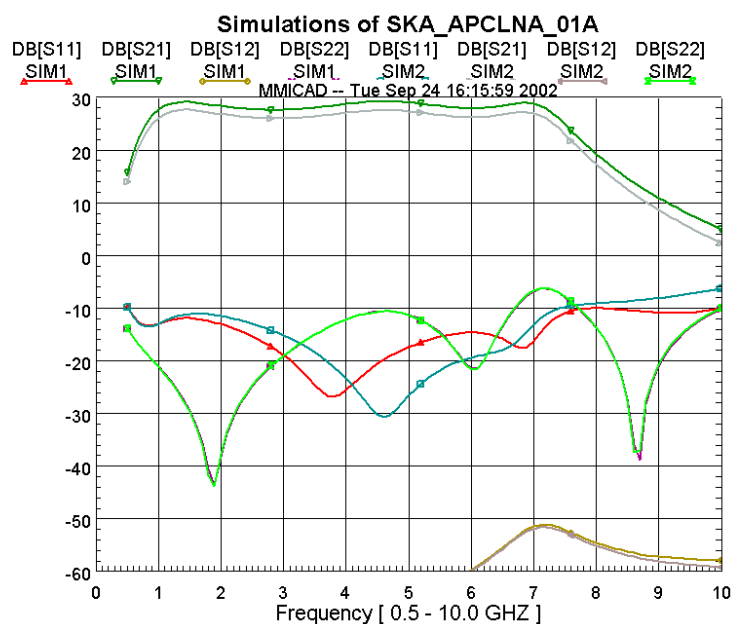


Fig. B1. A simulation of the circuit at its nominal bias point (SIM1) and a second simulation where the first stage is modelled with a bias of 3 V and 50 mA/mm which is much closer to its actual operating point during testing (SIM2).

Faulty Power Supply

It is of course possible that the problems with the first stage were due to a faulty gate power supply. The power supply used for the first stage gate actually had its lid removed at the time of Testing. It has also been suggested that the power supplies used are not good at accepting current, and should be replaced with a high quality digital power supply similar to that used for the drain bias during testing [5]. This possibility was ruled out by using different power supplies in further testing.

Overcompensation of the interstage gain equalisation filter

An overcompensation in the interstage gain equalisation filter could cause the observed gain slope. However, an error at this point would be likely to affect the final gain slope as well. This is not observed. Furthermore, this would not explain the oddities of the first stage biasing.

Additional capacitance in the output of each transistor

Small positive gain slopes are often observed in MMIC LNAs and are often attributed to poorly modelled output capacitances in transistor models [6]. However, it is unlikely that this would cause a discrepancy of the magnitude observed here.