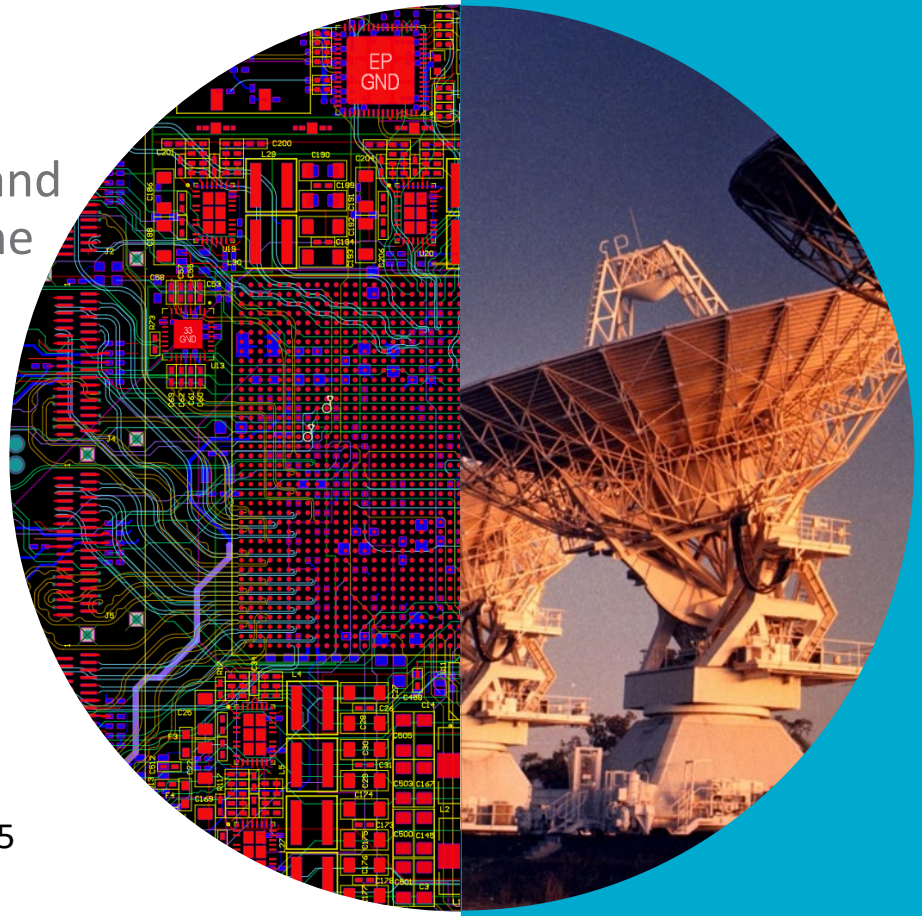
A Single-Chip Wideband Digital Receiver for the Australia Telescope Compact Array Upgrade



John Tuthill | 19 August 2025

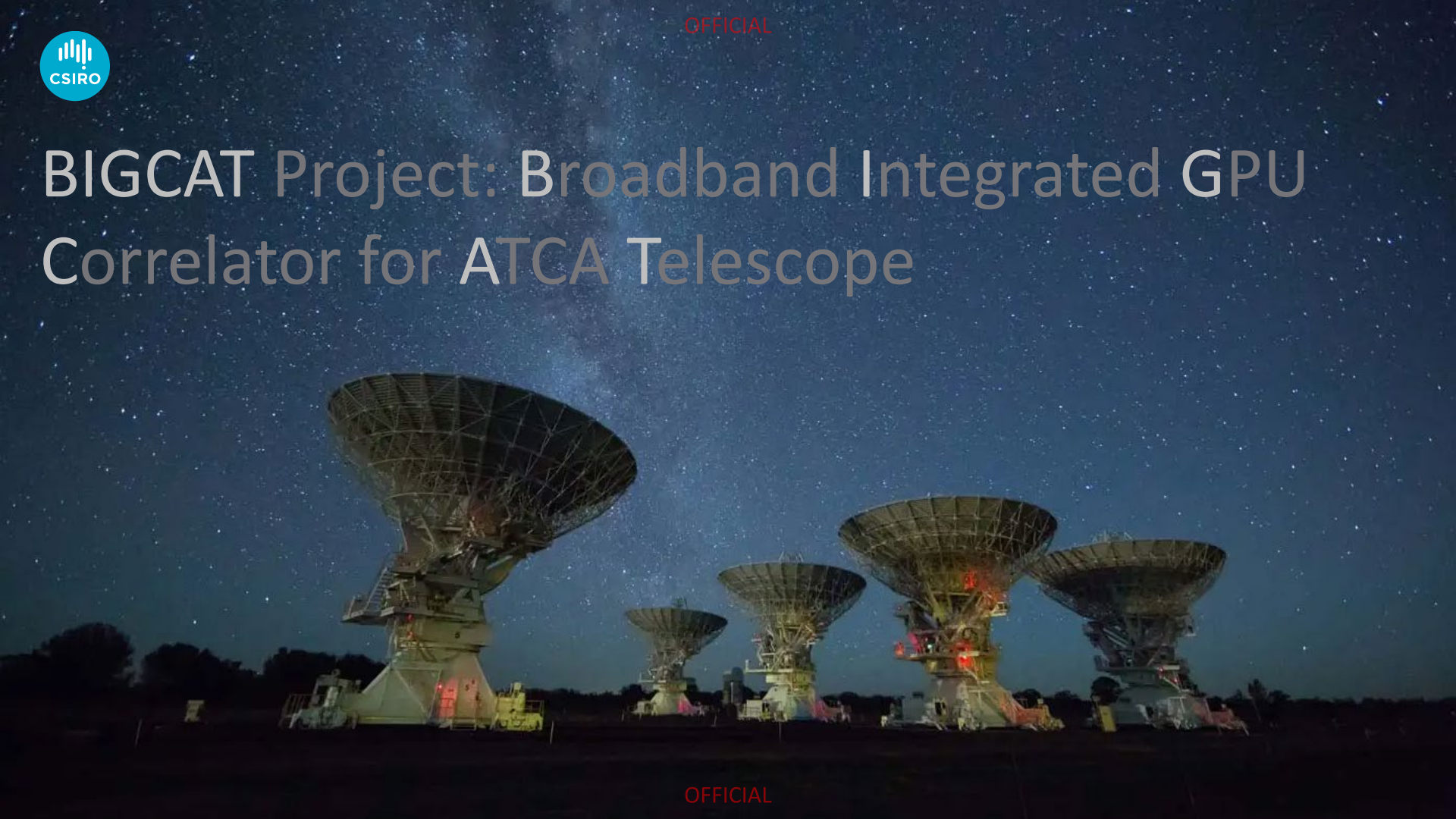
Australia Telescope Compact Array, Narrabri

I begin by acknowledging the **Gadigal people of the Eora Nation** as the Traditional Owners of the land and coastal waters of this place I'm presenting from today. I pay my respect to their Elders past and present and extend this to any First Nations people here today.

The team:

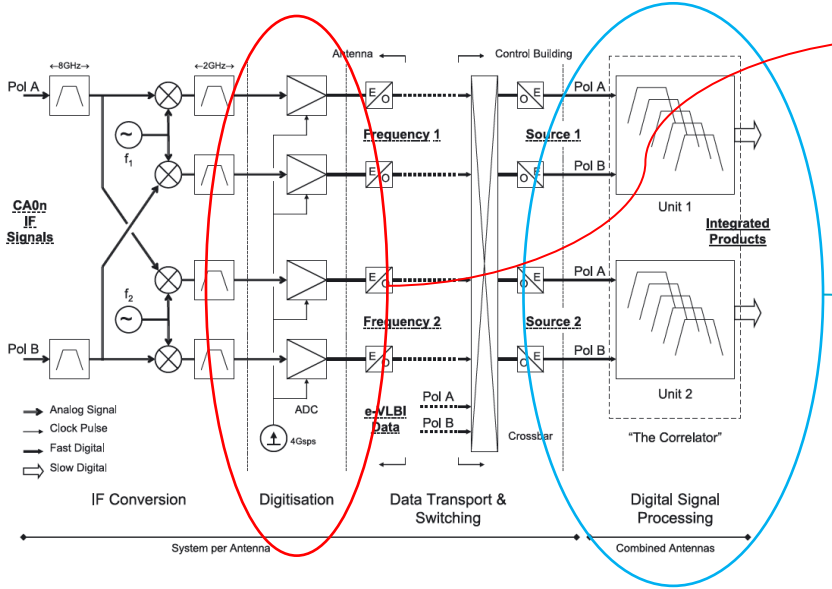
Mia Baquiran, Daniel George, Samantha Gordon, Paul Roberts, Grant Perry, Chris Phillips, Peter Roush

BIGCAT Project: Broadband Integrated GPU Correlator for ATCA Telescope

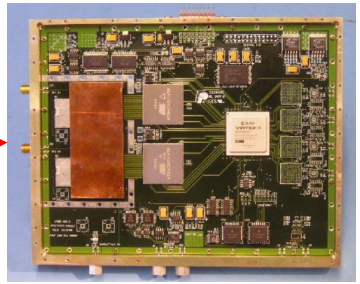


CABB:

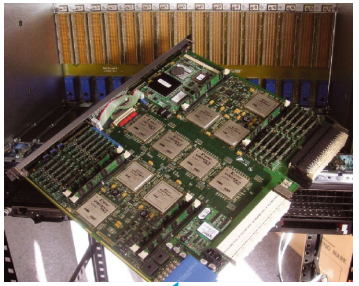
Compact Array Broadband Backend



CABB Digitisers:
4,096 MSamp/sec, 10-bit custom-designed interleaved converters



CABB FPGA Channeliser and Correlator card:
Xilinx Series-4 FPGAs
(Virtex-4 discontinued 2015)



CABB FPGA Correlator cabinet

Images: W. E. Wilson, et. al., The Australia Telescope Compact Array Broad-band Backend: description and first results, Monthly Notices of the Royal Astronomical Society, Volume 416, Issue 2, September 2011, Pages 832–856, https://doi.org/10.1111/j.1365-2966.2011.19054.x

BIGCAT Digital Systems Upgrade

Existing Infrastructure

LO
(4 GHz – 12 GHz)

New IF Stage

RF Module

4 GHz – 6 GHz
6 GHz – 8 GHz
8 GHz – 10 GHz
10 GHz – 12 GHz

Splitter, Filters & LO

New Digitiser and Frequency Channeliser

RFSoC (Jimble)

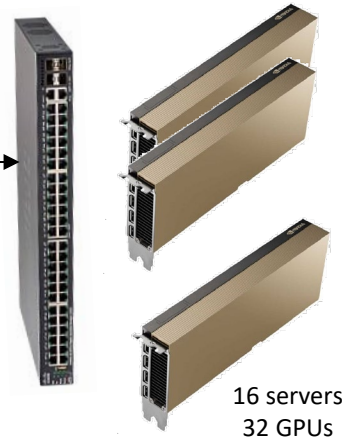
ADCs: 4,096 Msamp/sec @ 14-bits

Channeliser: 16 x 128 MHz channels
Fractionally oversampled by a factor of 32/27
Output re-quantisation to 8 or 16 bits (complex)

Packetiser: CODIF frames over Ethernet (UDP)

100GbE
SMF
~3km

New 100G switch and GPU Cluster (Correlator)

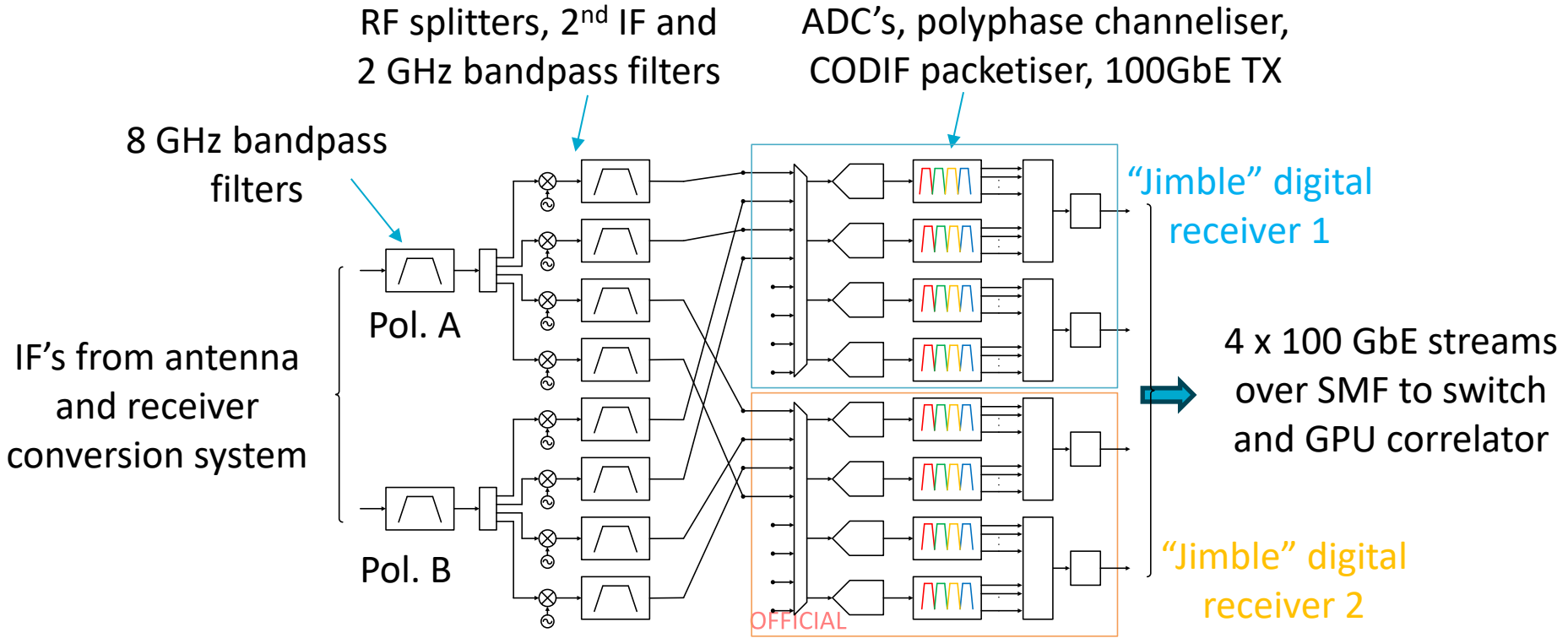


16 servers
32 GPUs

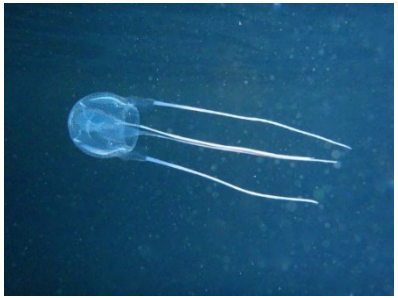
Per Antenna

Correlator Room

BIGCAT System Overview per Antenna

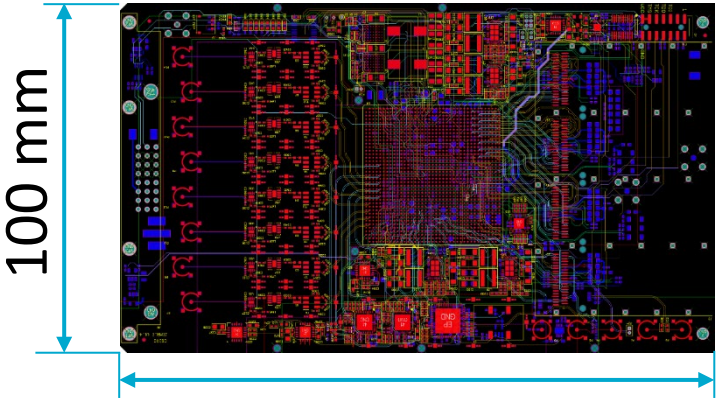


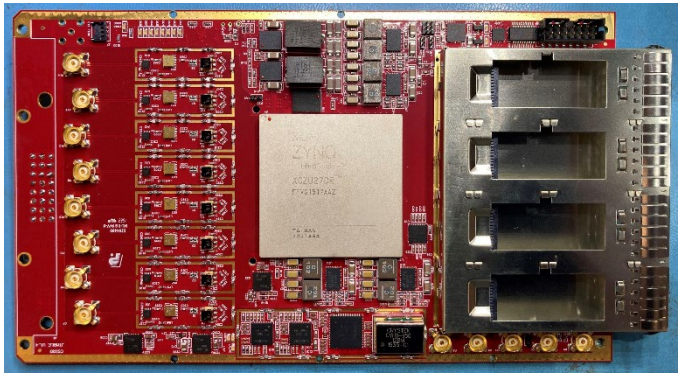
“Jimble” Digital Receiver Hardware



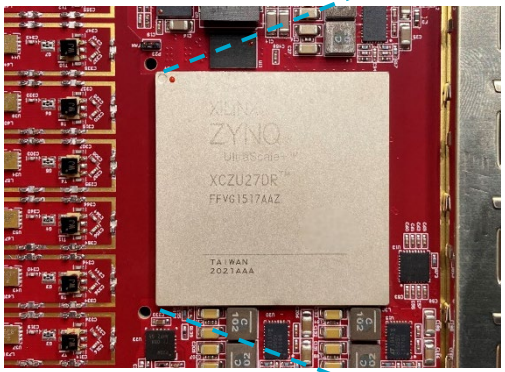
Jimble jellyfish, Carybdea rastoni

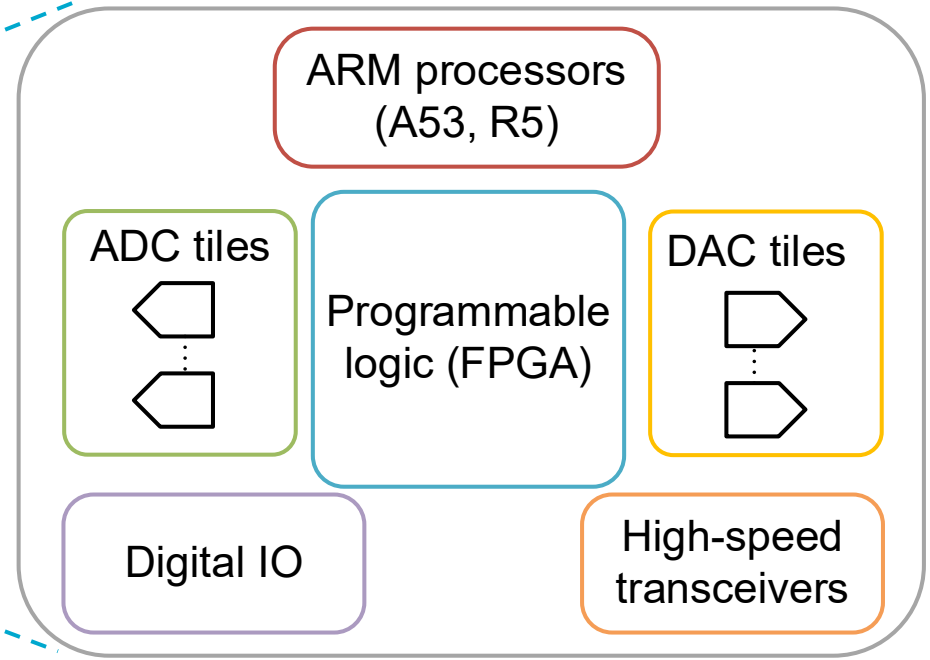
- Analogue BW = 6 GHz (processed BW = 2 GHz)
- 8 x RF inputs, simultaneous sampling @ 4096 MHz and 14-bits
- 2 x 100GbE QSFP+ outputs for BIGCAT (3 available)
- Eurocard form factor @ ~70W per card



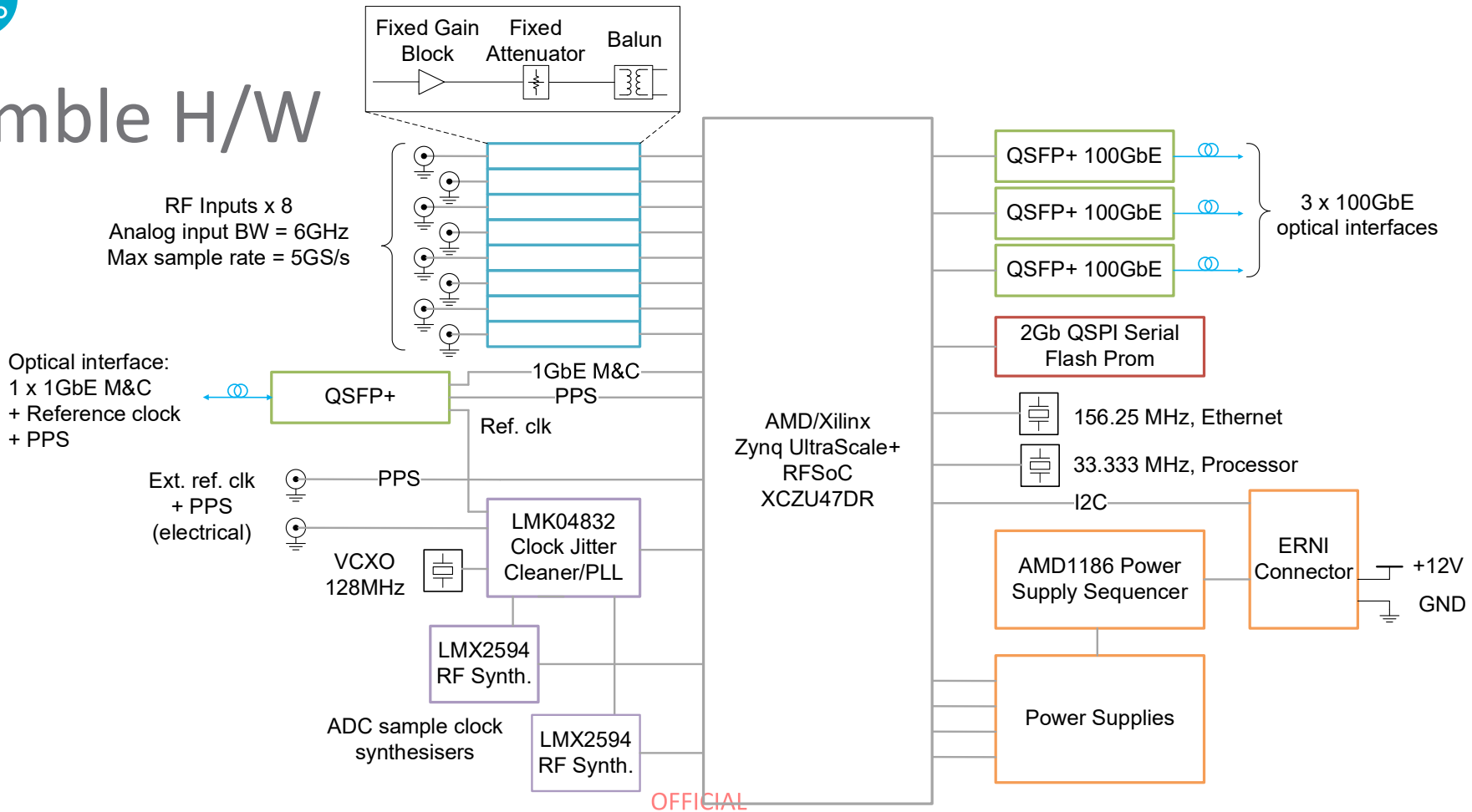


AMD/Xilinx Zynq UltraScale+ RFSoC





Jimble H/W


Fixed Gain Block
Fixed Attenuator
Balun
RF Inputs x 8
Analog input BW = 6GHz
Max sample rate = 5GS/s
Optical interface:
1 x 1GbE M&C
+ Reference clock
+ PPS
QSFP+
1GbE M&C
PPS
Ref. clk
Ext. ref. clk
+ PPS
(electrical)
PPS
VCXO
128MHz
LMK04832
Clock Jitter
Cleaner/PLL
LMX2594
RF Synth.
ADC sample clock
synthesisers
LMX2594
RF Synth.
AMD/Xilinx
Zynq UltraScale+
RFSoC
XCZU47DR
QSFP+ 100GbE
QSFP+ 100GbE
QSFP+ 100GbE
3 x 100GbE
optical interfaces
2Gb QSPI Serial
Flash Prom
156.25 MHz, Ethernet
33.333 MHz, Processor
I2C
AMD1186 Power
Supply Sequencer
ERNI
Connector
+12V
GND
Power Supplies

Sample clock VCXO selection

- Sample clock jitter couples directly to output sample noise
- Mechanical vibration (microphonic) effects on VCXO must also be considered

Measurement Integration range is 100Hz to 1MHz				
Model	Frequency (MHz)	Int. Phase Noise (dBc)	rms jitter	radians
Crystek	128	-79.23	192 fs	154 uRad
Crystek+Vibrations	128	-65.74	907 fs	730uRad
ABLNO_V_125	125	-77.65	236 fs	185 uRad
ABLNO_V_125+Vibrations	125	-68.84	651 fs	511 uRad
Rakon V4180	122.88	-83.86	117 fs	91 uRad
Rakon V4180 + Vibrations	122.88	-60.87	1.66 ps	1.28 mRad

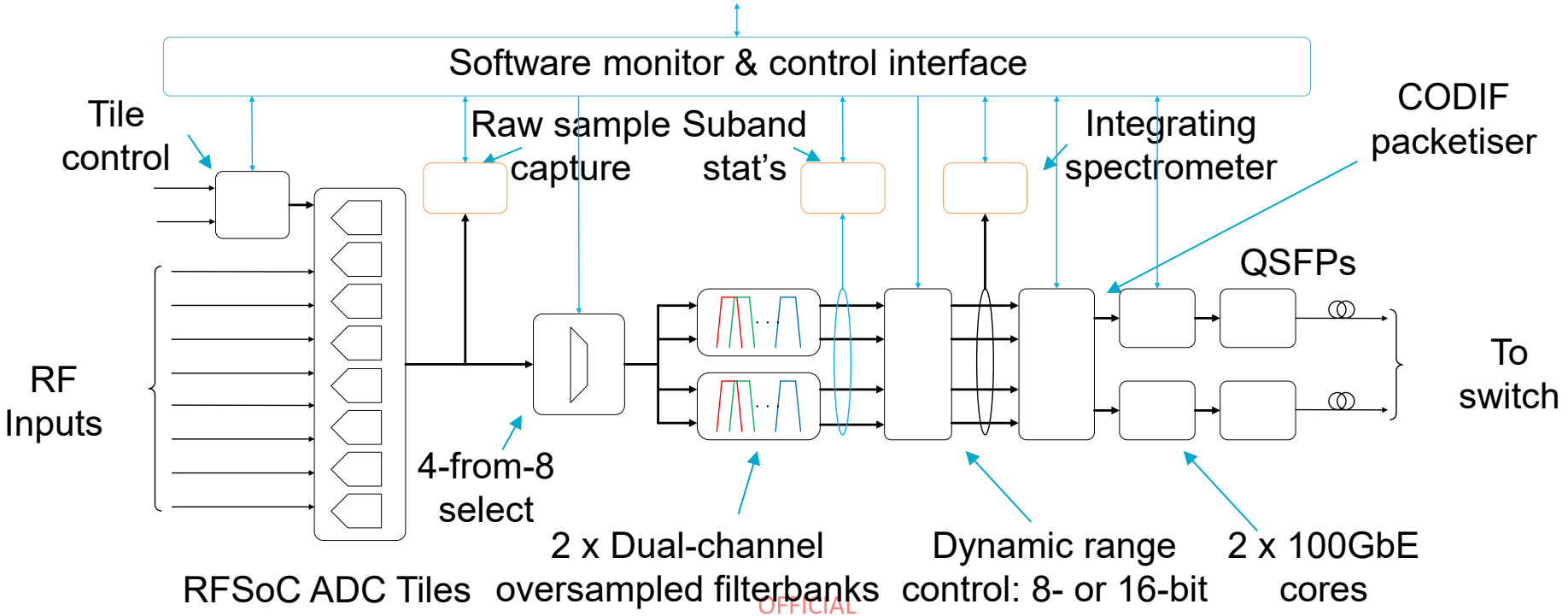
Reference Clock and Timing Synchronisation

The heart of a multi-channel synchronous sampling receiver

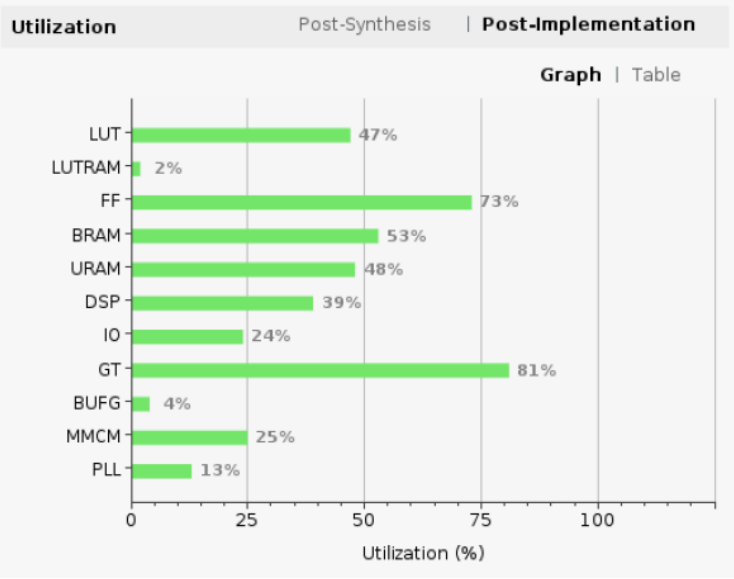
3-step process:

1. Hardware synchronisation of the board clock across multiple Jimble boards
   - ADC sample clocks always phase locked and edge-aligned
   - SYSREF signals synchronised using the distributed PPS
2. ADC synchronisation
   - Multi-tile sync process across the RFSoC devices using the SYSREF signal and a target latency
3. DSP and streaming output synchronisation and time-stamping
   - PPS synchronised event signal

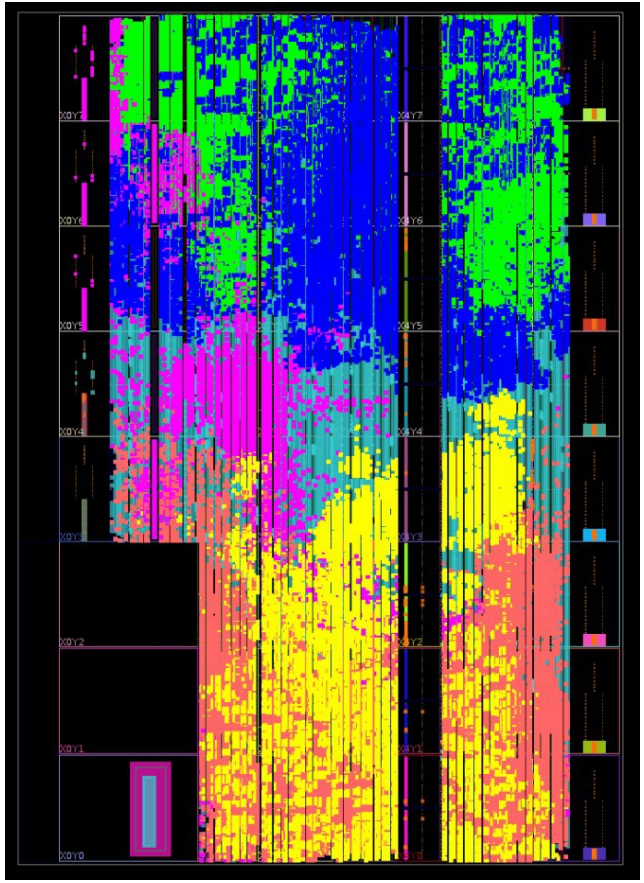
FPGA Firmware and Signal Path



FPGA Build



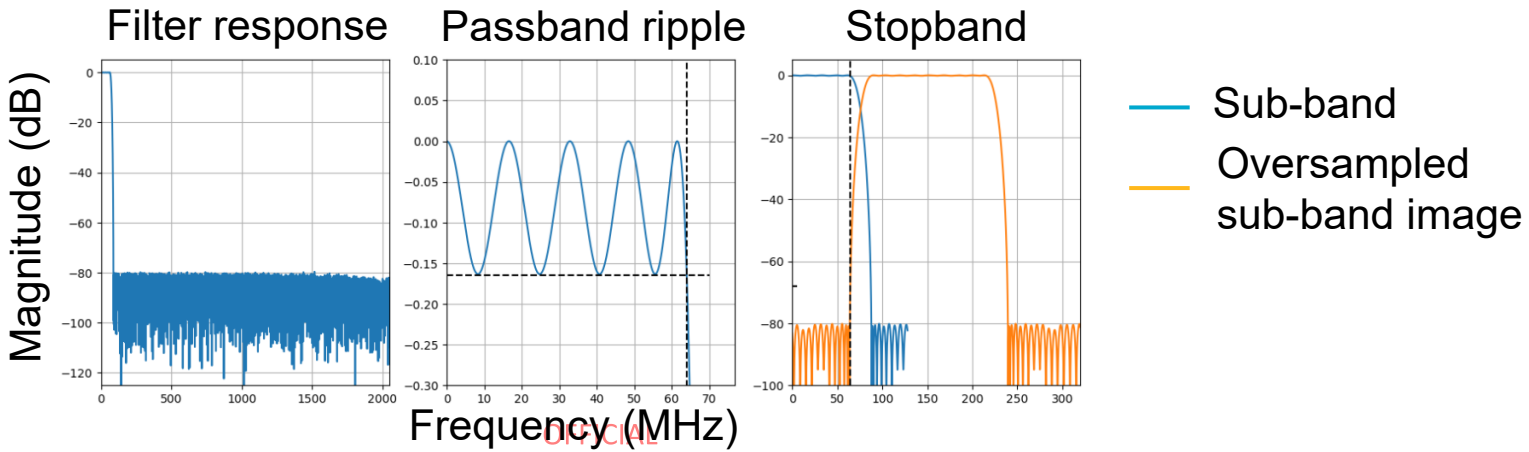
FPGA resource utilisation



FPGA floorplan

Polyphase Filterbank Frequency Channeliser

- Prototype filter: 576 taps
- Oversampling ratio = 32/27
- Stop-band attenuation > 80dB
- Pass-band ripple <0.2dB



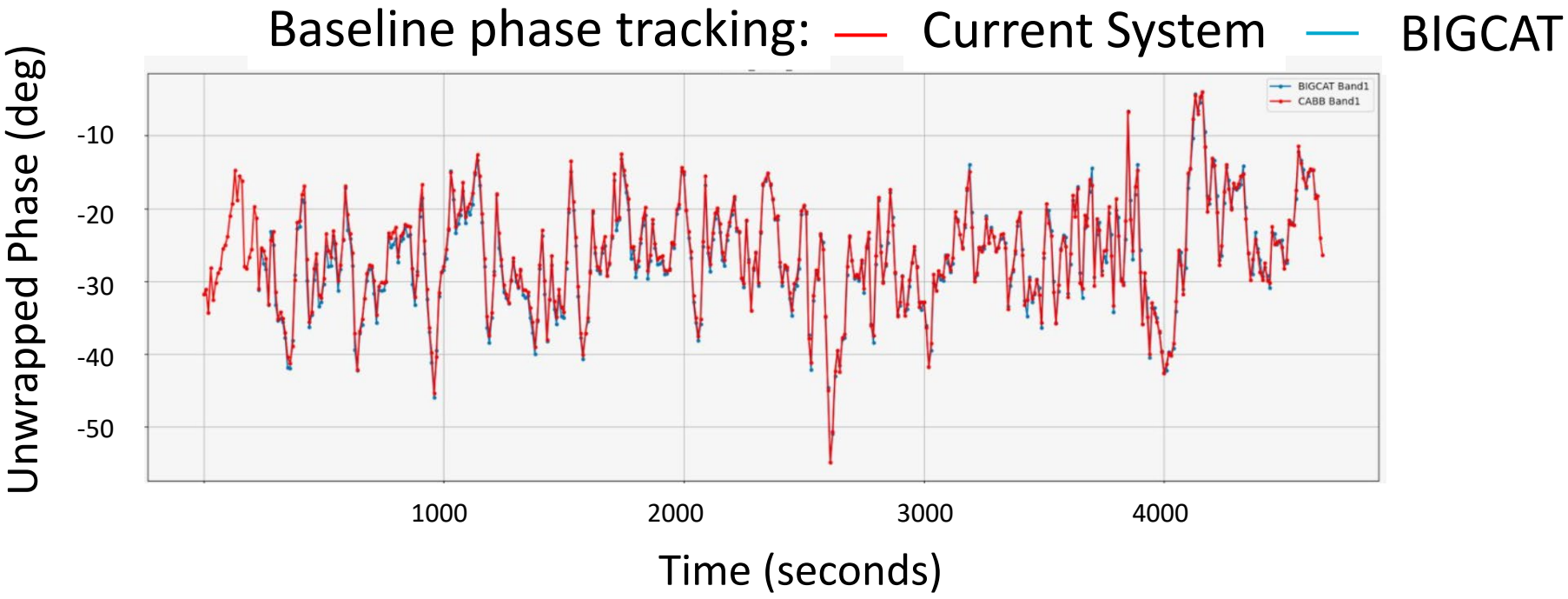
Streaming Data Interface

- 2 x 100GE (3 x 100GE interfaces possible)
- CODIF encapsulation in Ethernet UDP
  - CODIF: CSIRO Oversampled Data Interchange Format
  - Originally an extension of the VDIF standard to support fractionally oversampled data streams
  - 8 x 64-bit word header: timing, source and data payload details
  - Data array payload: user-defined length typically constrained by network factors such as MTU size.

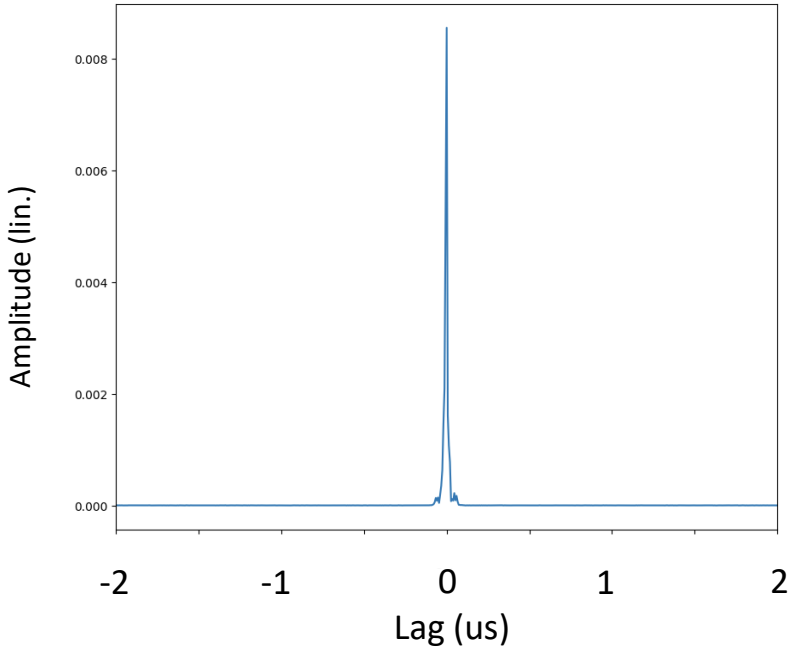
Software Monitoring and Control

- Python and Rust framework using the open source ZeroMQ messaging lib.
- Controls:
  - initialisation and synchronisation process
  - Dynamic range in the streaming output
  - Configuration, starting and stopping of the 100GE streams
  - Precisely timed event-based system functions
- Monitors:
  - Jimble hardware status – power supplies, temperatures, reference oscillator status
  - Signal chain – ADC histograms, subband statistics, integrated power spectra
  - Output stream status

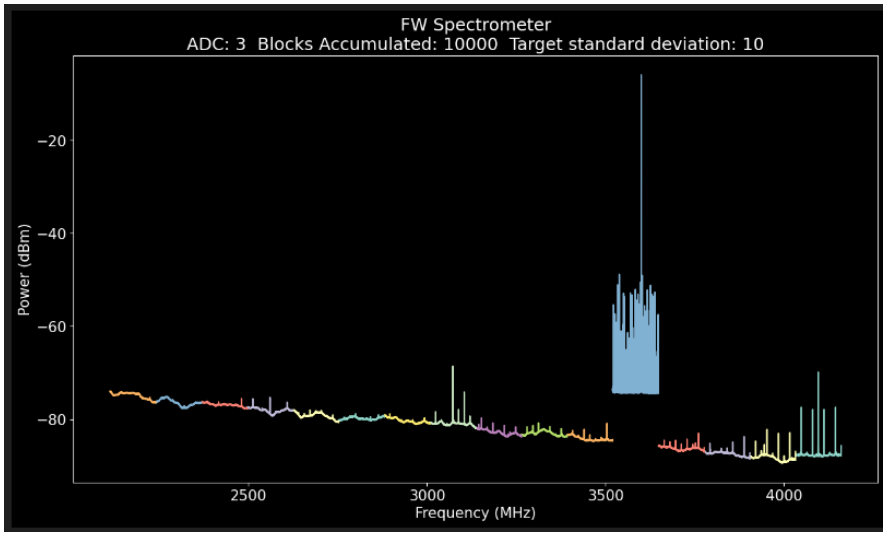
Performance against existing system



Results

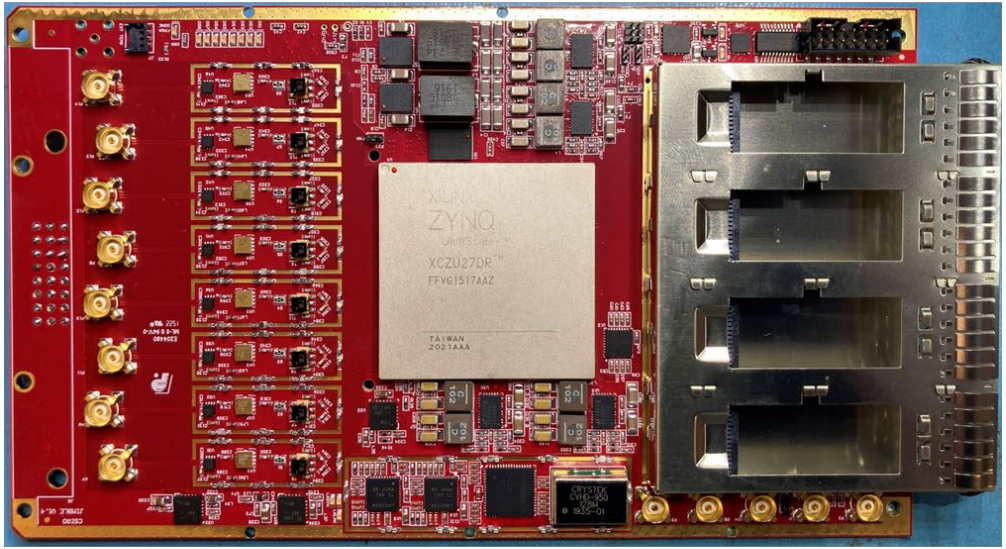


Two-Jimble cross-correlation lag spectrum



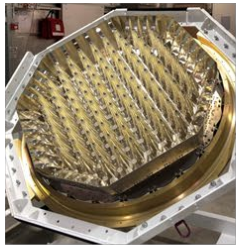
Subband integrated power spectrum from FPGA firmware spectrometer
(Strong test tone evident in 12th subband)

Jimble digital receiver



BIGCAT

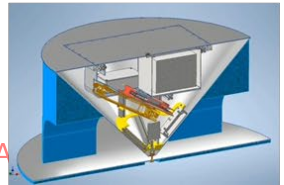
CryoPAF

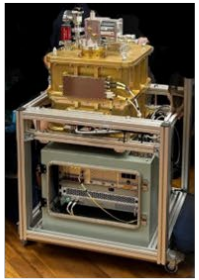


Parkes UW-M/H

JPL DSN receiver

GINAN





Thank you

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