Australia Telescope National Facility

AUSTRALIA TELESCOPE DISTRIBUTED CLOCK DISPLAY

USERS MANUAL

Paul Hales 5th April 2001

CONTENTS

1 Introduction

The ATDCD takes as input, a 1MHz pulse width modulated timeframe signal from the ATDC. This signal is demodulated and decoded to recover the raw timeframe data. The relevant time information is extracted from this data and displayed on segmented displays. The ATDCD is a portable device housed in an aesthetically pleasing enclosure that offers water and ingress protection as well as EMC shielding.

The unit has been constructed such that it can be used as a handheld device, used on a desk with a mini tripod support, or mounted on a wall via the supplied wall brackets or a swivel joint.

This document gives information on how to use the ATDCD, explains its functionality and describes its construction.

2 Input/Output Connectors

Figure 1: Front view of I/O panel

Figure 2: Back view of I/O panel

2.1 Inputs

2.1.1 Time Frame

Either a D9 or RJ-45 connector can be used to connect the Time Frame signal to the ATDCD. The pin-outs for each connector are given in the following table:

	D9	**RJ-45**
+Signal	1	4
-Signal	6	5
GND	5	3

2.1.2 Power

Power is supplied to the ATDCD via a 240V mains lead. This mains voltage is internally converted to the required 5VDC supply needed to power the main circuit board.

2.2 Outputs

2.2.1 Time Frame – D9 or RJ-45

The Time Frame is output from the unit via both a D9 and a RJ-45 connector. If the unit is the last in the line, then an external terminator is required on one of the output connectors to terminate the line. A terminator housed in a yellow D9 shell is supplied with the unit.

2.2.2 VCO - 50W BNC

An onboard voltage controlled oscillator is used as part of the PLL circuit. The clock signal from this oscillator is output via this BNC connector. When the PLL is locked, the VCO output will be in sync with the input 1MHz Time Frame. Two varieties of oscillators were used in the production of the ATDCD. One has a frequency of 50MHz, the other 10MHz.

2.2.3 1ms Sync - 50W BNC

The 1MHz PWM Time Frame encodes two synchronisation signals. One of these occurs every 1ms. When the PLL circuit has locked onto the input Time Frame, the 1ms-synchronisation signal will be output on this BNC connector as a500µs pulse.

2.2.4 1S Sync - 50W BNC

The other synchronisation signal encoded in the 1MHz Time Frame, is the 1s sync. When the PLL circuit has locked onto the input Time Frame, The1s synchronisation signal will be output on the BNC connector as a 1ms pulse.

2.2.5 Raw Data - 50W BNC

As the data is demodulated from the Time Frame, it is output again as raw data to this BNC connector.

2.2.6 Tick Phase - 50W BNC

If a tick phase error occurs (see section), a 1ms pulse will be output on this BNC connector.

2.2.7 Video – D15

This connector is currently unused. It allows for future expansion of the ATDCD to include a video controller board that will output the ATCD information to a VGA monitor via this connector.

3 Functionality

3.1 The Tick Phase Display Window

The Tick Phase display window can display three different pieces of information. Primarily it is used (as the name suggests) to display the current value of the Tick Phase in microseconds. When in this mode, the display also serves as a warning device to alert users that a jump of greater than 100 microseconds has occurred in the Tick Phase, refer to section **3.4 Error Monitoring** for more information on this feature.

The window can also be used to display the current value of the 64-bit Binary Atomic Time (BAT) register. As there are only ten characters available for displaying information in this window, and there are 64 bits in the BAT, the full BAT cannot be displayed at one time. To overcome this problem, the 64 bit BAT is displayed by either the 24 most significant bits or the 40 least significant bits.

The three buttons located below window give control over what information is displayed. These buttons are labelled BAT LOW, BAT HIGH and TICK PHASE.

The BAT LOW button displays the 40 least significant bits of the BAT

The BAT HIGH button displays the 24 most significant bits of the BAT

The TICK PHASE button displays the current Tick Phase in microseconds.

You can determine what is being displayed in the window by looking at which button is currently highlighted by is respective LED indicator.

3.2 Brightness Control

The are two modes of control for varying the brightness of the ATDCD, these are Manual or Automatic. The user can toggle between these two modes by simultaneously pressing the brightness down and brightness up buttons. It is often easier to perform this operation by the following method:

1. Press and hold the brightness down button with the index finger of the left hand
2. Immediately after, press the brightness up button with the index finger of the right hand
3. Release both fingers at the same time.

3.2.1 Manual Brightness Control

When in Manual mode, the brightness can be varied via the up/down brightness control buttons located at the lower left of the control panel. There are five levels of brightness to select from.

3.2.2 Automatic Brightness Control

When in Automatic mode, the brightness is controlled by a Light Dependant Resistor, which is located in the upper left-hand corner of the control panel. Again there are five discrete levels of brightness, the level selected will depend on the brightness of the ambient lighting. The brightness level will become brighter or duller in synchronisation with the ambient lighting.

Note:
In the transitional periods between one level an the next, the brightness may be seen to change back and forth between two levels until the ambient light moves out of the transitional range. This is normal and does not mean the unit is malfunctioning.

3.3 Audio

The Audible one second beep can be toggled on and off via the SPEAKER button. Once toggled on, a short tone will be heard each time the 1s synchronisation signal is received. If the time frame is disconnected from the ATDCD, the audible tone will cease.

The volume of the audible tone can be controlled via the VOLUME UP and VOLUME DOWN buttons. There are five discrete levels of volume.

3.4 Error Monitoring

3.4.1 Error LED'S

The ATDCD has the ability to detect and log time frame errors. These include:

- ⊕ GPS TICK LOST – The GPS tick signal is not detected at the ATDC.
- LOCAL PLL UNLOCKED – The local VCO PLL is out of lock.
- ⊕ ATDC PLL UNLOCKED – The ATDC PLL is out of lock.
- CRC FRAME ERROR – A bit error has occurred in the timeframe.
- LENGTH FRAME ERROR – A time frame length underrun or overrun has occurred.
- ⊕ IERSA TABLE LOW – The ATDC IERSA table is low.
- ⊕ IERSA TABLE EMPTY – The ATDC IERSA table is empty.
- ⊕ OTHER ERROR – As yet undefined.

⊕ Error logging not implemented in the as of 5/4/2001

Once an error is logged, it will remain logged until an Error Clear function is performed. This is done by pressing and holding the ERROR CLEAR button for two seconds. A beep will be heard when the button is first pressed, and another after two seconds when the errors are cleared.

Whenever the power is applied to the unit, the unit undergoes a System Reset, or the time frame is disconnected, the following errors will be logged:

- ATDCD PLL ERROR
- CRC FRAME ERROR
- LENGTH FRAME ERROR

An Error Clear will have to be performed before correct monitoring can begin.

3.4.2 Tick Phase Error

If a tick phase jump of greater than ±100µs is detected in one second, then a tick phase error is logged. The tick phase display window flashing at a frequency of 1Hz indicates this error. This error can be cleared by performing and Error Clear function as described above.

3.5 System Reset

If the ATDCD gets into an invalid state, a System Reset may need to be performed. To do this, press and hold the SYSTEM RESET button for two seconds. Remember to perform an Error Clear after a System Reset.

All user settings are stored in non-volatile RAM. This means that the last setting will be restored upon power up or system reset. The following settings will be restored:

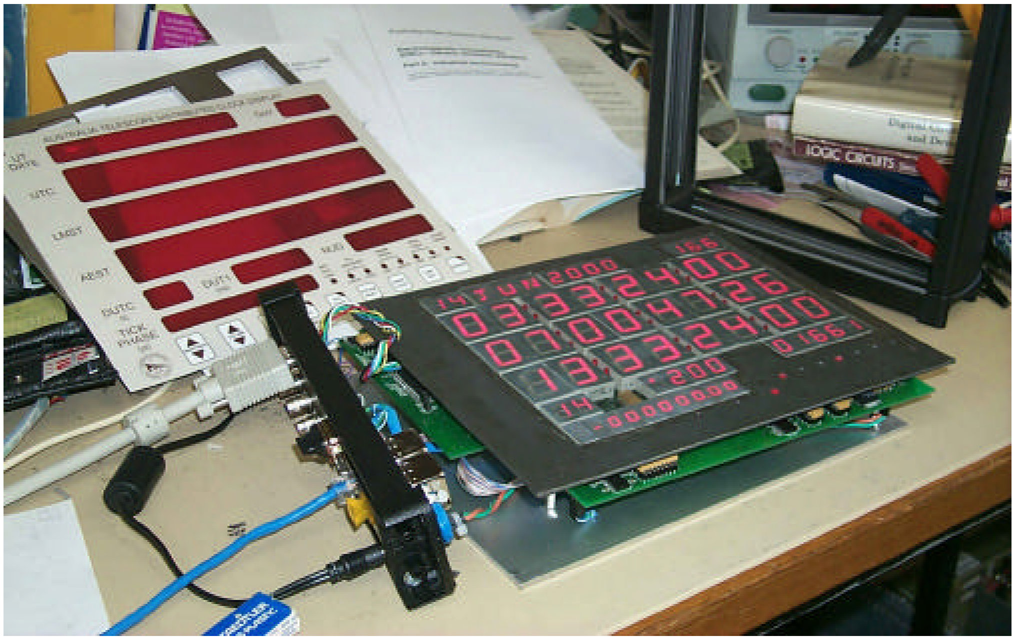
- Automatic or Manual brightness control.
- Brightness level if in manual mode
- Speaker on or off
- Speaker volume
- Tick phase display – BAT High/BAT Low/Tick Phase.

3.6 Lamp Test

To test the state of the LED displays, press and hold the LAMP TEST button. All LED’s in the ATDCD will be illuminated as long as this button is pressed. To limit current drain, the LED’s are illuminated at the lowest brightness level. For this reason it is best to perform this test in a room with low ambient lighting. This is especially true for the green and orange ATDCD’s.

4 Construction

4.1 Enclosure construction

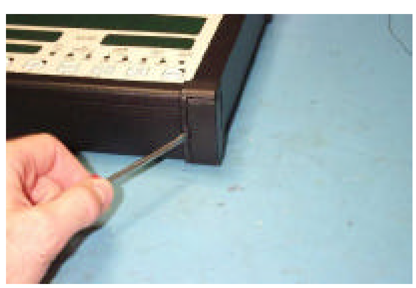


The requirements for the enclosure were that it protected the electronics from the environment (dust and water), provided a shield against Radio Frequency Interference RFI and was aesthetically pleasing.

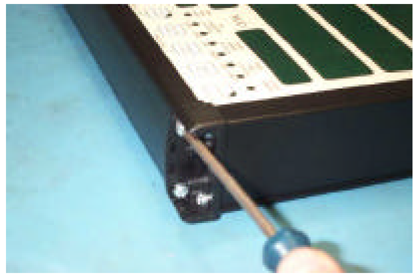
The box used is an Aluplan from Bopla. It is constructed from four pieces of aluminium extrusion, a 3mm rectangular aluminium plate for the base and a 3mm front panel.

To disassemble the housing use the following steps:

1. Remove the power.
2. Remove the four corner covers with a flat blade screwdriver.

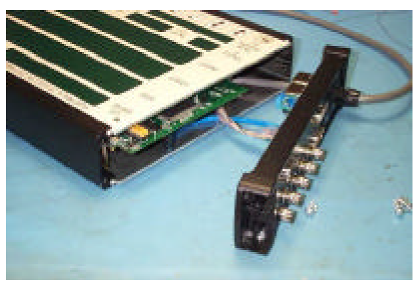


3. Working on the right hand flat panel (opposite to connector end), loosen the four screws going into the rounded sides, but do completely remove them.

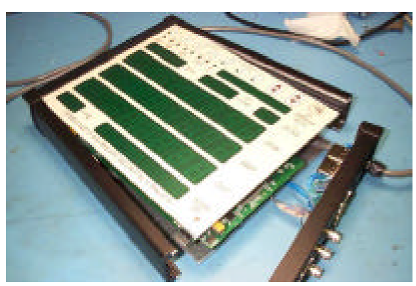


4. Working on the connector end, loosen and remove the four screws going into the rounded sides.

5. Pull the connector side away from the rest of the enclosure, but be careful not to damage the wiring coming away from the connectors.

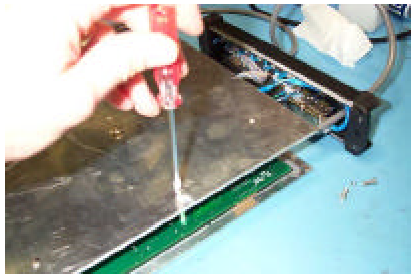


6. Pull the rounded sides out to the limit of the loosened screws from step 3.

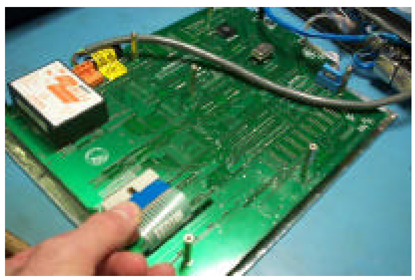


7. Pull the flat connectorless end and the rounded sides to the right as one unit.

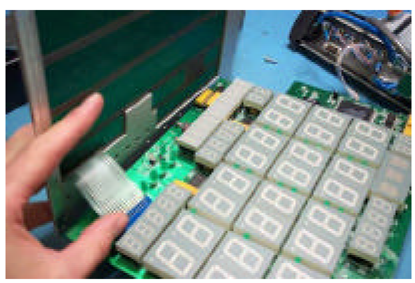
8. Turn the ATDCD over and unscrew the 7 mounting screws and remove the bottom plate.



9. Unclip front panel ribbon cable.

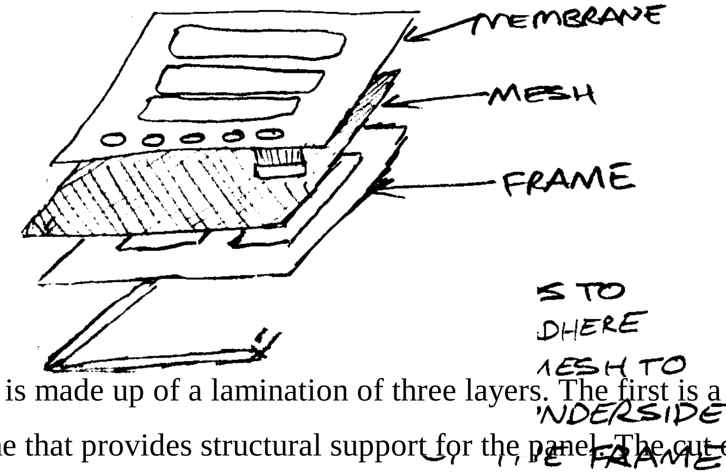


10. Disconnect the power cable, output ribbon cable and input time frame connector as necessary.
11. Turn the ATDCD over and lift off the front panel.



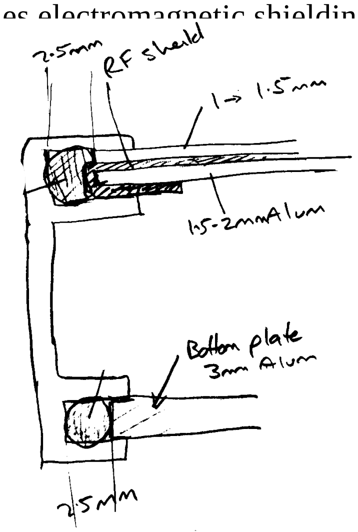
Carry out the steps in reverse order to reassemble.

4.2 Front Panel



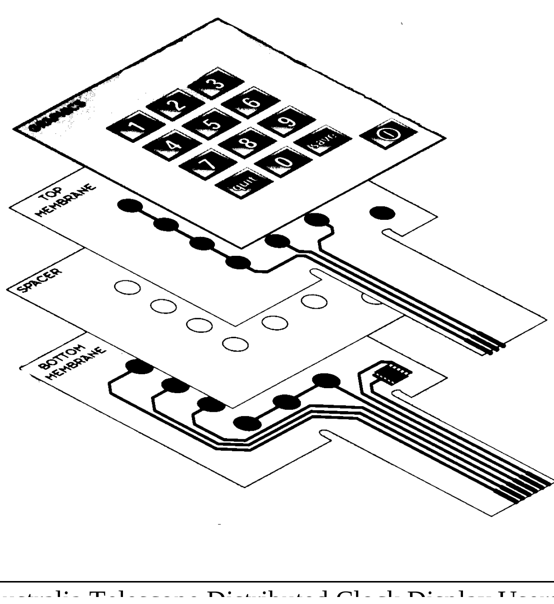
The front panel is made up of a lamination of three layers. The first is a 1.5mm aluminium frame that provides structural support for the panel. The cut-outs and holes in this frame have been milled to shape so that the frame sits around the outside of the segment displays.

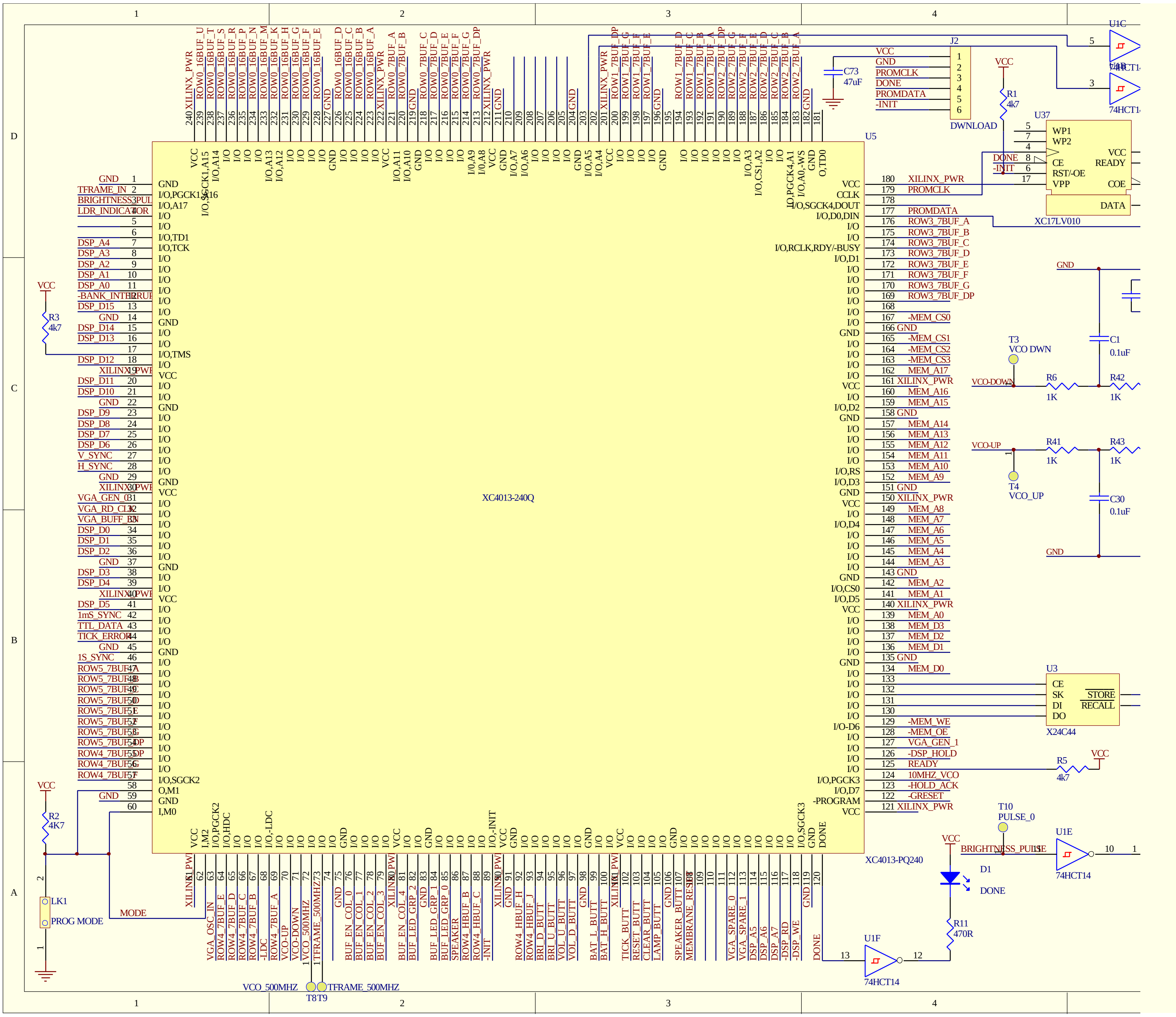
Next a 100 OPI blackened copper mesh is wrapped around the frame and held in place with conductive aluminium tape. This mesh provides electromagnetic shielding over the open area of the frame.



The third layer is comprised of a graphical and
the colour filtering, graphics, further shielding a
joined to the frame and mesh by an adhesive on

The membranes used were supplied by Sun Indu





XC4013-240Q
XC4013-PQ240
U5
J2
DWNLOAD
VCC
GND
PROMCLK
DONE
PROMDATA
-INIT
C73
47uF
R1
4k7
U37
XC17LV010
WP1
WP2
CE
RST/-OE
VPP
READY
COE
DATA
U1C
U1D
U1E
U1F
74HCT14
T3
VCO DWN
T4
VCO_UP
VCO-DOWN
VCO-UP
R6
R42
R41
R43
1K
C1
C30
0.1uF
U3
X24C44
SK
DI
DO
STORE
RECALL
R5
R3
4k7
R2
4K7
LK1
PROG MODE
MODE
T10
PULSE_0
BRIGHTNESS_PULSE
D1
DONE
R11
470R
T8
T9
VCO_500MHZ
TFRAME_500MHZ
XILINX_PWR
TFRAME_IN
BRIGHTNESS_PULSE
LDR_INDICATOR
DSP_A4
DSP_A3
DSP_A2
DSP_A1
DSP_A0
-BANK_INTERRUPT
DSP_D15
DSP_D14
DSP_D13
DSP_D12
DSP_D11
DSP_D10
DSP_D9
DSP_D8
DSP_D7
DSP_D6
V_SYNC
H_SYNC
VGA_GEN_0
VGA_RD_CLK
VGA_BUFF_EN
DSP_D0
DSP_D1
DSP_D2
DSP_D3
DSP_D4
DSP_D5
1mS_SYNC
TTL_DATA
TICK_ERROR
1S_SYNC
ROW5_7BUF_A
ROW5_7BUF_B
ROW5_7BUF_C
ROW5_7BUF_D
ROW5_7BUF_E
ROW5_7BUF_F
ROW5_7BUF_G
ROW5_7BUF_DP
ROW4_7BUF_DP
ROW4_7BUF_G
ROW4_7BUF_F
ROW3_7BUF_A
ROW3_7BUF_B
ROW3_7BUF_C
ROW3_7BUF_D
ROW3_7BUF_E
ROW3_7BUF_F
ROW3_7BUF_G
ROW3_7BUF_DP
-MEM_CS0
-MEM_CS1
-MEM_CS2
-MEM_CS3
MEM_A17
MEM_A16
MEM_A15
MEM_A14
MEM_A13
MEM_A12
MEM_A11
MEM_A10
MEM_A9
MEM_A8
MEM_A7
MEM_A6
MEM_A5
MEM_A4
MEM_A3
MEM_A2
MEM_A1
MEM_A0
MEM_D3
MEM_D2
MEM_D1
MEM_D0
-MEM_WE
-MEM_OE
VGA_GEN_1
-DSP_HOLD
READY
10MHZ_VCO
-HOLD_ACK
-GRESET
ROW0_16BUF_U
ROW0_16BUF_T
ROW0_16BUF_S
ROW0_16BUF_R
ROW0_16BUF_P
ROW0_16BUF_N
ROW0_16BUF_M
ROW0_16BUF_K
ROW0_16BUF_H
ROW0_16BUF_G
ROW0_16BUF_F
ROW0_16BUF_E
ROW0_16BUF_D
ROW0_16BUF_C
ROW0_16BUF_B
ROW0_16BUF_A
ROW0_7BUF_A
ROW0_7BUF_B
ROW0_7BUF_C
ROW0_7BUF_D
ROW0_7BUF_E
ROW0_7BUF_F
ROW0_7BUF_G
ROW0_7BUF_DP
ROW1_7BUF_DP
ROW1_7BUF_G
ROW1_7BUF_F
ROW1_7BUF_E
ROW1_7BUF_D
ROW1_7BUF_C
ROW1_7BUF_B
ROW1_7BUF_A
ROW2_7BUF_DP
ROW2_7BUF_G
ROW2_7BUF_F
ROW2_7BUF_E
ROW2_7BUF_D
ROW2_7BUF_C
ROW2_7BUF_B
ROW2_7BUF_A
VGA_OSC_IN
ROW4_7BUF_E
ROW4_7BUF_D
ROW4_7BUF_C
ROW4_7BUF_B
-LDC
ROW4_7BUF_A
VCO-UP
VCO-DOWN
BUF_EN_COL_0
BUF_EN_COL_1
BUF_EN_COL_2
BUF_EN_COL_3
BUF_EN_COL_4
BUF_LED_GRP_2
BUF_LED_GRP_1
BUF_LED_GRP_0
SPEAKER
ROW4_HBUF_B
ROW4_HBUF_C
-INIT
ROW4_HBUF_H
ROW4_HBUF_J
BRI_D_BUTT
BRI_U_BUTT
VOL_U_BUTT
VOL_D_BUTT
BAT_L_BUTT
BAT_H_BUTT
TICK_BUTT
RESET_BUTT
CLEAR_BUTT
LAMP_BUTT
SPEAKER_BUTT
MEMBRANE_RESET
VGA_SPARE_0
VGA_SPARE_1
DSP_A5
DSP_A6
DSP_A7
-DSP_RD
-DSP_WE
1
2
3
4
A
B
C
D

1
2
3
4
D
C
B
A
U38
R0_G0_7SEG_E
R0_G0_7SEG_D
EN_COL_0
R0_G0_7SEG_C
R0_G0_7SEG_DP
R0_G0_7SEG_G
R0_G0_7SEG_F
EN_COL_0
R0_G0_7SEG_A
R0_G0_7SEG_B
SA05-11
U39
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R0_G0_7SEG_B
SA05-11
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R0_G1_7SEG_D
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R0_G1_7SEG_F
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R0_G1_7SEG_B
SA05-11
U59
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ROW0_16SEG_M
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ROW0_16SEG_H
ROW0_16SEG_U
ROW0_16SEG_S
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R1_G0_7SEG_B
SA10-21
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R1_G0_7SEG_F
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R1_G0_7SEG_B
SA10-21
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R1_G0_7SEG_B
SA10-21
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R1_G1_7SEG_B
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R1_G1_7SEG_G
R1_G1_7SEG_F
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R1_G1_7SEG_B
SA10-21
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R2_G0_7SEG_F
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R2_G0_7SEG_B
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R2_G0_7SEG_DP
R2_G0_7SEG_G
R2_G0_7SEG_F
EN_COL_2
R2_G0_7SEG_A
R2_G0_7SEG_B
SA10-21
U67
R2_G0_7SEG_E
R2_G0_7SEG_D
EN_COL_3
R2_G0_7SEG_C
R2_G0_7SEG_DP
R2_G0_7SEG_G
R2_G0_7SEG_F
EN_COL_3
R2_G0_7SEG_A
R2_G0_7SEG_B
SA10-21
U70
R2_G0_7SEG_E
R2_G0_7SEG_D
EN_COL_4
R2_G0_7SEG_C
R2_G0_7SEG_DP
R2_G0_7SEG_G
R2_G0_7SEG_F
EN_COL_4
R2_G0_7SEG_A
R2_G0_7SEG_B
SA10-21
U73
R2_G1_7SEG_E
R2_G1_7SEG_D
EN_COL_0
R2_G1_7SEG_C
R2_G1_7SEG_DP
R2_G1_7SEG_G
R2_G1_7SEG_F
EN_COL_0
R2_G1_7SEG_A
R2_G1_7SEG_B
SA10-21
U62
R3_G0_7SEG_E
R3_G0_7SEG_D
EN_COL_0
R3_G0_7SEG_C
R3_G0_7SEG_DP
R3_G0_7SEG_G
R3_G0_7SEG_F
EN_COL_0
R3_G0_7SEG_A
R3_G0_7SEG_B
SA10-21
U65
R3_G0_7SEG_E
R3_G0_7SEG_D
EN_COL_1
R3_G0_7SEG_C
R3_G0_7SEG_DP
R3_G0_7SEG_G
R3_G0_7SEG_F
EN_COL_1
R3_G0_7SEG_A
R3_G0_7SEG_B
SA10-21
U68
R3_G0_7SEG_E
R3_G0_7SEG_D
EN_COL_2
R3_G0_7SEG_C
R3_G0_7SEG_DP
R3_G0_7SEG_G
R3_G0_7SEG_F
EN_COL_2
R3_G0_7SEG_A
R3_G0_7SEG_B
SA10-21
U71
R3_G0_7SEG_E
R3_G0_7SEG_D
EN_COL_3
R3_G0_7SEG_C
R3_G0_7SEG_DP
R3_G0_7SEG_G
R3_G0_7SEG_F
EN_COL_3
R3_G0_7SEG_A
R3_G0_7SEG_B
SA10-21
U74
R3_G0_7SEG_E
R3_G0_7SEG_D
EN_COL_4
R3_G0_7SEG_C
R3_G0_7SEG_DP
R3_G0_7SEG_G
R3_G0_7SEG_F
EN_COL_4
R3_G0_7SEG_A
R3_G0_7SEG_B
SA10-21
U83
R3_G1_7SEG_E
R3_G1_7SEG_D
EN_COL_2
R3_G1_7SEG_C
R3_G1_7SEG_DP
R3_G1_7SEG_G
R3_G1_7SEG_F
EN_COL_2
R3_G1_7SEG_A
R3_G1_7SEG_B
SA10-21
U47
R4_G0_7SEG_E
R4_G0_7SEG_D
EN_COL_0
R4_G0_7SEG_C
R4_G0_7SEG_DP
R4_G0_7SEG_G
R4_G0_7SEG_F
EN_COL_0
R4_G0_7SEG_A
R4_G0_7SEG_B
SA05-11
U48
R4_G0_7SEG_E
R4_G0_7SEG_D
EN_COL_1
R4_G0_7SEG_C
R4_G0_7SEG_DP
R4_G0_7SEG_G
R4_G0_7SEG_F
EN_COL_1
R4_G0_7SEG_A
R4_G0_7SEG_B
SA05-11
U84
ROW4_HSEG_J
EN_COL_2
ROW4_HSEG_C
EN_COL_2
ROW4_HSEG_H
EN_COL_2
EN_COL_2
ROW4_HSEG_B
FX56-11
U49
R4_G0_7SEG_E
R4_G0_7SEG_D
EN_COL_2
R4_G0_7SEG_C
R4_G0_7SEG_DP
R4_G0_7SEG_G
R4_G0_7SEG_F
EN_COL_2
R4_G0_7SEG_A
R4_G0_7SEG_B
SA05-11
U52
R4_G1_7SEG_E
R4_G1_7SEG_D
EN_COL_0
R4_G1_7SEG_C
R4_G1_7SEG_DP
R4_G1_7SEG_G
R4_G1_7SEG_F
EN_COL_0
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R4_G1_7SEG_B
SA05-11
U56
R4_G1_7SEG_E
R4_G1_7SEG_D
EN_COL_1
R4_G1_7SEG_C
R4_G1_7SEG_DP
R4_G1_7SEG_G
R4_G1_7SEG_F
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R4_G1_7SEG_B
SA05-11
U55
R4_G1_7SEG_E
R4_G1_7SEG_D
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R4_G1_7SEG_C
R4_G1_7SEG_DP
R4_G1_7SEG_G
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SA05-11
U54
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R4_G1_7SEG_F
EN_COL_3
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R4_G1_7SEG_B
SA05-11
U53
R4_G1_7SEG_E
R4_G1_7SEG_D
EN_COL_4
R4_G1_7SEG_C
R4_G1_7SEG_DP
R4_G1_7SEG_G
R4_G1_7SEG_F
EN_COL_4
R4_G1_7SEG_A
R4_G1_7SEG_B
SA05-11
U85
R5_G0_7SEG_A
R5_G0_7SEG_F
EN_COL_2
R5_G0_7SEG_E
EN_COL_2
R5_G0_7SEG_B
R5_G0_7SEG_G
R5_G0_7SEG_C
R5_G0_7SEG_DP
R5_G0_7SEG_D
SA03-11
U87
R5_G0_7SEG_A
R5_G0_7SEG_F
EN_COL_3
R5_G0_7SEG_E
EN_COL_3
R5_G0_7SEG_B
R5_G0_7SEG_G
R5_G0_7SEG_C
R5_G0_7SEG_DP
R5_G0_7SEG_D
SA03-11
U88
R5_G0_7SEG_A
R5_G0_7SEG_F
EN_COL_4
R5_G0_7SEG_E
EN_COL_4
R5_G0_7SEG_B
R5_G0_7SEG_G
R5_G0_7SEG_C
R5_G0_7SEG_DP
R5_G0_7SEG_D
SA03-11
U89
R5_G1_7SEG_A
R5_G1_7SEG_F
EN_COL_0
R5_G1_7SEG_E
EN_COL_0
R5_G1_7SEG_B
R5_G1_7SEG_G
R5_G1_7SEG_C
R5_G1_7SEG_DP
R5_G1_7SEG_D
SA03-11
U90
R5_G1_7SEG_A
R5_G1_7SEG_F
EN_COL_1
R5_G1_7SEG_E
EN_COL_1
R5_G1_7SEG_B
R5_G1_7SEG_G
R5_G1_7SEG_C
R5_G1_7SEG_DP
R5_G1_7SEG_D
SA03-11
U86
R5_G1_7SEG_A
R5_G1_7SEG_F
EN_COL_4
R5_G1_7SEG_E
EN_COL_4
R5_G1_7SEG_B
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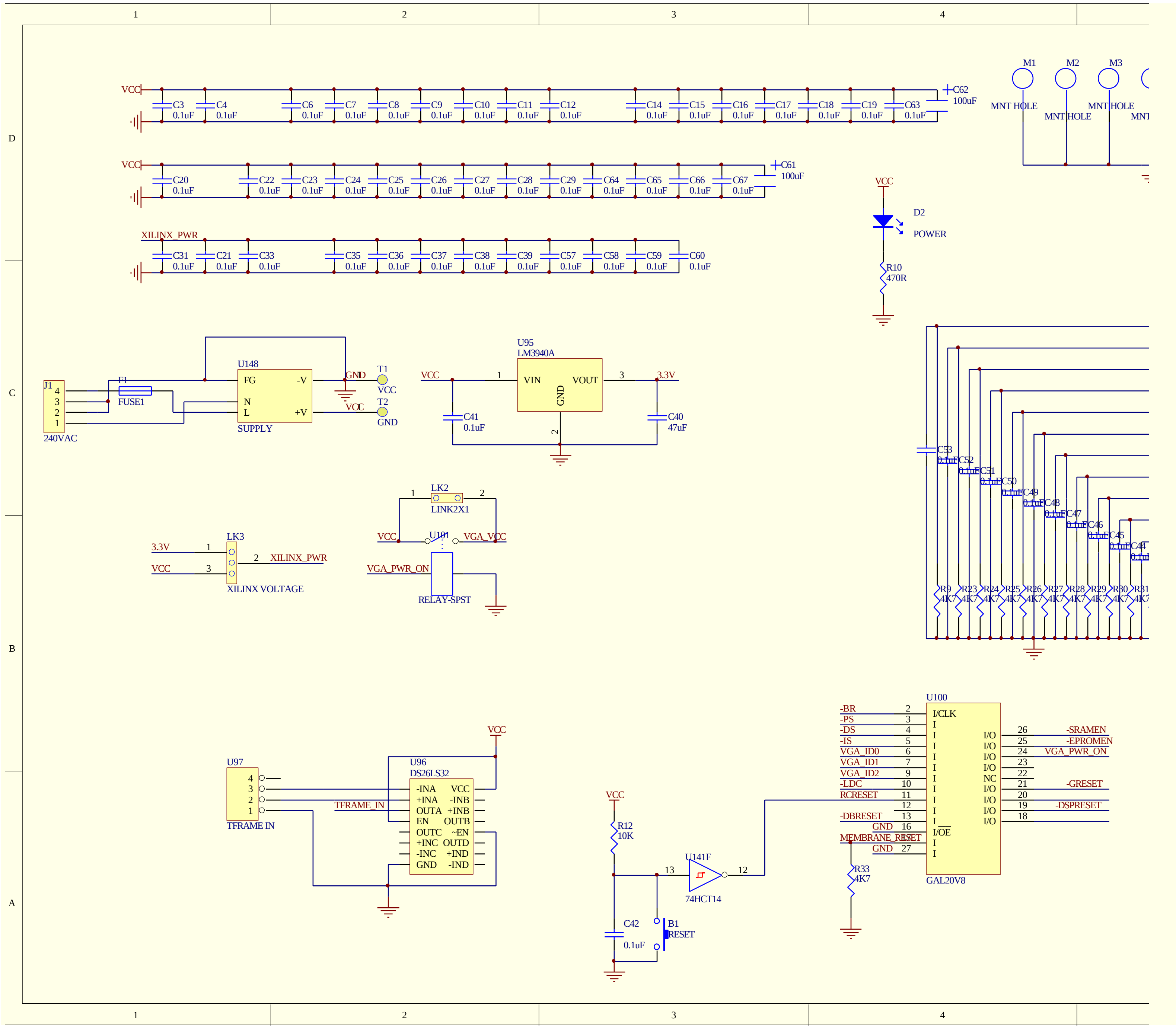
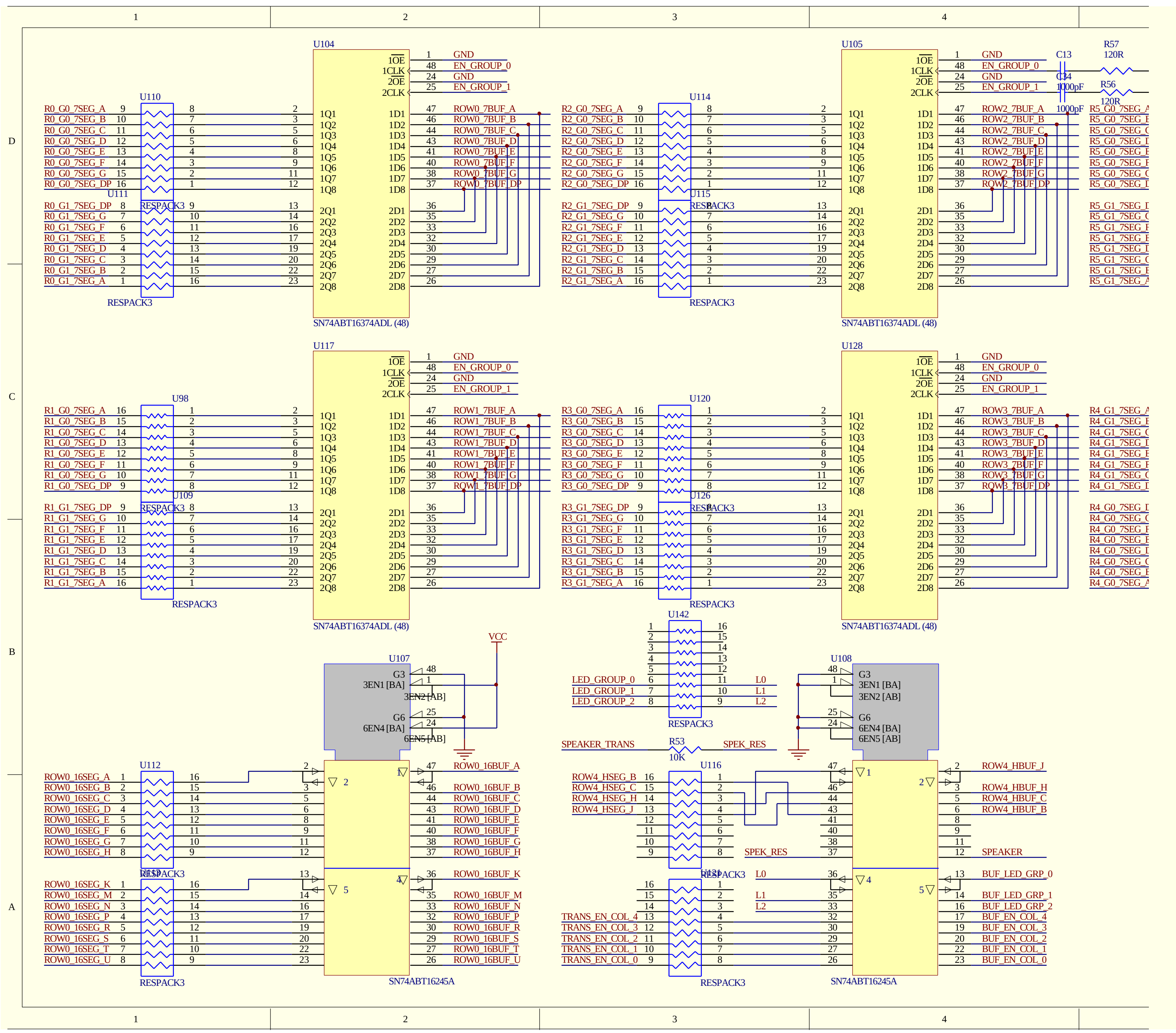
R5_G1_7SEG_DP
R5_G1_7SEG_D
SA03-11



VCC
C3 0.1uF
C4 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C11 0.1uF
C12 0.1uF
C14 0.1uF
C15 0.1uF
C16 0.1uF
C17 0.1uF
C18 0.1uF
C19 0.1uF
C63 0.1uF
C62 100uF
M1
M2
M3
MNT HOLE
C20 0.1uF
C22 0.1uF
C23 0.1uF
C24 0.1uF
C25 0.1uF
C26 0.1uF
C27 0.1uF
C28 0.1uF
C29 0.1uF
C64 0.1uF
C65 0.1uF
C66 0.1uF
C67 0.1uF
C61 100uF
D2
POWER
R10 470R
XILINX_PWR
C31 0.1uF
C21 0.1uF
C33 0.1uF
C35 0.1uF
C36 0.1uF
C37 0.1uF
C38 0.1uF
C39 0.1uF
C57 0.1uF
C58 0.1uF
C59 0.1uF
C60 0.1uF
J1
240VAC
F1
FUSE1
U148
FG
-V
N
L
+V
SUPPLY
GND
T1
T2
U95
LM3940A
VIN
VOUT
3.3V
C41 0.1uF
C40 47uF
LK2
LINK2X1
U101
VGA_VCC
VGA_PWR_ON
RELAY-SPST
LK3
XILINX VOLTAGE
C53
C52
C51
C50
C49
C48
C47
C46
C45
C44
R9
R23
R24
R25
R26
R27
R28
R29
R30
R31
4K7
U100
GAL20V8
I/CLK
I/O
NC
I/OE
-BR
-PS
-DS
-IS
VGA_ID0
VGA_ID1
VGA_ID2
-LDC
RCRESET
-DBRESET
MEMBRANE_RESET
-SRAMEN
-EPROMEN
-GRESET
-DSPRESET
U97
TFRAME IN
U96
DS26LS32
-INA
+INA
OUTA
EN
OUTC
+INC
-INC
-INB
+INB
OUTB
~EN
OUTD
+IND
-IND
TFRAME_IN
R12 10K
U141F
74HCT14
C42 0.1uF
B1
RESET
R33 4K7


1
2
3
4
D
C
B
A
U104
U105
U117
U128
U107
U108
U110
U111
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U115
U98
U109
U120
U126
U112
U113
U116
U131
U142
R57
120R
R56
120R
C13
C14
1000pF
1000pF
R53
10K
VCC
SN74ABT16374ADL (48)
SN74ABT16245A
RESPACK3
1OE
1CLK
2OE
2CLK
1Q1
1Q2
1Q3
1Q4
1Q5
1Q6
1Q7
1Q8
2Q1
2Q2
2Q3
2Q4
2Q5
2Q6
2Q7
2Q8
1D1
1D2
1D3
1D4
1D5
1D6
1D7
1D8
2D1
2D2
2D3
2D4
2D5
2D6
2D7
2D8
G3
3EN1 [BA]
3EN2 [AB]
G6
6EN4 [BA]
6EN5 [AB]
GND
EN_GROUP_0
EN_GROUP_1
R0_G0_7SEG_A
R0_G0_7SEG_B
R0_G0_7SEG_C
R0_G0_7SEG_D
R0_G0_7SEG_E
R0_G0_7SEG_F
R0_G0_7SEG_G
R0_G0_7SEG_DP
R0_G1_7SEG_DP
R0_G1_7SEG_G
R0_G1_7SEG_F
R0_G1_7SEG_E
R0_G1_7SEG_D
R0_G1_7SEG_C
R0_G1_7SEG_B
R0_G1_7SEG_A
ROW0_7BUF_A
ROW0_7BUF_B
ROW0_7BUF_C
ROW0_7BUF_D
ROW0_7BUF_E
ROW0_7BUF_F
ROW0_7BUF_G
ROW0_7BUF_DP
R2_G0_7SEG_A
R2_G0_7SEG_B
R2_G0_7SEG_C
R2_G0_7SEG_D
R2_G0_7SEG_E
R2_G0_7SEG_F
R2_G0_7SEG_G
R2_G0_7SEG_DP
R2_G1_7SEG_DP
R2_G1_7SEG_G
R2_G1_7SEG_F
R2_G1_7SEG_E
R2_G1_7SEG_D
R2_G1_7SEG_C
R2_G1_7SEG_B
R2_G1_7SEG_A
ROW2_7BUF_A
ROW2_7BUF_B
ROW2_7BUF_C
ROW2_7BUF_D
ROW2_7BUF_E
ROW2_7BUF_F
ROW2_7BUF_G
ROW2_7BUF_DP
R1_G0_7SEG_A
R1_G0_7SEG_B
R1_G0_7SEG_C
R1_G0_7SEG_D
R1_G0_7SEG_E
R1_G0_7SEG_F
R1_G0_7SEG_G
R1_G0_7SEG_DP
R1_G1_7SEG_DP
R1_G1_7SEG_G
R1_G1_7SEG_F
R1_G1_7SEG_E
R1_G1_7SEG_D
R1_G1_7SEG_C
R1_G1_7SEG_B
R1_G1_7SEG_A
ROW1_7BUF_A
ROW1_7BUF_B
ROW1_7BUF_C
ROW1_7BUF_D
ROW1_7BUF_E
ROW1_7BUF_F
ROW1_7BUF_G
ROW1_7BUF_DP
R3_G0_7SEG_A
R3_G0_7SEG_B
R3_G0_7SEG_C
R3_G0_7SEG_D
R3_G0_7SEG_E
R3_G0_7SEG_F
R3_G0_7SEG_G
R3_G0_7SEG_DP
R3_G1_7SEG_DP
R3_G1_7SEG_G
R3_G1_7SEG_F
R3_G1_7SEG_E
R3_G1_7SEG_D
R3_G1_7SEG_C
R3_G1_7SEG_B
R3_G1_7SEG_A
ROW3_7BUF_A
ROW3_7BUF_B
ROW3_7BUF_C
ROW3_7BUF_D
ROW3_7BUF_E
ROW3_7BUF_F
ROW3_7BUF_G
ROW3_7BUF_DP
ROW0_16SEG_A
ROW0_16SEG_B
ROW0_16SEG_C
ROW0_16SEG_D
ROW0_16SEG_E
ROW0_16SEG_F
ROW0_16SEG_G
ROW0_16SEG_H
ROW0_16SEG_K
ROW0_16SEG_M
ROW0_16SEG_N
ROW0_16SEG_P
ROW0_16SEG_R
ROW0_16SEG_S
ROW0_16SEG_T
ROW0_16SEG_U
ROW0_16BUF_A
ROW0_16BUF_B
ROW0_16BUF_C
ROW0_16BUF_D
ROW0_16BUF_E
ROW0_16BUF_F
ROW0_16BUF_G
ROW0_16BUF_H
ROW0_16BUF_K
ROW0_16BUF_M
ROW0_16BUF_N
ROW0_16BUF_P
ROW0_16BUF_R
ROW0_16BUF_S
ROW0_16BUF_T
ROW0_16BUF_U
LED_GROUP_0
LED_GROUP_1
LED_GROUP_2
L0
L1
L2
SPEAKER_TRANS
SPEK_RES
SPEAKER
ROW4_HSEG_B
ROW4_HSEG_C
ROW4_HSEG_H
ROW4_HSEG_J
ROW4_HBUF_J
ROW4_HBUF_H
ROW4_HBUF_C
ROW4_HBUF_B
TRANS_EN_COL_4
TRANS_EN_COL_3
TRANS_EN_COL_2
TRANS_EN_COL_1
TRANS_EN_COL_0
BUF_LED_GRP_0
BUF_LED_GRP_1
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BUF_EN_COL_4
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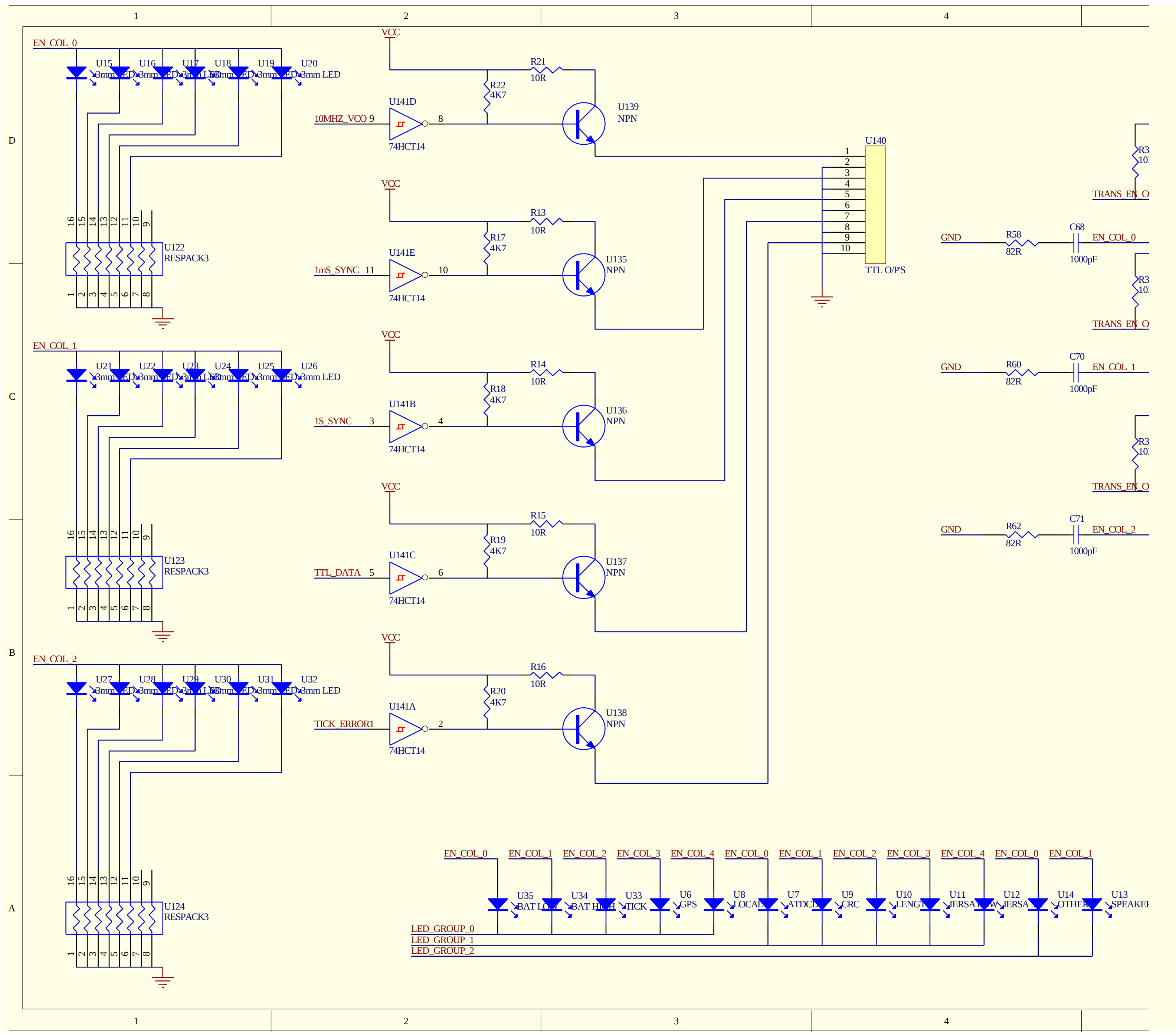
BUF_EN_COL_0



EN_COL_0
EN_COL_1
EN_COL_2
U15 U16 U17 U18 U19 U20 3mm LED
U21 U22 U23 U24 U25 U26 3mm LED
U27 U28 U29 U30 U31 U32 3mm LED
U122 RESPACK3
U123 RESPACK3
U124 RESPACK3
VCC
R21 10R
R22 4K7
U141D 74HCT14
10MHZ_VCO
U139 NPN
R13 10R
R17 4K7
U141E 74HCT14
1mS_SYNC
U135 NPN
R14 10R
R18 4K7
U141B 74HCT14
1S_SYNC
U136 NPN
R15 10R
R19 4K7
U141C 74HCT14
TTL_DATA
U137 NPN
R16 10R
R20 4K7
U141A 74HCT14
TICK_ERROR
U138 NPN
U140
TTL O/P'S
GND
R58 82R
C68 1000pF
R60 82R
C70 1000pF
R62 82R
C71 1000pF
TRANS_EN_C
U35 BAT LOW
U34 BAT HIGH
U33 TICK
U6 GPS
U8 LOCAL
U7 ATDCL
U9 CRC
U10 LENGT
U11
U12
U14 OTHER
U13 SPEAKEI
EN_COL_3
EN_COL_4
LED_GROUP_0
LED_GROUP_1
LED_GROUP_2