Australia Telescope National Facility

AUSTRALIA TELESCOPE DISTRIBUTED CLOCK DISPLAY

 USERS MANUAL

Paul Hales 5th April 2001
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1 Introduction

The ATDCD takes as input, a 1MHz pulse width modulated timeframe signal from the ATDC. This signal is demodulated and decoded to recover the raw timeframe data. The relevant time information is extracted from this data and displayed on segmented displays. The ATDCD is a portable device housed in an aesthetically pleasing enclosure that offers water and ingress protection as well as EMC shielding.

The unit has been constructed such that it can be used as a handheld device, used on a desk with a mini tripod support, or mounted on a wall via the supplied wall brackets or a swivel joint.

This document gives information on how to use the ATDCD, explains its functionality and describes its construction.
2 Input/Output Connectors

![Figure 1: Front view of I/O panel](image)

![Figure 2: Back view of I/O panel](image)

2.1 Inputs

2.1.1 Time Frame

Either a D9 or RJ-45 connector can be used to connect the Time Frame signal to the ATDCD. The pin-outs for each connector are given in the following table:

<table>
<thead>
<tr>
<th></th>
<th>D9</th>
<th>RJ-45</th>
</tr>
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<tbody>
<tr>
<td>+Signal</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>-Signal</td>
<td>6</td>
<td>5</td>
</tr>
<tr>
<td>GND</td>
<td>5</td>
<td>3</td>
</tr>
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</table>
2.1.2 Power

Power is supplied to the ATDCD via a 240V mains lead. This mains voltage is internally converted to the required 5VDC supply needed to power the main circuit board.

2.2 Outputs

2.2.1 Time Frame – D9 or RJ-45

The Time Frame is output from the unit via both a D9 and a RJ-45 connector. If the unit is the last in the line, then an external terminator is required on one of the output connectors to terminate the line. A terminator housed in a yellow D9 shell is supplied with the unit.

2.2.2 VCO - 50Ω BNC

An onboard voltage controlled oscillator is used as part of the PLL circuit. The clock signal from this oscillator is output via this BNC connector. When the PLL is locked, the VCO output will be in sync with the input 1MHz Time Frame. Two varieties of oscillators were used in the production of the ATDCD. One has a frequency of 50MHz, the other 10MHz.

2.2.3 1ms Sync - 50Ω BNC

The 1MHz PWM Time Frame encodes two synchronisation signals. One of these occurs every 1ms. When the PLL circuit has locked onto the input Time Frame, the 1ms-synchronisation signal will be output on this BNC connector as a 500µs pulse.

2.2.4 1S Sync - 50Ω BNC

The other synchronisation signal encoded in the 1MHz Time Frame, is the 1s sync. When the PLL circuit has locked onto the input Time Frame, The 1s synchronisation signal will be output on the BNC connector as a 1ms pulse.
2.2.5 Raw Data - 50Ω BNC

As the data is demodulated from the Time Frame, it is output again as raw data to this BNC connector.

2.2.6 Tick Phase - 50Ω BNC

If a tick phase error occurs (see section), a 1ms pulse will be output on this BNC connector.

2.2.7 Video – D15

This connector is currently unused. It allows for future expansion of the ATDCD to include a video controller board that will output the ATCD information to a VGA monitor via this connector.
3 Functionality

3.1 The Tick Phase Display Window

The Tick Phase display window can display three different pieces of information. Primarily it is used (as the name suggests) to display the current value of the Tick Phase in microseconds. When in this mode, the display also serves as a warning device to alert users that a jump of greater than 100 microseconds has occurred in the Tick Phase, refer to section 3.4 Error Monitoring for more information on this feature.

The window can also be used to display the current value of the 64-bit Binary Atomic Time (BAT) register. As there are only ten characters available for displaying information in this window, and there are 64 bits in the BAT, the full BAT cannot be displayed at one time. To overcome this problem, the 64 bit BAT is displayed by either the 24 most significant bits or the 40 least significant bits.

The three buttons located below window give control over what information is displayed. These buttons are labelled BAT LOW, BAT HIGH and TICK PHASE.

The BAT LOW button displays the 40 least significant bits of the BAT

The BAT HIGH button displays the 24 most significant bits of the BAT

The TICK PHASE button displays the current Tick Phase in microseconds.

You can determine what is being displayed in the window by looking at which button is currently highlighted by is respective LED indicator.

3.2 Brightness Control

The are two modes of control for varying the brightness of the ATDCD, these are Manual or Automatic. The user can toggle between these two modes by simultaneously pressing the brightness down and brightness up buttons. It is often easier to perform this operation by the following method:
1. Press and hold the brightness down button with the index finger of the left hand
2. Immediately after, press the brightness up button with the index finger of the right hand
3. Release both fingers at the same time.

3.2.1 Manual Brightness Control

When in Manual mode, the brightness can be varied via the up/down brightness control buttons located at the lower left of the control panel. There are five levels of brightness to select from.

3.2.2 Automatic Brightness Control

When in Automatic mode, the brightness is controlled by a Light Dependant Resistor, which is located in the upper left-hand corner of the control panel. Again there are five discrete levels of brightness, the level selected will depend on the brightness of the ambient lighting. The brightness level will become brighter or duller in synchronisation with the ambient lighting.

Note:
In the transitional periods between one level and the next, the brightness may be seen to change back and forth between two levels until the ambient light moves out of the transitional range. This is normal and does not mean the unit is malfunctioning.

3.3 Audio

The Audible one second beep can be toggled on and off via the SPEAKER button. Once toggled on, a short tone will be heard each time the 1s synchronisation signal is received. If the time frame is disconnected from the ATDCD, the audible tone will cease.

The volume of the audible tone can be controlled via the VOLUME UP and VOLUME DOWN buttons. There are five discrete levels of volume.
3.4 Error Monitoring

3.4.1 Error LED’S

The ATDCD has the ability to detect and log time frame errors. These include:

- ⊗ GPS TICK LOST – The GPS tick signal is not detected at the ATDC.
- LOCAL PLL UNLOCKED – The local VCO PLL is out of lock.
- ⊗ ATDC PLL UNLOCKED – The ATDC PLL is out of lock.
- CRC FRAME ERROR – A bit error has occurred in the timeframe.
- LENGTH FRAME ERROR – A time frame length underrun or overrun has occurred.
- ⊗ IERSA TABLE LOW – The ATDC IERSA table is low.
- ⊗ IERSA TABLE EMPTY – The ATDC IERSA table is empty.
- ⊗ OTHER ERROR – As yet undefined.

⊗ Error logging not implemented in the as of 5/4/2001

Once an error is logged, it will remain logged until an Error Clear function is performed. This is done by pressing and holding the ERROR CLEAR button for two seconds. A beep will be heard when the button is first pressed, and another after two seconds when the errors are cleared.

Whenever the power is applied to the unit, the unit undergoes a System Reset, or the time frame is disconnected, the following errors will be logged:

- ATDCD PLL ERROR
- CRC FRAME ERROR
- LENGTH FRAME ERROR

An Error Clear will have to be performed before correct monitoring can begin.

3.4.2 Tick Phase Error

If a tick phase jump of greater than ±100µs is detected in one second, then a tick phase error is logged. The tick phase display window flashing at a frequency of 1Hz indicates this error. This error can be cleared by performing and Error Clear function as described above.
3.5 System Reset

If the ATDCD gets into an invalid state, a System Reset may need to be performed. To do this, press and hold the SYSTEM RESET button for two seconds. Remember to perform an Error Clear after a System Reset.

All user settings are stored in non-volatile RAM. This means that the last setting will be restored upon power up or system reset. The following settings will be restored:

- Automatic or Manual brightness control.
- Brightness level if in manual mode
- Speaker on or off
- Speaker volume
- Tick phase display – BAT High/BAT Low/Tick Phase.

3.6 Lamp Test

To test the state of the LED displays, press and hold the LAMP TEST button. All LED’s in the ATDCD will be illuminated as long as this button is pressed. To limit current drain, the LED’s are illuminated at the lowest brightness level. For this reason it is best to perform this test in a room with low ambient lighting. This is especially true for the green and orange ATDCD’s.
4 Construction

4.1 Enclosure construction

The requirements for the enclosure were that it protected the electronics from the environment (dust and water), provided a shield against Radio Frequency Interference RFI and was aesthetically pleasing.

The box used is an Aluplan from Bopla. It is constructed from four pieces of aluminium extrusion, a 3mm rectangular aluminium plate for the base and a 3mm front panel.

To disassemble the housing use the following steps:

1. Remove the power.
2. Remove the four corner covers with a flat blade screwdriver.
3. Working on the right hand flat panel (opposite to connector end), loosen the four screws going into the rounded sides, but do completely remove them.

4. Working on the connector end, loosen and remove the four screws going into the rounded sides.

5. Pull the connector side away from the rest of the enclosure, but be careful not to damage the wiring coming away from the connectors.

6. Pull the rounded sides out to the limit of the loosened screws from step 3.

7. Pull the flat connectorless end and the rounded sides to the right as one unit.
8. Turn the ATDCD over and unscrew the 7 mounting screws and remove the bottom plate.

9. Unclip front panel ribbon cable.

10. Disconnect the power cable, output ribbon cable and input time frame connector as necessary.

11. Turn the ATDCD over and lift off the front panel.

Carry out the steps in reverse order to reassemble.
4.2 Front Panel

The front panel is made up of a lamination of three layers. The first is a 1.5mm aluminium frame that provides structural support for the panel. The cut-outs and holes in this frame have been milled to shape so that the frame sits around the outside of the segment displays.

Next a 100 OPI blackened copper mesh is wrapped around the frame and held in place with conductive aluminium tape. This mesh provides electromagnetic shielding over the open area of the frame.

The third layer is comprised of a graphical and electrical membrane that incorporates the colour filtering, graphics, further shielding and touch switches. The membrane is joined to the frame and mesh by an adhesive on the bottom of the membrane.

The membranes used were supplied by Sun Industries.
4.3 Circuit Schematics