InP MMIC's and High Speed Samplers (SEP) – Wafer Test Results

Five HBT wafers were delivered from TRW. Two of the wafers were fabricated using TRW's new low base resistance process, and the remaining three with the higher base resistance process. On-wafer tests of the high speed digital and multiplier circuits on the wafers have now been completed. A summary of results is as follows:

1) Digitiser/Demultiplexer. The 3 level digitiser with integrated demultiplexer shows correct operation to at least 10 GHz clock rate. Of 229 circuits measured 217 are functional giving a 94% yield

2) Digitiser. The 3 level digitiser with no demultiplexer shows correct operation to at least 10 GHz. Of 62 circuits measured 58 are functional.

3) Photonic I/O Digitiser. The photonic I/O digitiser shows correct operation to at least 4 GHz clock rate. Testing at higher clock rates is currently limited by the lack of a > 4GHz modulated optical source. Of 20 circuits measued 18 are functional.

4) Multiplier. The multiplier circuit shows a 3dB multiplication bandwidth of 15.5 GHz. Of 84 circuits measured on the high base resistance wafers 83 are functional. The remaining 56 circuits on the low base resistance wafers while nominally functional show a tendency to oscillate at ~ 31 GHz. Experiments indicate this is due to a coupling from output to the inverting input which we hope to cure with an RF short when packaged.

Given the high yields we have decided not to measure each of the remaining circuits on the wafers but a selective spot testing has been done. Based on the previous yield estimates expected number of yielded circuits prior to dicing is

Digitiser/Demultiplexer	360 circuits
Digitiser	258 circuits
Photonic Digitiser	180 circuits
Multiplier	130 circuits

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