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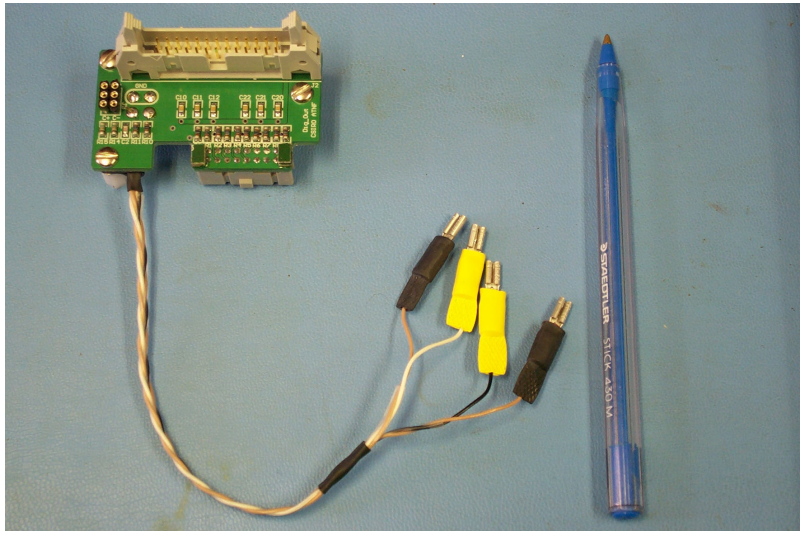
DIG_OUT
Digital Output TTL – LVDS Converter



DESIGN NOTES

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1. Introduction:

The Digital Output TTL – LVDS Converter was primarily designed to aid in extending the capabilities of the LBA DAS. The Dig_Out board converts the Digital Output Signal (TTL) on the Back of the LBA DAS to LVDS pairs, which are suitable for extended transmission and further processing. As well as this the Dig_Out incorporates the 32Mhz Clock reference and SYNC signals from the LBA DAS on its output connecter to aid in signal processing at the receiving Device.

2. Connection Information

J1 – Digital Input Port

Pin	Signal	Signal Type	Comment
1	D0	TTL	Two's Complement data
2	D1	TTL	"
3	D2	TTL	"
4	D3	TTL	"
5	D4	TTL	"
6	D5	TTL	"
7	D6	TTL	"
8	D7	TTL	"
9	D8	TTL	"
10	D9	TTL	"
11	GND	GROUND	Signal Ground
12	GND	GROUND	"
13	GND	GROUND	"
14	GND	GROUND	"
15	GND	GROUND	"
16	GND	GROUND	"

J2 – LVDS Output Port

Pin	Signal	Signal Type	Comment
1	D0+	LVDS	Differential Digital data
2	D0-	LVDS	"
3	D1+	LVDS	"
4	D1-	LVDS	"
5	D2+	LVDS	"
6	D2-	LVDS	"
7	D3+	LVDS	"
8	D3-	LVDS	"
9	D4+	LVDS	"
10	D4-	LVDS	"
11	D5+	LVDS	"
12	D5-	LVDS	"
13	GND	GROUND	Signal Ground Input
14	LV3	POWER	3.3V Power Input
15	D6+	LVDS	Differential Digital data
16	D6-	LVDS	"
17	D7+	LVDS	"
18	D7-	LVDS	"
19	D8+	LVDS	"
20	D8-	LVDS	"
21	D9+	LVDS	"
22	D9-	LVDS	"
23	DSYNC+	LVDS	"
24	DSYNC-	LVDS	"
25	DCLK+	LVDS	"
26	DCLK-	LVDS	"

J3 – LVDS Test Port

Pin	Signal	Signal Type	Comment
1	TSYNC+	LVDS	Note Termination
2	TSYNC-	LVDS	"
3	GND	GROUND	Signal Ground
4	GND	GROUND	"
5	T32MHz+	LVDS	Note Termination
6	T32MHz-	LVDS	"

3. Brief Explanation of Design:

The design specifications for the Digital Output board were given as:

1. Convert the TTL digital output data from the LBA DAS to LVDS signals so that it can be transmitted over a distance for further processing.
2. Eliminate reflections and signal degradation through the use of line termination.
3. Include test points for monitoring the Clock and Sync Signal.
4. Derive Power from the Receiving Device.

These were considered and designed into the final product in the following manner:

Convert the TTL digital output data from the LBA DAS to LVDS signals so that it can be transmitted over a distance for further processing.

Preliminary designs had already been drawn of the receiving device, namely the DAS MUX. In these designs the signal type expected was LVDS. Quantities of LVDS receivers and transmitters had already been ordered and thus the SN75LVDS389 was chosen for use on the Digital Output Board. It offered good distance transmission characteristics and was compact to fit on the board.

Eliminate reflections and signal degradation through the use of line termination.

The data and clock signals being received from the LBA DAS were considered to be signals that had traveled on a 100ohm transmission line. Therefore to avoid reflectance, each signal was terminated with a 100ohm resistor before entering the LVDS Driver. The Output of the Dig_Out board is un-terminated on the board, however it is anticipated that termination resistors will be included on the receiving device.

Include test points for monitoring the Clock and Sync Signal.

Only 12 of the Possible 16 LVDS drivers were required for the data to be included on the output connector. Therefore four drivers were spare for use in a test port. It was decided that termination of this port on the board would make it less vulnerable to reflections and give it higher signal integrity. It was also assumed that termination of a similar style would be used on anything connected to this port. Thus two LVDS outputs were joined for each signal to eliminate the V/2 effect created by double termination. Signal Grounds were also included in the test port to separate signals and provide a ground point.

Derive Power from the Receiving Device.

Electrical power is obtained from Pin 13 & 14 on th board. By placing on the middle pins, the dangers of "hot plugging" are reduced. Power (+3.3V) was placed on Pin 14 as this allowed a thick track to be run to the LVDS chips.

The top layer of the Dig_Out Board is a Ground Plane and thus Pin 13 is connected there.

4. Design Background

Some concerns that were dealt with during design:

4.1.Signal Timing

There was concern that the Digital Data, Clock and Sync signal would not be in phase when they reached the D-Latch on the receiving device. Therefore a timing analysis was undertaken, that researched the Propagation Delays and Signals Skews.

4.1.1. Summary of Results

A reference point (Analog Sampler - Clock synchronizer) was chosen and used to calculate the following propagation delays from there to the D latch chip on the Receiving Board. Cable delay has been included.

The following Table summarises results found.

SIGNAL	**PROPOGATION DELAY**
SYNC	7.13ns – 14.3ns
32MHz Clock	9ns – 10.9ns
DATA	15.7ns – 17.6ns

4.1.2. Timing Comparison

The specifications for the D latch SN74LVTH574 on the receiving board are:
t(setup) = 2.0ns
t(hold) = 0.3ns

From the Chart "Setup & Hold Times" we can see that for our system in worst case scenario:

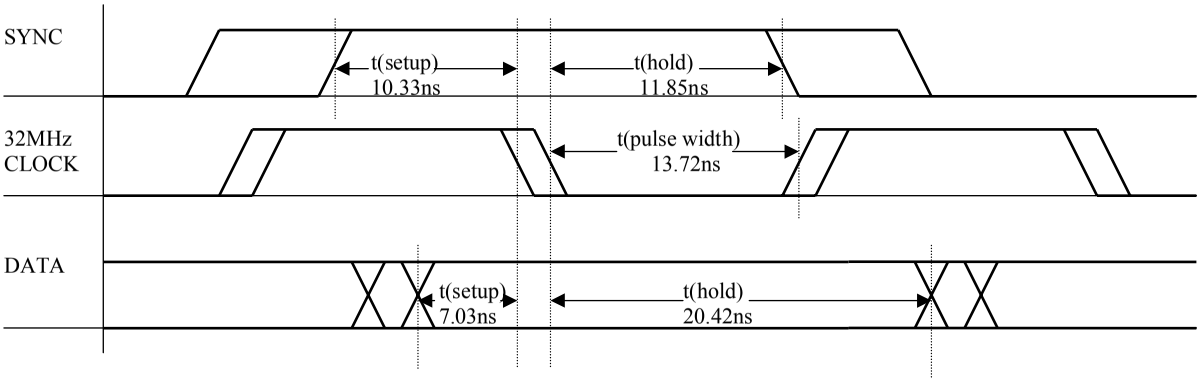
Data Signal:
t(setup) = 7.03ns
t(hold) = 20.42ns

Sync Signal:
t(setup) = 10.33ns
t(hold) = 11.85ns

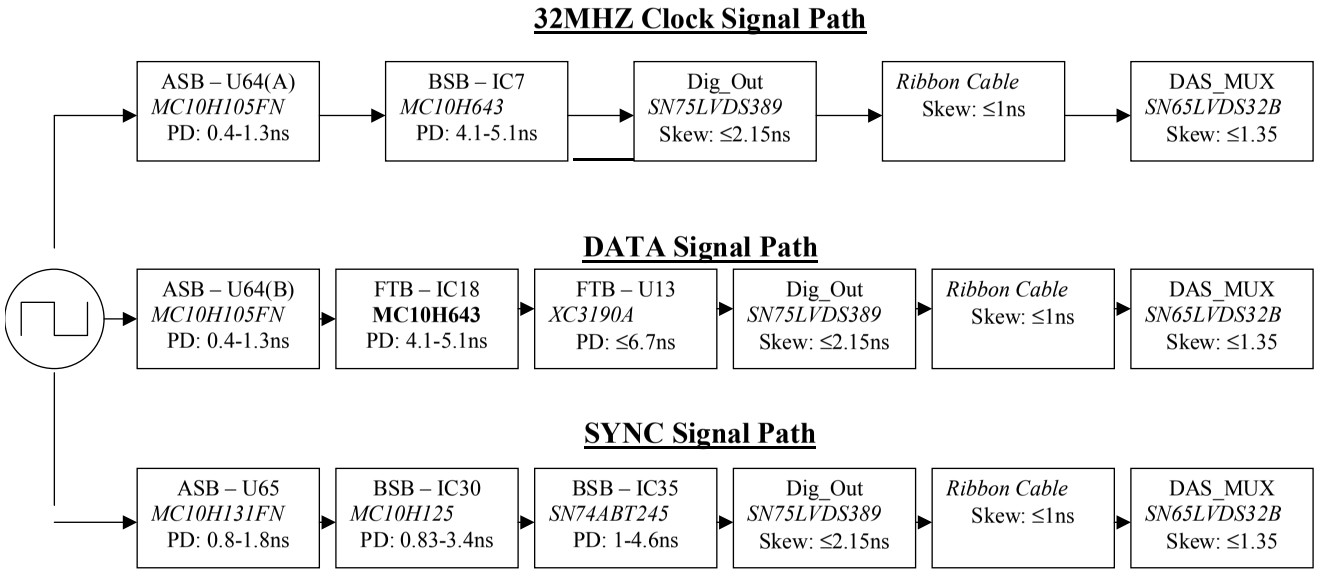
4.1.3. Timing Conclusion

It can clearly be seen that both the Data and Sync signals satisfy the timing requirements of the receiving D latch SN74LVTH574 chip. Since this was a "Worst Case Scenario" analysis it is safe to assume that the Data and Sync signals will satisfy the requirements of the D latch in all situations.

4.1.4. Chart A – Setup & Hold Times



4.1.5. DAS Signal Paths



4.1.6. Explanation of Values in Block Diagram

The times in the Block Diagram were calculated in the following manner.

MC10H105FN, MC10H643, MC10H131FN, MC10H125, SN74ABT245:

These are the minimum to maximum propagation delay times for these chips at the highest rated temperature. This gives us a view of the worst case scenario.

XC3190A:

The Xilinx chip is configured to operate in **fast** mode (not slew rate limited), speed grade –2. Therefore the maximum value for the fast Global and Alternate Clock distribution Buffer Delay is added to the fast propagation delay of the output to pad. The "≤" indicates that the value shown is a worst case value.

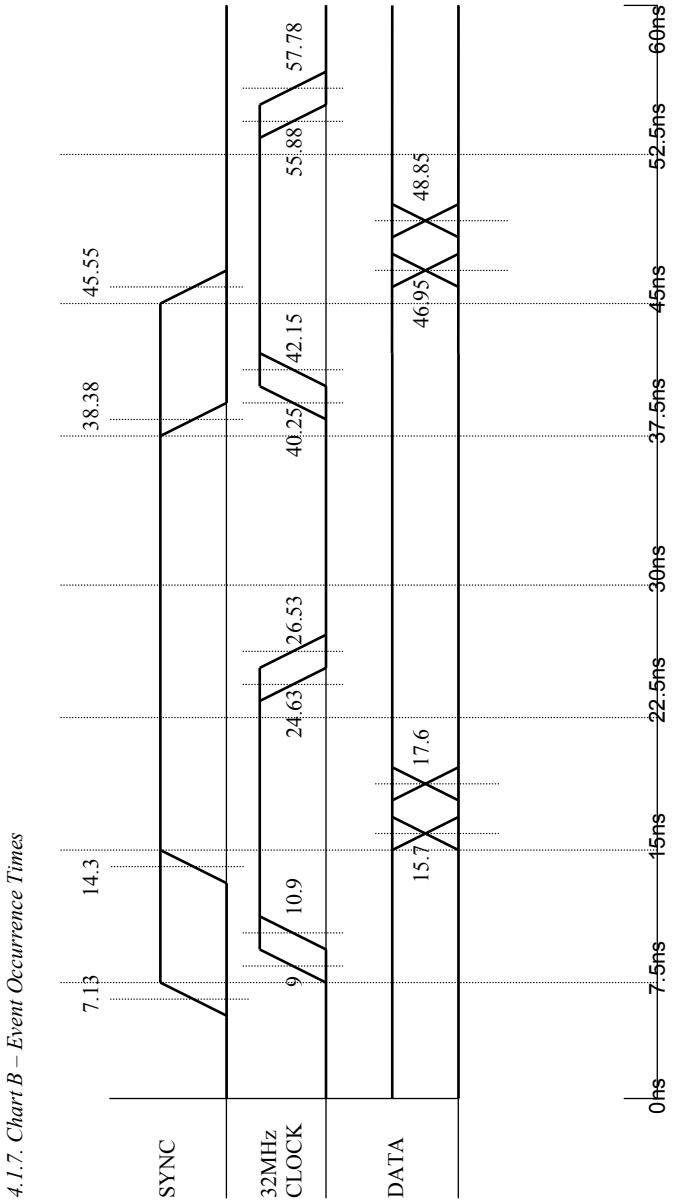
SN75LVDS389, SN65LVDS32B:

Since these chips are common to all signals only the signal skew through them need be considered. The value shown is calculated by adding the maximum value of Pulse Skew, Output Skew and Part to Part Skew. The "≤" indicates that the value shown is a worst case value.

RIBBON CABLE:

100R twisted pair transmission line has a signal skew of up to 0.5ns per meter. The figure shown is based on a two meter cable.

4.1.7. Chart B – Event Occurrence Times



4.2. Load Lines

Within the LBA DAS, an SN74ABT245 Octal Transceiver was used in the output stage. There was concern that the ABT chip would not be able to pull down the voltage to an acceptable TTL level with the total resistance present. A load line analysis was performed and it was concluded that suitable voltage levels could be attained.

5. Hardware

Mounting
The Digital Output board is designed to be plugged directly into the Digital Output Port of the LBA DAS. The fastening ears will clamp onto the PCB to hold it secure. Plastic Spacers (13mm) are located at the three remote corners of the board to provide extra support when plugging/unplugging the output cable.

Clock input cable
A 20cm four core (two pair) twist and flat cable is used to connect the 32MHz Clock and 1pps SYNC signal to the Dig_Out Board. This is achieved by plugging the Spade connectors on the end of this cable into the respective spade terminals on the back of the LBA DAS as well as the Ground Terminals.