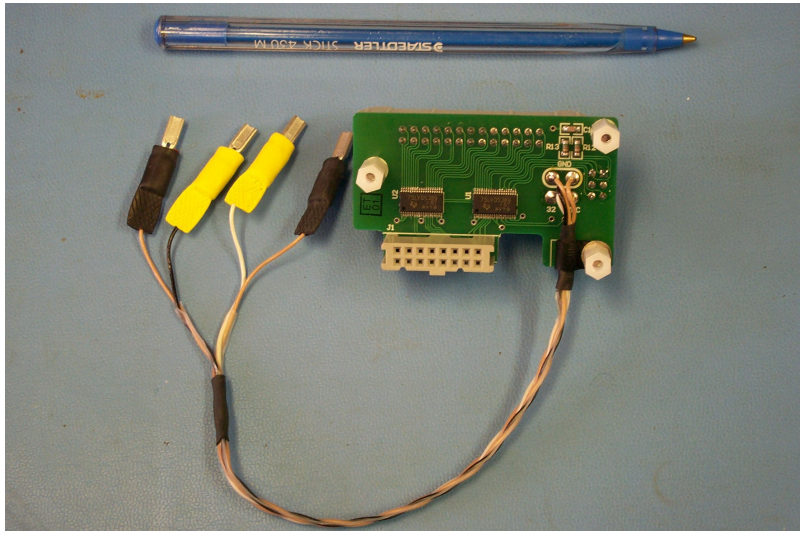
Revised 21/10/01

DIG_OUT



Prototype Testing

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Aim:

To test the validity of the Dig_Out design in performing its task and assess to what degree this has been achieved.

Equipment:

- Tektronix TDS3034 Digital Oscilloscope
- Tektronix TDS580C Digital Oscilloscope
- 3 x Tektronix FET Probes
- Dig_Out Board
- 3.3V DC Regulated Power Supply
- Test Termination resistor (100R)
- Test Termination Plug

Procedure:

1. Visually inspect Dig_Out board looking for:
   - Solder Faults
   - Incorrect component placement or orientation
   - Correct cable colour coding.
2. Trigger Oscilloscope on 32MHz clock signal
3. Plug Dig_Out Board in Digital Out Port on back of DAS
4. Measure the Jitter on all Data lines of the Digital Out Port. This is done by measuring the amount of time from the vertical middle of the back edge of the cross (or eye) to the vertical middle of the front edge of the cross.
5. Connect Power to Dig_Out Board (3.3V).
6. Plug Dig_Out termination resistor (100ohm) into DO+- on Dig_Out board.
7. Connect the FET Probes to either side of the termination resistor ensuring each probe is grounded nearby on the same ground plane. Check the minimum signal Period. (Should be approx 31.25ns)
8. Now measure the Jitter of each individual LVDS line. This is done by measuring the amount of time from the vertical middle of the back edge of the cross to the vertical middle of the front edge of the cross. According to TI, the Jitter should be < 5% of the total period.
9. For a completely accurate measure of Jitter, minus the Jitter of the Digital Out port (step 2) from the Jitter of the Dig_Out board. Should be < 4%.
10. Measure the Common Mode Voltage. This is the voltage at which the logic changeover occurs. Typical voltage offset is 1.2V (ref. TI) relative to ground with a signal swing from 247mV to 454mV. There can be +-1V of Ground noise before the signal reaches the receiver chip.
11. Check Logic High – Logic Low > 100mV. This is the minimum sensitivity that the receiver will have. If it is less than 100mV there is a problem.
12. Repeat steps 9 to 11 for the Differential signal.
13. Measure the time lag between the 32Mhz clock on the board and the Data

14. Repeat steps 7 to 12 for the rest of the Data lines

Results:

The following table summarises the results found from the above tests. These results are discussed in the discussion.

Signal	Period (ns)	Jitter (ns)	TTL Jiter (ns)	Accurate Jitter (ns)	Jitter (%)	Comm Mode (V)	Peak-Peak (mV)	Data/Clk lag (ns)	Rise Time (ps)
D0+	32	10	9	1	3.13%	1.2	500		100
D0-	32	12.2	9	3.2	10.00%	1.2	450		100
D0	32	8.5	9	0.5	1.56%	0	300	5.8	150
D1+	32	13	9	4	12.50%	1.2	450		100
D1-	32	14	9	5	15.63%	1.2	500		70
D1	32	11	9	2	6.25%	0	600	6	200
D2+	32	12	10	2	6.25%	1.2	500		100
D2-	32	12	10	2	6.25%	1.2	600		100
D2	32	10.5	10	0.5	1.56%	0	600	6	100
D3+	32	14	10	4	12.50%	1.2	500		80
D3-	32	14	10	4	12.50%	1.2	500		80
D3	32	11	10	1	3.13%	0	600	5	80
D4+	32	13	10	3	9.38%	1.2	600		100
D4-	32	14	10	4	12.50%	1.2	600		100
D4	32	10.5	10	0.5	1.56%	0	600	6.5	80
D5+	32	14	9	5	15.63%	1.2	600		70
D5-	32	13.6	9	4.6	14.38%	1.2	600		80
D5	32	11	9	2	6.25%	0	600	7	80
D6+	32	13.5	9	4.5	14.06%	1.2	500		100
D6-	32	14	9	5	15.63%	1.2	500		70
D6	32	10	9	1	3.13%	0	600	6.5	100
D7+	32	14	9	5	15.63%	1.2	600		100
D7-	32	14	9	5	15.63%	1.2	500		100
D7	32	14	9	5	15.63%	0	600	8	200
D8+	32	11.5	9	2.5	7.81%	1.2	500		100
D8-	32	14	9	5	15.63%	1.2	500		100
D8	32	12	9	3	9.38%	0	600	6	150
D9+	32	12	9	3	9.38%	1.2	500		100
D9-	32	14	9	5	15.63%	1.2	500		100
D9	32	12	9	3	9.38%	0	600	6.5	100
SYNC+	32	0			0	1.2	500		
SYNC-	32	0			0	1.2	500		
SYNC	32	0			0	0	600	-4	
CLK+	32	1			0	1.2	600		
CLK-	32	1			0	1.2	600		
CLK	32	1			0	0.1	600	0	

Discussion

Period

The data rate of the Digital Output Port is determined by one of the DAS internal clocks. This is set to 32MHz, thus the minimum signal period observed on any data should be 32.25ns. All data lines were checked and this was found to be the case most of the time. It was noticed however that occasionally "spurs" occurred in the LVDS data. Originally this was thought to be an LVDS error but upon further investigation it was seen that the spurs originated from the TTL as shown in the diagram below.

D0+ ; D0- ; D0 (Difference) ; D0 (TTL) ; 32Mhz Clock

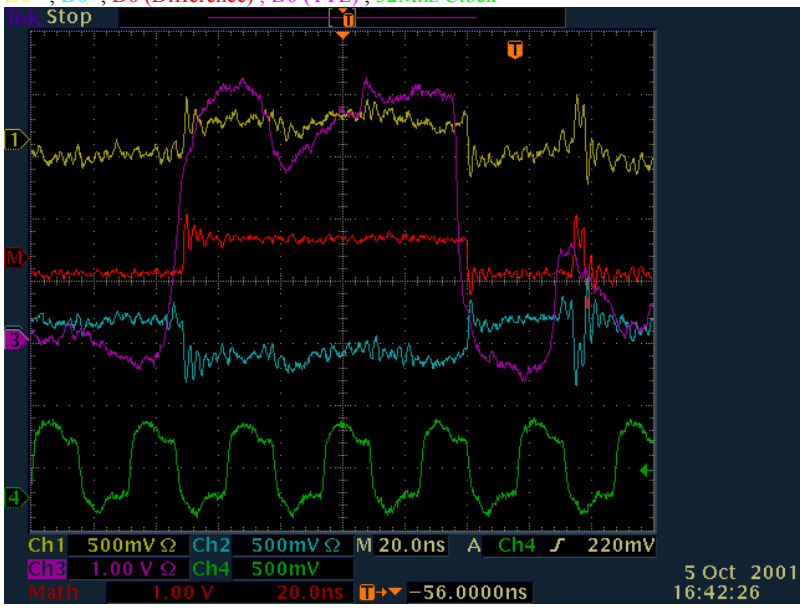

Figure 1- Mysterious Spurs

This, therefore, is a problem that is beyond the scope of this testing and will therefore not be investigated any further. However it is recommended that independent investigation be undertaken into this phenomenon before data is used.

Jitter

The Jitter in the Digital data will allow us to determine if the data will be valid when we latch it for processing. Jitter was measured for the TTL, D+, D- and D (Difference). In order to gain a result representative of a reasonable time-span, the persistence of the Oscilloscope was set to infinite and thus a waveform such as the following was produced.

TTL ; 32MHz Clock

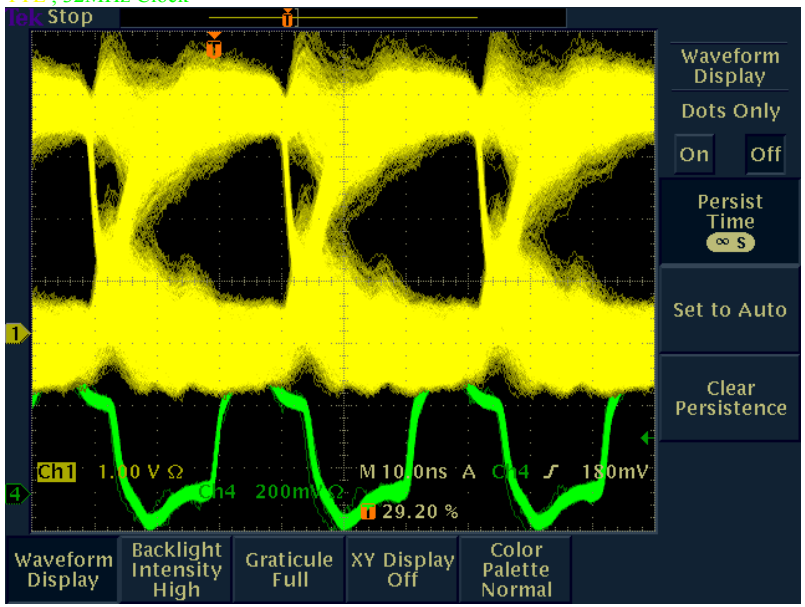

Figure 2 - Infinite Persistence on TTL signal

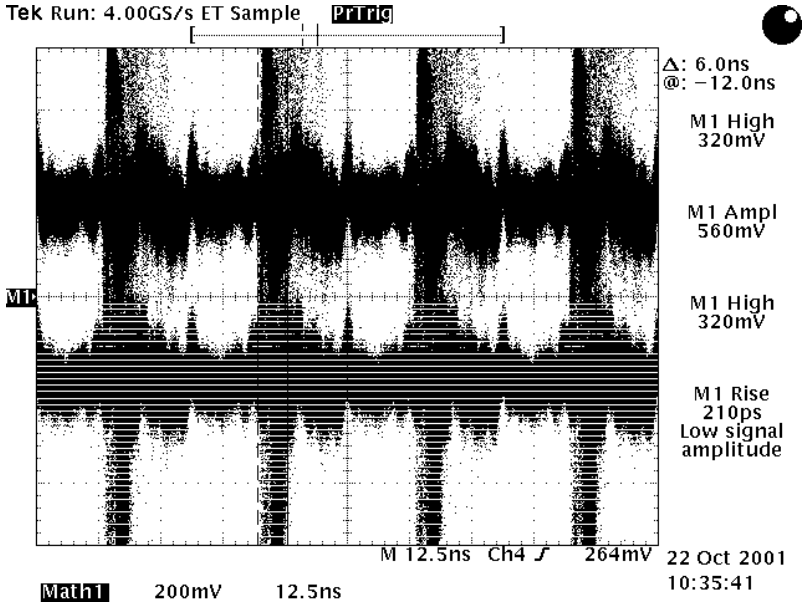

Figure 3 - Infinite Persistence on LVDS signal

It was found that the Jitter on the Digital lines alone was in the order of 9-10ns. Naturally, when measured it was found that the Jitter on the LVDS lines was equal to or higher the 9ns as a result of the TTL Jitter. The LVDS Jitter ranged from 9ns to 14ns.

Thus, in most cases, the Jitter created between the TTL in and the LVDS out is a matter of approximately 6% of the signal period.

Common Mode Voltage

As expected it was seen that the independent LVDS signals have a common mode voltage of approx 1.2V. The Difference signal had its common mode at Ground.

Peak to Peak range

In order for the LVDS receiver chip to recognize a logic change, a voltage swing of greater than 200mV needs to occur. This criteria was satisfied in on all data and clock channels.

Data/Clock Lag

As calculated in the Timing Specifications of the Dig_Out Board, the Data lags the clock in the range 4.8ns – 8.6ns. This was seen in practice in our results with the data lagging the clock in the range 5ns – 7ns.

Rise Time
The criteria specified in TI's LVDS documentation is that the Rise Time should be less than half the signal period. Our rise times meet this criteria

Noise
There was initial concern for the amount of noise present on the two logic states of the LVDS signal. It was unsure as to the origin of this noise and whether it would have any significant affect on the data quality.

The AC coupled noise on the Power rail was then compared to the noise in the waveform, and a good correlation was seen.

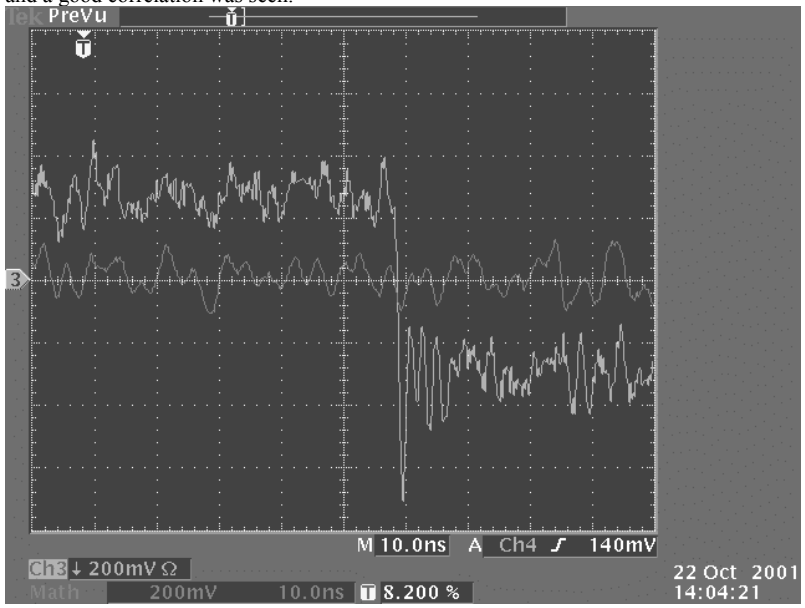

Figure 4 - AC Coupled Noise on Power compared to LVDS

The AC coupled noise was then measured for the Ground Plane and found to be of similar magnitude. The correlation with the data, however, was not so great. Therefore it was decided that some of the noise was originating from the power rails. This implies that the rest of the noise was measurement/quantisation error introduced when the probes were connected to the board.

Conclusion

The Dig_Out board met and exceeded criteria specified in the test Procedure. The Dig_out board by itself does not adversely affect the Digital Output data.