Australia Telescope National Facility

SEST INTERMEDIATE FREQUENCY (IF) SUB-SYSTEM

Paul Hales 3th April 2000

CONTENTS

1. Description

1.1 General

The SEST IF Sub-System's basic function is to filter and prepare the IF signal ready for the Samplers and to perform a Total Power Measurement on the signal. The Sub-System has two main modes of operation:

Slave Automatic Mode:
In this mode, the Block Control Computer (BCC) has full control. The BCC will set bits in the configuration register to control the bandwidth and attenuation settings. In this mode, the BCC must also tell the IF unit the current Integration time so that the front panel can display the correct power level.

If manual mode is invoked whilst in Slave Automatic mode, the bandwidth and attenuation setting can be changed by the front panel switches. Upon switching back to Automatic mode, the IF unit will return to the last configuration set by the BCC.

The choice of Automatic or Manual mode is selected either by a switch on the Manual Interface, or through setting a bit in the configuration register via the BCC

Note: In Slave Automatic Mode, the IF unit will expect two external control signals. One to set the integration time (referred to as Integration Signal), and one to switch between the internal high and low counters (Referred to as Counter Select). If these signals are not present, the power counts will be invalid and the front panel will not display the correct output power.

Master Automatic Mode:
In this mode, the attenuation level is controlled by an internal control loop within the IF unit. The external Integration Signal is ignored, and instead an internal Integration signal is generated with an integration time of five seconds. The internal control loop will adjust the variable attenuator in the IF unit, such that the nominal output of -8dBm is achieved on the output to the sampler. The Bandwidth setting can be changed by the front panel switches.

If Manual mode is invoked whilst in Master Automatic Mode, the bandwidth and attenuation levels can be altered via the front panel switches. Upon switching back to Master Automatic Mode, the bandwidth setting will remain the same as set by the front panel switches, and the attenuation level will once again be under the control of the control loop.

The choice of Automatic or Manual mode is selected either by a switch on the Manual Interface, or through setting a bit in the configuration register via the BCC.

A bit in the configuration register (set by the BCC) Determines if the IF unit is in Slave Automatic Mode or Master Automatic Mode. At start up, the system is configured for Master Mode.

Source of Counter Select Signal

The Counter Select Signal has two possible sources. One source is from the AT Event Generator, in the form of a 'Sync' signal. This signal is synchronous with the Integration Signal (also generated by the Event Generator), and therefore there is an equal integral number of low and high pulses during the integration period.

The other source of Counter Select signal is an asynchronous signal. In this case, the IF Sub-System not only counts the power counts for each state of the Counter Select signal, but also counts the time that the Counter Select signal is in each state. The Integration time for each state is now known, hence the total power can be determined. If this input is used, another register in the IF unit has to be set. This register indicates the amount of time to hold off counting on each transition of the Counter Select signal.

1.2 Total Power Detection

The total power detector uses a synchronous detection scheme to measure noise power of the IF signal. A calibrated noise source is coupled into the RF input of the receiver. The signal used to switch this noise source is also input to the IF sub-system (Counter Select).

IF noise power is detected by a Tunnel Diode Detector, and amplified on the Total Power Board (TPB). The amplified DC output drives a voltage to frequency converter, the output of which is fed into a pair of counters on the Xilinx chip in the control board. These counters are enabled by the Counter Select signal.

When Counter Select is Low, frequency output from the TPB increments the Low counter. When Counter Select is High, the High counter is incremented. Since the excess noise power is well known, the difference between the low and high counts allows the IF total power to be determined. The Integration signal is used to reset and load the counter registers, and determines the length of the integration time.

The power range of the System is limited to the range of the Total Power Board, which is -20dBm to -2dBm. The nominal power is -8dBm. The average power level of the signal fed into the samplers is displayed on the VFD and is controlled by a digital attenuator.

2. System Architecture

2.1 Overview

A block diagram of where the IF Sub System fits into the correlator system is shown in figure 1:

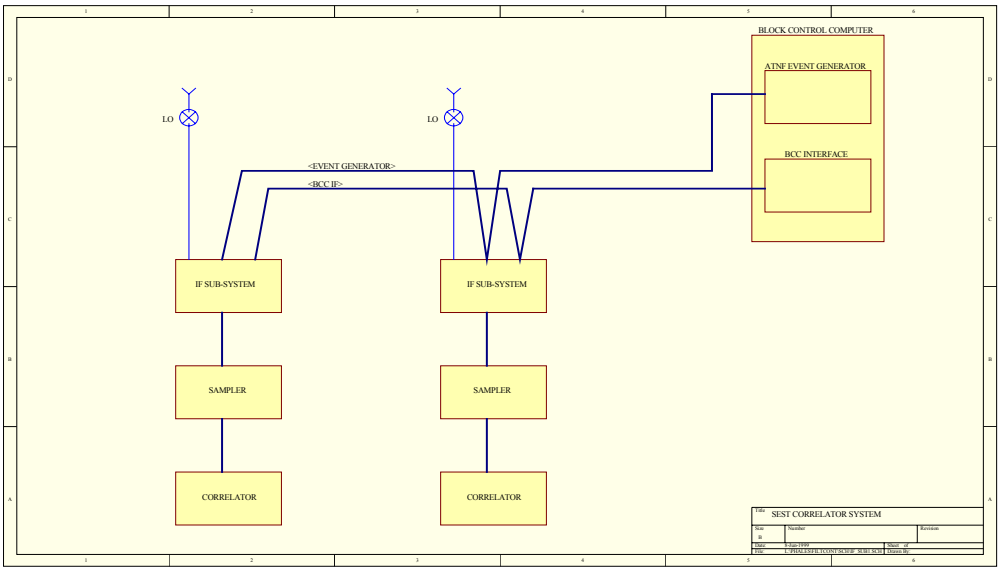


Figure 1: Overview

The If Sub-System is expanded and shown in figure 2.

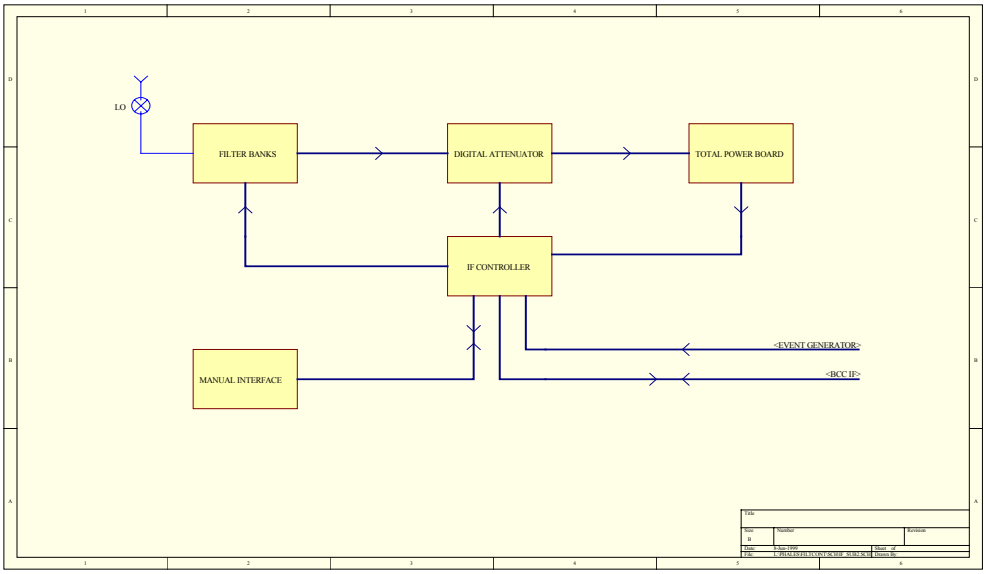


Figure 2: SEST IF Sub-System

2.2 Filter Banks

The filter system is made up of the following components:

- Mini Circuits 2KL-2R7 23dB Amplifiers
- Mini Circuits ZSDR-425 Four Way switches
- Mini Circuits ZSDR-230 Two Way switches
- Mini Circuits ZFSC-2-2500 2 Way Splitter
- Various fixed attenuators
- 2GHz and 1GHz Low Pass Filters

- 512MHz, 256MHz, 128MHz and 64MHz Band Pass Filters

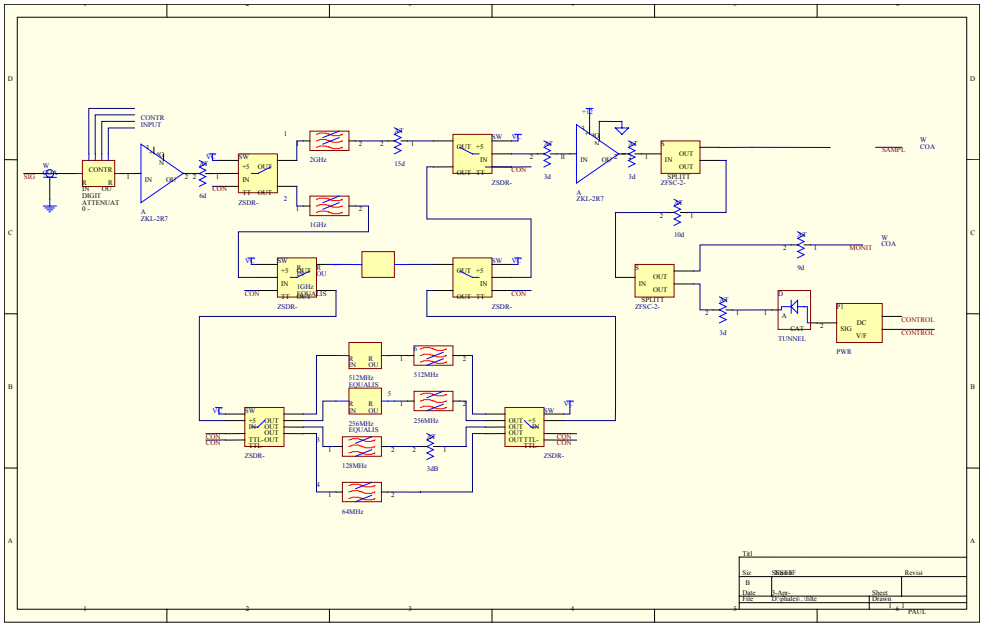


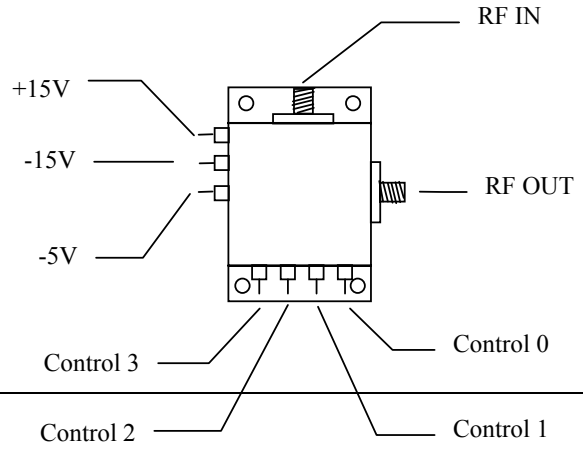
Figure 3: Filter Bank Configuration

It can be seen that by applying the appropriate logic to the switches, any of six Bandwidths can be selected. Figure 3 shows that there are six switches with a total of eight control inputs. Since the switches are mirrored on either side of the filters, we can reduce this to only four control inputs. These logic signals are provided by the IF controller.

	CONT1	CONT2	CONT3	CONT4
2GHz	0	X	X	X
1GHz	1	0	X	X
512MHz	1	1	0	0
256MHz	1	1	0	1
128MHz	1	1	1	0
64MHz	1	1	1	1

0 = Logic Low, 1 = Logic High, X = Don't Care

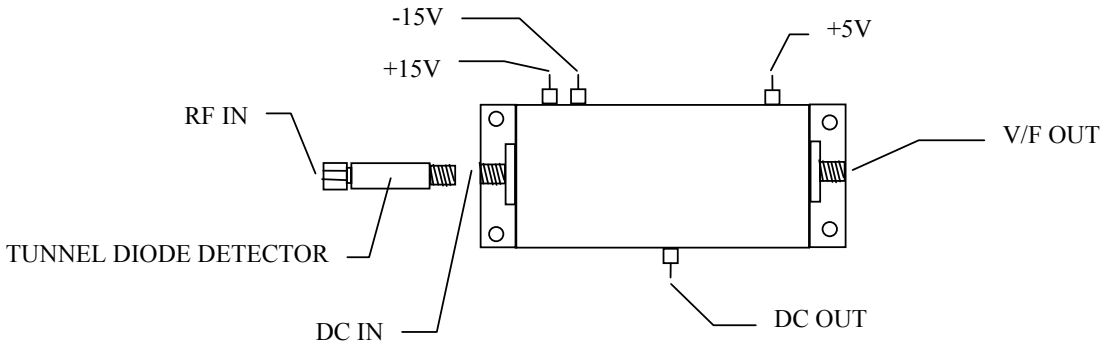
2.3 Digital Attenuator:



The digital Attenuator is M/A-COM AT-210 housed in an RF box along with the necessary control logic. See Appendix A for circuit diagrams and Appendix D for the data sheets. It has a DC to 2GHz range with 0 to 15dB attenuation in 1dB steps. Control is via four binary TTL data lines. The AT-210 requires eight control inputs (4 differential control signals) at 0V for logic low, and -5V for logic high. An ADG333A analog switch is used to convert the TTL inputs to differential 0 and -5V signals.

The Digital Attenuator is used in a control loop to keep the input signal power level going into the samplers at a nominal value of -8dBm. With the 1dB step levels, it is possible to keep the signal within ±0.5dB of the reference. The control signals come from a register in the Xilinx on the IF controller.

2.4 Total Power Board (See Appendix A for circuit diagram)



The TPB includes the tunnel diode detector even though it is not physically part of the board. The detector used is an Advanced Control Components part ACTP-1629NC3, housed in a SMA connector. It provides 1100mV/mW output, which gives us a range of ~0.6mV to 11mV over the operating range of -32dBm to -20dBm. This device has very good linearity with temperature and over the frequency range of DC-2GHz. The signal is fed into the detector from the Digital Attenuator, the DC voltage from the output of the detector is then fed into the input stage of a low noise FET operational amplifier. This amplifier has a gain of around 10 and is followed by a BJT amplifier with a gain of around 27. Both the gains and the offset are adjustable via trimpots. This provides a maximum voltage of 3V which is fed into a Burr-Brown VFC121BP voltage to Frequency converter. The converter is set for a 1MHz output at 3V and is linearly proportional with input voltage below 3V. The Total Power Board is

contained within a RF box which has feed through inputs for ±15V, +5V and a feed through output for the amplified DC voltage signal.

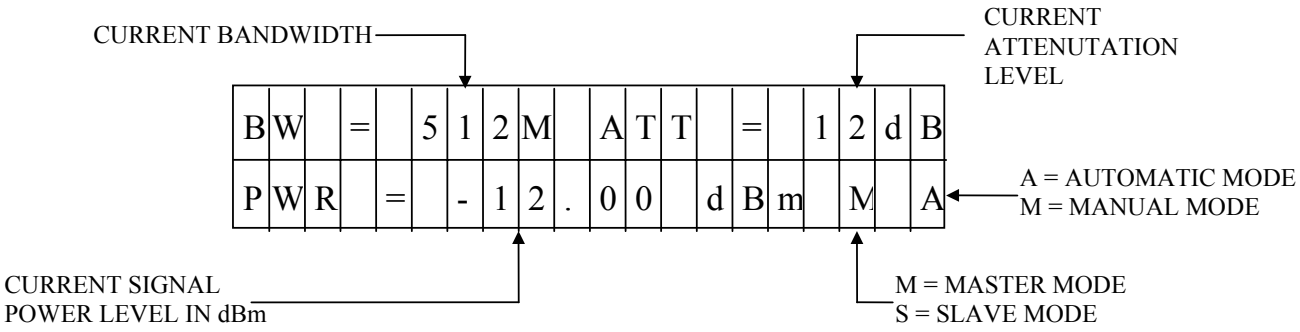
2.5 Manual Interface

Manual mode can be initiated at any time by means of an Automatic/Manual switch. When the mode is changed to manual, the current settings of Bandwidth and Attenuation will remain at the value just before the mode was changed. There are four push button switches provided, two for Attenuation control and Two for Bandwidth control. The Attenuation will increment or decrement (depending on which button is depressed) in 1dB steps. The Bandwidth will step up or down in binary steps from 64MHz to 2GHz.

A two line by 20 character Vacuum Fluorescent Display provides the following information to the user:

- Bandwidth
- Attenuation
- Signal power level at the output to the sampler in dBm
- Current mode

This information is updated from the Xilinx registers every 50ms. Figure 4 shows a diagram of how the information is set out on the display .



2.6 Control Board

The control board comprises of a Xilinx FPGA chip and a DSP. The hardware was designed by Paul Roberts of ATNF for the SEST samplers and has been implemented in the IF SUB-System due to its versatile nature and appropriate features. See Appendix B for the Xilinx schematics and Appendix C for the DSP assembly code.

2.6.1 I/O

Connector	Pin	Description	I/O

Terminal Block	1	VCC +5V	INPUT
Power connections	2	GND	INPUT
	3	VEE -5.2	INPUT

Connector	**Pin**	**Description**	**I/O**
J2 4pin IDC connector	1	TX	OUTPUT
Serial Interface to DSP for	2	TR	INPUT
Debugging	3	DTR	INPUT
	4	GND	INPUT

Connector	**Pin**	**Description**	**I/O**
J4 26pin IDC connector	1	BCC Interface A0	BI-DIR
BCC Interface connection	2	BCC Interface A1	BI-DIR
	3	BCC Interface A2	BI-DIR
	4	BCC Interface A3	BI-DIR
	5	BCC Interface A4	BI-DIR
	6	BCC Interface A5	BI-DIR
	7	BCC Interface A6	BI-DIR
	8	BCC Interface A7	BI-DIR
	9	BCC Interface A8	BI-DIR
	10	BCC Interface A9	BI-DIR
	11	BCC Interface A10	BI-DIR
	12	BCC Interface A11	BI-DIR
	13	BCC Interface A12	BI-DIR
	14	BCC Interface A13	BI-DIR
	15	BCC Interface A14	BI-DIR
	16	BCC Interface A15	BI-DIR
	17	GND	OUTPUT
	18	BCC Interface READ/WRITE	INPUT
	19	GND	OUTPUT
	20	BCC Interface -WAIT	OUTPUT
	21	GND	OUTPUT
	22	BCC Interface -REQUEST	INPUT
	23	GND	OUTPUT
	24	-STROBE	INPUT
	25	GND	OUTPUT
	26	NOT CONNECTED	

Connector	**Pin**	**Description**	**I/O**
J6 14 pin IDC connector	1	GND	OUTPUT
FRONT DISPLAY	2	VCC	OUTPUT
	3	NOT CONNECTED	
	4	DISPLAY REGISTER SELECT	OUTPUT
	5	DISPLAY READ/WRITE	OUTPUT
	6	DISPLAY ENABLE	OUTPUT
	7	DISPLAY DATA D0	BI-DIR
	8	DISPLAY DATA D1	BI-DIR
	9	DISPLAY DATA D2	BI-DIR
	10	DISPLAY DATA D3	BI-DIR
	11	DISPLAY DATA D4	BI-DIR
	12	DISPLAY DATA D5	BI-DIR
	13	DISPLAY DATA D6	BI-DIR

	14	DISPLAY DATA D7	BI-DIR

Connector	**Pin**	**Description**	**I/O**
J3 26pin IDC connector	1	GND	OUTPUT
EXPANSION PORT	2	VCC	OUTPUT
Power Count signals and	3	BLANK SIGNAL	INPUT
Manual interface connections	4	SYNC SIGNAL	INPUT
	5	POWER LEVEL FREQUENCY	INPUT
	6	AUTO/MANUAL CONTROL	INPUT
	7	BANDWIDTH DWN SET	INPUT
	8	BANDWIDTH DWN CLEAR	INPUT
	9	BANDWIDTH UP SET	INPUT
	10	BANDWIDTH UP CLEAR	INPUT
	11	ATTENUATION UP SET	INPUT
	12	ATTENUATION UP CLEAR	INPUT
	13	ATTENJUATION DWN SET	INPUT
	14	ATTENUATION DWN CLEAR	INPUT
	15 to 26	NOT CONNECTED	

Connector	**Pin**	**Description**	**I/O**
J8 26pin D connector	1	BANDWIDTH D0	OUTPUT
Bandwidth and Attenuation	2	BANDWIDTH D1	OUTPUT
outputs	3	BANDWIDTH D2	OUTPUT
	4	BANDWIDTH D3	OUTPUT
	5	ATTENUATION D0	OUTPUT
	6	ATTENUATION D1	OUTPUT
	7	ATTENUATION D2	OUTPUT
	8	ATTENUATION D3	OUTPUT
	9 TO 26	NOT CONNECTED	

2.6.2 Xilinx FPGA

The function of the Xilinx chip is to create the registers that are required by the DSP and the External control computer. It provides a buffer between the input commands to the IF controller and the output signals to the filter switches and Digital Attenuator.

The functions of the Xilinx can be broken down into seven main blocks. A brief description of each block along with the associated schematic files are given below:

- TARGET.SCH
  This file contains the circuitry for interfacing with the BCC Interface card. The address from the BCC Interface is buffered and stored in a register. The 8 MSB's are then compared to the IF Controller's DIP switch address to check if the controller is being addressed. The WAIT and WAIT ENABLE signals are created here in accordance with the BCC Interface protocol. A one bit register is also created for Mode control.

- DECODE.SCH

A register for the bandwidth/attenuation settings from the BCC Interface is created. From this register, the Bandwidth setting is decoded and output to the filter switches. The Auto/Manual register is created and used to control the output of either the manual or automatic setting of bandwidth to the output switches. The input stage for the manual Bandwidth push button switches and a up/down counter is implemented.

- ATDECODE.SCH
  An input stage for the manual Attenuation push button switches and a up/down counter is implemented. Control between Manual setting, BCC setting or DSP setting of attenuation output is also implemented in this file.

- VF_COUNT.SCH
  An eight bit and a 16 bit counter are used to form the 24 bit counter for counting the frequency signal from the TPB. Two of these counters are created along with the registers used to lock the count in after the integration period. The Xilinx interrupt to the DSP chip is created here.

- VFD.SCH
  The circuitry required by the display device and the data input from the DSP chip is created in this file. The ready signal to insert wait states into the read/write from the DSP is also created.

- OUTPUT1.SCH, OUTPUT2.SCH and OUTPUT3.SCH
  These three files contain the logic necessary to feed all the different register outputs to the BCC Interface Bus data bus and the DSP data bus.

2.6.2.1 Register Memory Map

The following is a list of the registers addressable by the BCC Interface
Source can be either the Sync signal or the Paddle.

Address	**Description**	**Read/Write**
Base	IF Configuration	R/W
Base + 0x1	Power count, Source Low 16 LSB	R
Base + 0x2	Power count, Source Low 8 MSB	R
Base + 0x3	Power count, Source High 16 LSB	R
Base + 0x4	Power count, Source High 8 MSB	R
Base + 0x5	Accumulation Time Source low 16 LSB	R
Base + 0x6	Accumulation Time Source low 8 MSB	R
Base + 0x7	Accumulation Time Source High 16 LSB	R
Base + 0x8	Accumulation Time Source High 8 MSB	R
Base + 0x9	Hold Time 16 LSB	R/W
Base + 0xa	Hold Time 8 MSB	R/W
Base + 0xb	Integration Time	R/W

The following is a list of the registers which are addressable by the DSP on the IF controller.

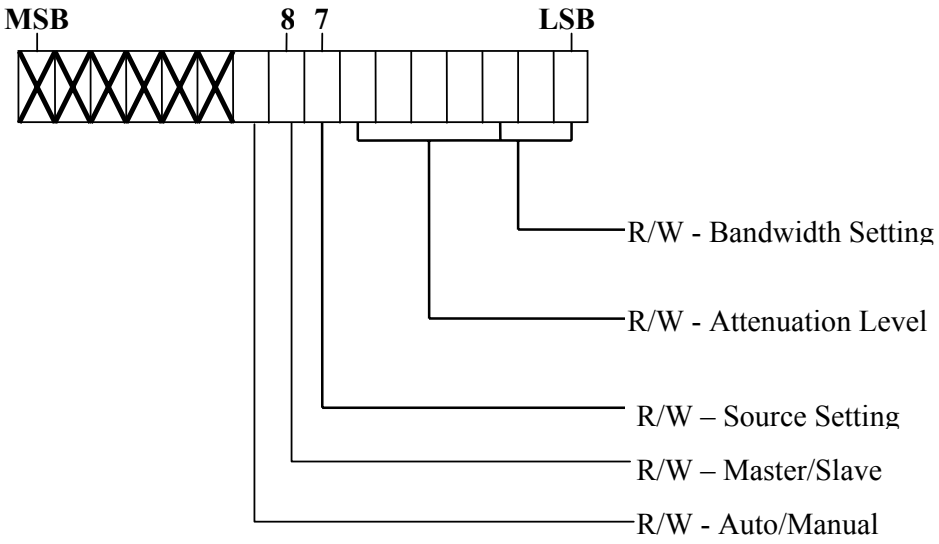
Address	Description	Read/Write
Base + 0x8	Attenuation setting	W
Base + 0x9	IF mode register	R
Base + 0xa	Display register	R/W
Base + 0xb	Power count, Sync OFF	R
Base + 0xc	Power count, Sync ON	R
Base + 0xd	IF configuration	R
Base + 0xe	Integration time	R
Base + 0xf	DSP generated BLANK signal	W

2.6.2.2 Register Descriptions

2.6.2.2.1 BCC Controller Registers

The following register descriptions are for the registers addressable by the BCC. The base address is set by 8 DIP switches on the IF controller board.

2.6.2.2.1.1 IF Controller Register 0 (Offset 0x0)



Bandwidth Setting : When writing, these three bits select the bandwidth setting for Slave Automatic Mode (SAM):

000 - 2 GHz
001 - 1 GHz
010 - 512 MHz
011 - 256 MHz
100 - 128 MHz
101 - 64 MHz
110 - 64 MHz
111 - 64 MHz

The setting is decoded by the Xilinx logic and is output to the filter switches. If another Mode is selected, the setting will be stored in this register and will be implemented when the mode is changed back to SAM.

When Reading, these three bits contain the current bandwidth setting independent of the mode.

Attenuation Level: When writing, these four bits contain the attenuation level for SAM.

0000 - 0 dB
0001 - 1 dB
.
.
1111 - 15 dB

This level is output to the digital attenuator control inputs.

When Reading, these four bits contain the current attenuation level, independent if the mode.

Source Setting This bit tells the IF unit the source of the count enables for the high and low power counters.

0 – Indicates that the counter enables are driven by a Sync signal from the Event Generator.
1- Indicates that an external signal is being used to select the counters.

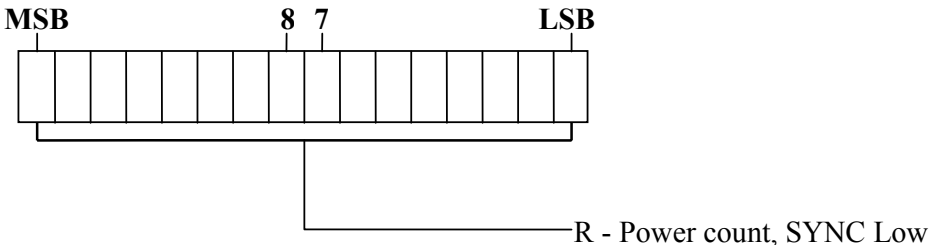
Auto/Manual This register is set if the IF controller is in Automatic Mode, and is clear if the IF controller is in Manual Mode. Automatic or Manual mode is controlled by an external switch on the Manual Interface or by setting/clearing this bit. The current mode is also displayed on the VFD.

Master/Slave: This bit sets the IF controller in either Master Mode or Slave Mode. In Master Mode, the IF controller implements its own control loop to keep the signal power at -8dBm. The IF controller will vary the attenuation level of the digital attenuator based on the calculated power level with a 5 second integration time. The IF controller will produce its own BLANK signal to control the integration timing. In Slave Mode, the BCC is responsible for setting the integration time and controlling the attenuation level. In this case, the IF controller is passive, only displaying the settings and power level.

0 - Master Mode (Default on power up)
1 - Slave Mode

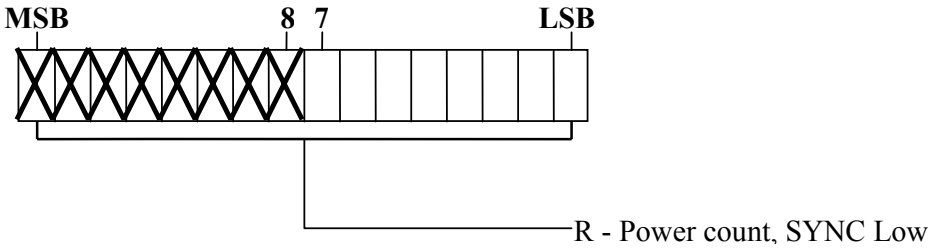
NOTE: Automatic/Manual Mode can be changed at any time by an external switch. If this occurs, Master/Slave mode will be irrelevant, as all control will be via the Manual Interface. When the mode is changed back to Automatic, the Master/Slave bit will determine who has control and what settings to load into the bandwidth and attenuation outputs. The Master/Slave bit can be changed at anytime, even during Manual control.

2.6.2.2.1.2 IF controller register 1 (offset 0x1)



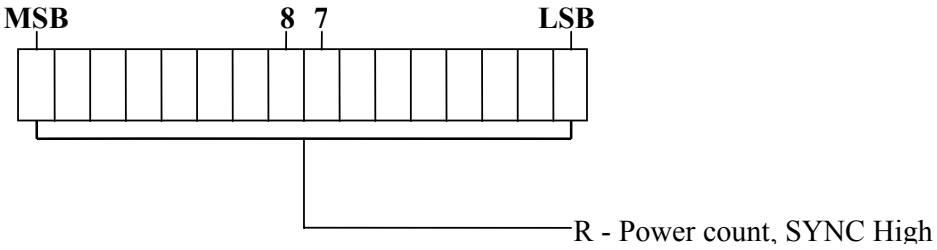
Power Count, SYNC LOW: 16 LSB This is a read only register which holds the value of the power count for the time that the SYNC signal was Low during the previous integration period. This is a 16 bit register which holds the bits 0 to 15 of a 24 bit counter
The count registers are loaded just before the counters are cleared after receipt of a BLANK signal. The BCC can then read the values from these registers at any time until the next BLANK signal occurs.

2.6.2.2.1.3 IF controller register 2 (offset 0x2)



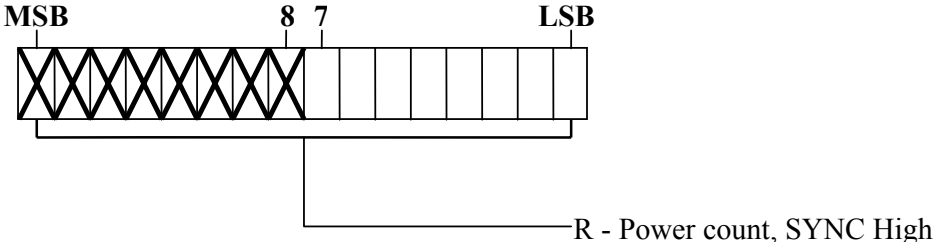
Power Count, SYNC LOW: 8 MSB This is a read only register which holds the value of the power count for the time that the SYNC signal was Low during the previous integration period. This is a 16 bit register which holds the bits 16 to 23 of a 24 bit counter. The counter can count to a maximum of 167772176 counts. With a 1MHz input frequency (Maximum power), the integration time can be as large as 16.7s.

2.6.2.2.1.4 IF Controller Register 3 (offset 0x3)



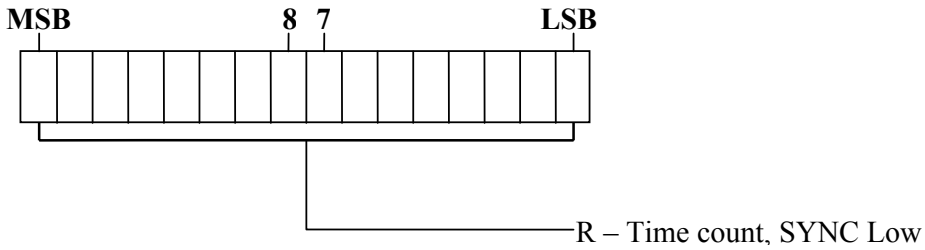
Power Count, SYNC High 16 LSB This is the same as register 1, except that the register holds the count for the time when the SYNC signal was High during the previous integration period.

2.6.2.2.1.5 IF Controller Register 4 (offset 0x4)



Power Count, SYNC High 8 MSB This is the same as register 2, except that the register holds the count for the time when the SYNC signal was High during the previous integration period.

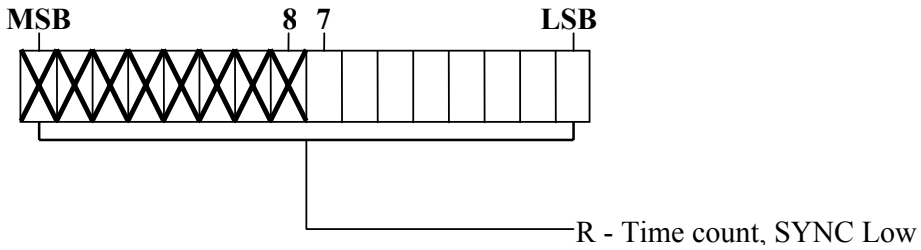
2.6.2.2.1.6 IF controller register 5 (offset 0x5)



Time Count, SYNC LOW: 16 LSB This is a read only register which holds the value of the Time count for the time that the SYNC signal was

Low during the previous integration period. This is a 16 bit register which holds the bits 0 to 15 of a 24 bit counter
The Time counter is used when the source is switched to external. The counter holds the accumulated time in micro seconds, for when the low power counter was enabled.

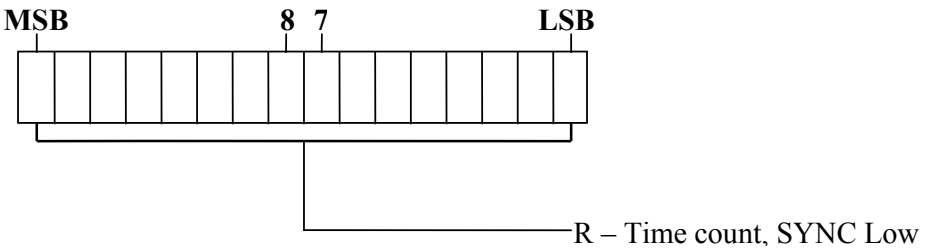
2.6.2.2.1.7 IF controller register 6 (offset 0x6)



Time Count, SYNC LOW: 8 LSB

This is a read only register which holds the value of the Time count for the time that the SYNC signal was Low during the previous integration period. This is a 16 bit register which holds the bits 16 to 23 of a 24 bit counter
The Time counter is used when the source is switched to external. The counter holds the accumulated time in micro seconds, for when the low power counter was enabled.

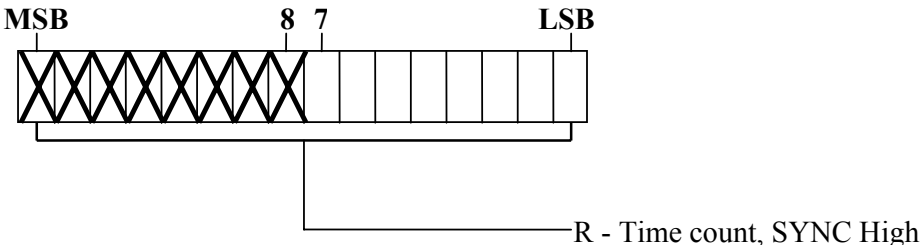
2.6.2.2.1.8 IF Controller Register 7 (offset 0x7)



Time Count, SYNC High 16 LSB

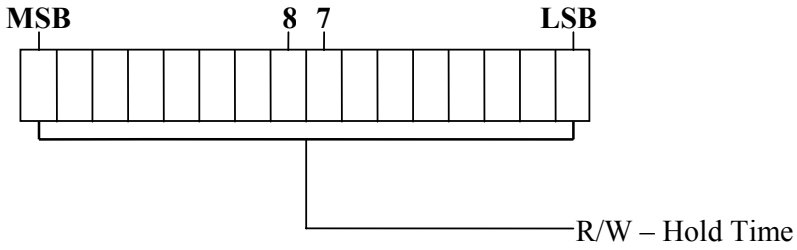
This is the same as register 5, except that the register holds the count for the time when the SYNC signal was High during the previous integration period.

2.6.2.2.1.9 IF Controller Register 8 (offset 0x8)



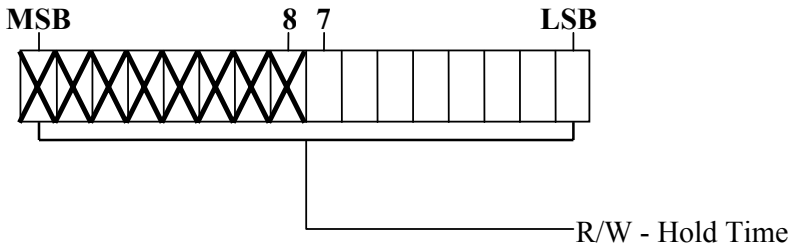
Time Count, SYNC High 8 MSB This is the same as register 6, except that the register holds the count for the time when the SYNC signal was High during the previous integration period.

2.6.2.2.1.10 IF Control Register 9 (offset 0x)



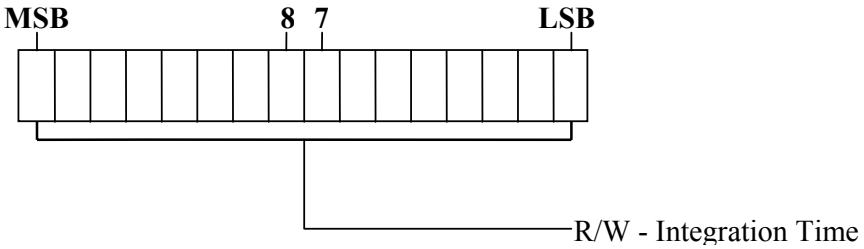
Hold Time 16 LSB: This 16 bit register contains the 16 LSB of the 24 bit hold time. The hold time is the amount of time in micro seconds, that the counters are held off from counting. The hold time is active after every transition of the external counter enable signal.

2.6.2.2.1.11 IF Control Register 10 (offset 10x)



Hold Time 8 MSB: This 16 bit register contains the 8 MSB of the 24 bit hold time. The hold time is the amount of time in micro seconds, that the counters are held off from counting. The hold time is active after every transition of the external counter enable signal.

2.6.2.2.1.12 IF Control Register 11 (offset 0x11)

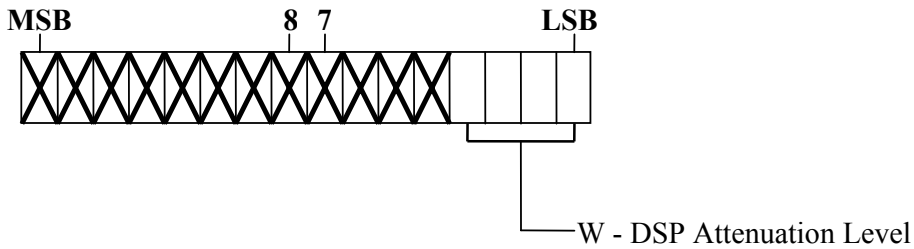


Integration Time: This 16 bit register holds the value of the integration time in milliseconds. It is used by the IF controller DSP to calculate the power level for display. The BCC will set this register during the initialisation phase. To set the integration time to 5 seconds, the BCC would load this register with 5000 ie 0x1388

2.6.2.2.2 DSP Controller Registers

The following register descriptions are for the registers in the Xilinx used by the DSP. The base address is set by the onboard address decoder to 0x2000

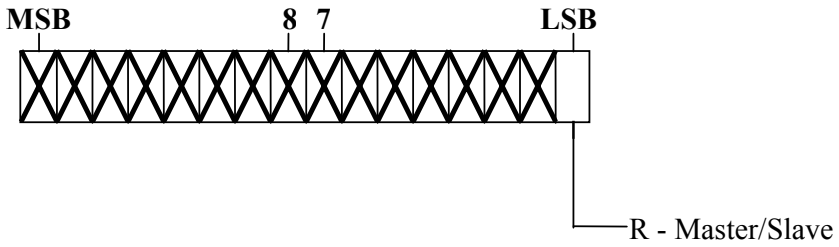
2.6.2.2.2.1 DSP IF Controller Register 0 (Offset 8)



DSP Attenuation Level: These four bits hold the value of the attenuation level as set by the DSP. This value is used in Master Automatic Mode (MAM) to control the attenuation level. The DSP will write to this register when the IF

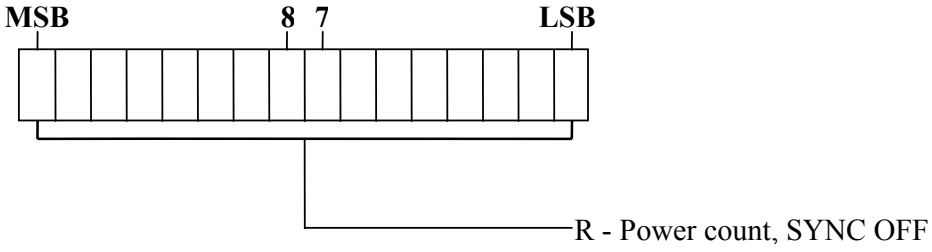
controller is in other Modes, but the value will only be output to the Digital Attenuator when the mode is changed to MAM.

2.6.2.2.2.2 DSP IF Controller Register 1 (Offset 0xb)



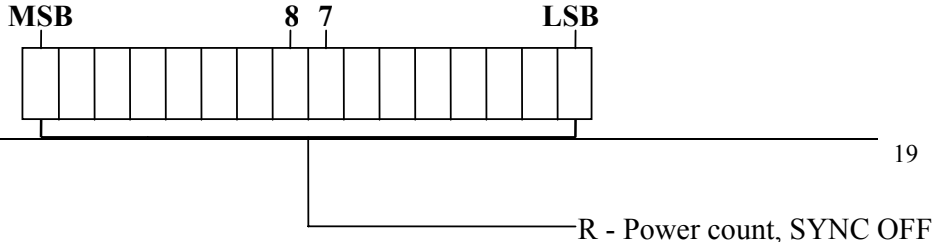
Master/Slave: This bit is read by the DSP to determine which mode is currently active. The results of a read from this register are used to display the current mode on the VFD. The display is updated every 50ms

2.6.2.2.2.3 DSP IF Controller Register 2 (Offset 0xb)



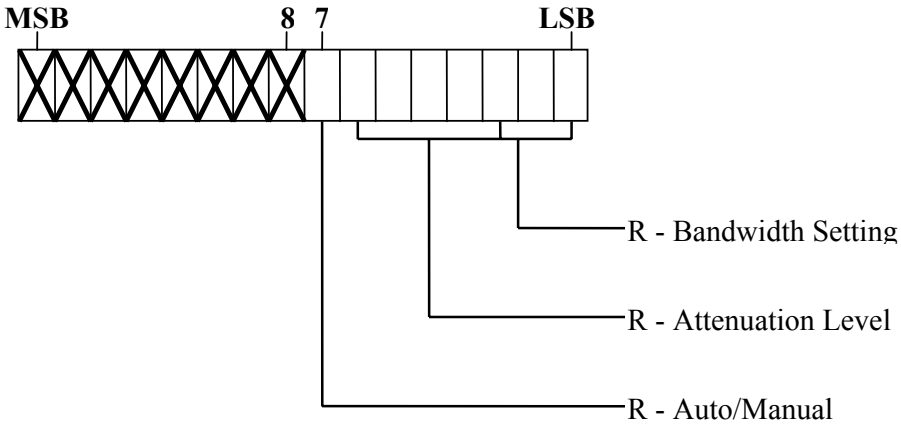
Power count, SYNC OFF: This register provides the same function as IF controller register. However, this register is used by the DSP to read the count obtained during the previous integration period. The contents of this and DSP IF Control Register 3, are added together and used to obtain a value of the average power of the IF signal sent to the samplers.

2.6.2.2.2.4 DSP IF Controller Register 3 (Offset 0xc)



Power count, SYNC OFF: This register performs the same function as IF Control Register 2. However, this register is used by the DSP to read the count obtained during the previous integration period The contents of this and DSP IF Control Register 3, are added together and used to obtain a value of the average power of the IF signal sent to the samplers.

2.6.2.2.2.5 DSP IF Controller Register 4 (Offset 0xd)

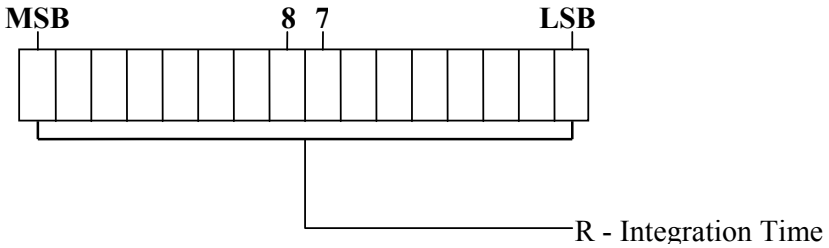


Bandwidth: The DSP reads the current Bandwidth setting every 50ms for display on the VFD.

Attenuation Level: The DSP uses the current attenuation level in its control loop calculations. This value is also displayed on the VFD.

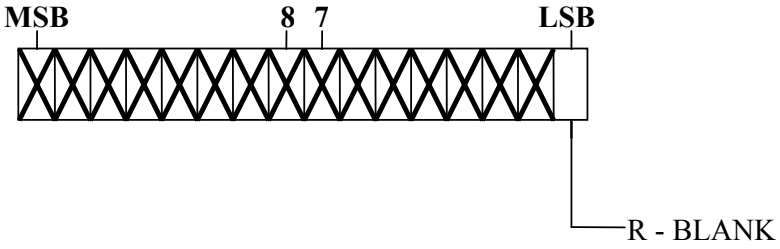
Auto/Manual: Auto/Manual setting is read and displayed every 50ms

2.6.2.2.2.6 DSP IF Controller Register 5 (Offset 0xe)



Integration Time: The Integration time as set by the BCC, is used by the DSP to calculate the power level.

2.6.2.2.2.7 DSP IF Controller Register 6 (Offset 0xf)



BLANK: This is the signal sent to the Xilinx logic to simulate a BLANK signal during Master Automatic Mode. Integration begins when a logic high is sent to this address and ends when a logic low is sent. The counter registers are read and the counters cleared as with a real BLANK signal.

2.6.3 DSP

The DSP program is written in assembly language and included in appendix C. The program is interrupt driven by two interrupts. One is internally generated by a timer every 50ms. This is used to update the display device with the latest information as read by the Xilinx registers and to increase a timer variable buy one. The second interrupt is generated by the Xilinx chip whenever the blank signal goes low. This indicates that the current integration period has concluded and the data in the counters is valid and can be read. During normal operation (after initialisation), the program will sit in one of two loops.

If the current Mode (as set by the BCC) is Master Mode, then the DSP is in control of the power setting and hence has to implement a control loop. A DSP-BLANK signal will be sent to the Xilinx to start the integration period. The program will then loop until the timer variable indicates that 5 seconds is up. The BLANK signal is removed which will cause the Xilinx to store the count, clear the counters and generate an interrupt. When the interrupt is received by the DSP, an interrupt service routine is executed and the power level is read, converted to log and output to the display device. The control loop is also executed and the attenuation level of the Digital Attenuator is adjusted if necessary, so that the power level is kept at -8dBm. The program will then output the BLANK signal again and wait in its loop for the next five second period to conclude.

If the current Mode is Slave Mode, then the DSP will sit in a loop waiting for a Xilinx interrupt to occur. When this happens, the interrupt service routine is executed as above, except this time the control loop is not executed. The program then returns to its loop awaiting the next interrupt

2.6.4 BCC Communications

The protocol used for communication between the IF controller and the BCC Interface is the same as that described in the document BCC Interface MKII. This document is placed in Appendix E.

2.6.5 Jumper links

There are three jumper links on the control board. Only one of these has any effect on the IF controller.

Link	**State**	**Function**
XMODE LK1	OPEN	Xilinx Configuration Mode - Serial Slave. Used to download Xilinx design via an external computer and a download cable.
	CLOSED	Xilinx Configuration Mode - Serial Master. Xilinx prom must be installed.