EVN Doc 2

PROPOSAL
for a
MULTIBAND & MULTITONE PHASE CALIBRATION SIGNAL EXTRACTOR
for the EVN Upgrade Project

Sergei V. Pogrebenko

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1. GENERAL WORDS

1.1. Main Idea

The main idea of the proposed Extractor is to capture the calibration pulses in their entirety. Each pulse is composed of all calibration tone harmonics in the band analyzed.

Then, by means of spectral decomposition of the captured pulse, the required information on phases and amplitudes of the calibration harmonics may be obtained.

1.2. Signal Structure

As shown in Fig.1.1, the calibration signal structure looks like a periodic pulse sequence with period P = 1 microsec, if bandwidth is broad enough to have three or more harmonics with 1 MHz separation.
When the bandwidth is less than 2 MHz, it will look like simple sine wave.

In fact, this periodic pulse sequence is modulated with a frequency, equal to the frequency offset between the sum of the heterodyne frequencies and the frequency of the nearest calibration harmonic.
So the spectral components of pulses will be shifted by this offset, as it is shown in Fig.1.2 and 1.3.

The way to remove this frequency offset is traditional - one applier the proper reference signal to the signal analysed, as it is done in a crosscorrelator. But the small frequency offset (of the order of 0.1 Hz) is needed to be unremoved for spectral analysis convenience.

After the frequency offset is removed, we will have a periodic, slowly rotated pulse sequence.

1.3. Pulse Capturing

The next step is the linear accumulation of this periodic signal, the process resembling folding procedure of pulsar analysis.
But in our case we need to "fold" voltage rather than power. This is possible, because we will store voltages in phase.

Many solutions for such periodic pulse sequence folding may be proposed, but the obvious one is to use correlator for this purpose.

A block diagram of this solution is presented in Fig.2.
Signal X is pumped into input X of the crosscorrelator with clock rate CLK.
Than it rotates with reference signal to remove offset, wile the Y signal is kept in "1" to make the multipliers transparent.
But the multipliers are blocked by the Validity signal, which is kept in "0" all the time, exept once per 1 microsec. When Validity is set to "1", it opens the multipliers, and the bitpattern of X, situated at this moment in the shift register, falls down into accumulators and adds to the previous content. Then the Validity needs to be set to "0" again to store the next 1 microsec cycle in the shift register.

The interval of 1 microsec is the basic one, because it is the period of pulses sequence. When N*1 microsec period is used, the result will be better. But in this case we need the shift register in the correlator to be of proper length.

Thus the signal voltage is stored in accumulators of the correlator. The length of this linear accumulation depends on the rest frequency offset we do not remove from the input signal. In practice the capacity of the correlator accumulators is not enough to store the signal longer than tens of milliseconds. So additional accumulation needs to be done in a microcomputer.

The subsequent correlator readouts will form an array, looking like the one presented in Fig.3.1.

If an FFT along the correlator lags is applied to each line of this array, we obtain the data set shown in Fig.3.2.
Stored in the time domain pulse structure transforms into a spectral structure. And if we have enough data points in the time domain (enough correlator lags) - the spectral components of the calibration pulse will be resolved.

Then an FFT along the time axis of the correlator readout needs to be applied to do the final accumulation.
The rest frequency offset is determined at this step, and the final result of storage of spectral structure of signal, including Phase and Amplitude data of each harmonic will look like those, presented in Fig.3.3.

So, complete information about all phase calibration harmonics in the analysed videoband is obtained simultaneously, not sequentially as with traditional solution for the tone extraction.

The prosedure proposed gives the same SNR as Haystack/VLBA solution, but in shorter time.

2. IMPLEMENTATION

2.1. Hardware Solution

The best way to implement the procedure proposed is to use the Haystack designed Correlator Chip (HCC).

HCC may be configured as a block of 8 independent complex crosscorrelators with 32 lags in each sine and cosine sections.

Eight independent correlators in one HCC give us the possibility to analyse 8 basebands simultaneously and independently.
To analyse 16 basebands simple multiplexing logic needs to be added.
In this case 16 basebands will be analysed in two steps.
Also two HCC working in parallel may do this task in one step.
A cross-point switch may be used to make the configuration flexible:
to connect each chosen HCC input to the each chosen baseband.

32 complex lags in each correlator is just enough to resolve all 16 spectral components in the case of 16 MHz bandwidth.
If bandwidth is less then 16 MHz, smaller number of lags may be analysed, or a slower correlator readout take place.

The block diagram of the hardware solution using one HCC with input multiplexer is shown in Fig.3.1. The simplest way of pulse bitpattern capturing is to mix "1" once per 32 clocks with the Validity signal. For this purpose simple 5-bit counter needed. In general case this counter may be programmable.

A module of two HCCs in parallel (Fig.3.2) with Cross-point multiplexer provide universal solution for a 16 basebands parallel multitone analyser.
The cross-point MX and programmable counter are implemented in one Xilinx chip.

2.2. Secondary Processing

In case of 1/32 counter the accumulators of the HCC will store bitpattern only once per 32 clocks, so the accumulation rate is 32 times smaller, than in the case of the crosscorrelation prosedure, e.g. the accumulation rate of the correlator is 32 times less, and a life of the microcomputer slaving it is easy.

Spectral analysis of the correlator readout is also not a hard work for the microcomputer. Secondary processing computational power requirements (in the case of 10 seconds accumulation interval) are about 8*16 of 32-points FFT and 8*16 of 16-points FFT per 10 seconds (about 500 000 operations per 10 seconds).

2.3. Layout

The small size of the hardware block (one or two HCC and one Xilinx PLD) makes it possible to mount it on the same board with the Delay Control Unit.

The crate-controller computer may be used for secondary processing.

3. PERFORMANCE COMPARISON WITH HAYSTACK/VLBA PCAL EXTRACTOR BOARD

ITEM	Haystack PCal Extractor Board (VLBA Acq Memos #248,249)	Two HCC Based Multiband & Multitone Phase Cal Extractor
3.1. Max. frequency offset of tones extracted	16 MHz	16 MHz
3.2. Frequency adjustment step	10 KHz	15 mHz at B= 2 MHz 130 mHz at B=16 MHz
3.3. Number of basebands, processed simultaneously	4 with 4-bit sine table 8 with 2-bit sine table 16 with 1-bit sine table	16 with 2-bit sine table
3.4.Number of calibration tones, extracted simultaneously	exchange of bb-number with tone-number with the limit of bb-num*ton-num=16	
a) per baseband		up to 16
b) per unit		up to 256
3.5. Time, needed for complete processing of 16 basebands		
at 2 MHz bandwidth	1	1/2
at 4 MHz bandwidth	1	1/4
at 8 MHz bandwidth	1	1/8
at 16 MHz bandwidth	1	1/16
3.6. Hardware volume	1 VME board (with the A/D Unit)	2 HCChip + 1 Xilinx (on the Delay Unit)

4. ADVANTAGES

4.1. Reducing the time needed to obtain complete phase tone information

It makes avalable more reliable (refered to the same time point) phase data. Also this information will be obtained more quickly, thus compensation of short-period phase fluctuations may be possible.

Increase of sensitivity and accuracy is also possible.
Increase of sensitivity should allow solution of the problem of a confusion of real tones with the images and so to make the data more reliable.

4.2. Smaller Hardware Volume

4.3. Another Application

Capturing of any periodic Spread-Spectrum Signals, like used in Planetary Missions Positioning (NASA-JPL/USA and IKI-Space_Devices/Russia).

5. COST ESTIMATION AND COMPARISON WITH HAYSTACK/VLBA BOARD

Components required	Number required	Approx. Board Area (Sq.Inch)	Cost of components
HCChip	2	6	$ 600
Xilinx	1	3	$ 275
TOTAL	3	9	$ 875
VLBA TOTAL(using LSI)	43	54	$ 1145
(using VLSI)	13	38	$ 1470
			plus frame, connector, wiring
(VLBA Acq.MEMO#249)			Total replication cost $ 3 500 per A/D+PCal Board

The solution proposed gives about $ 1000 savings per Unit

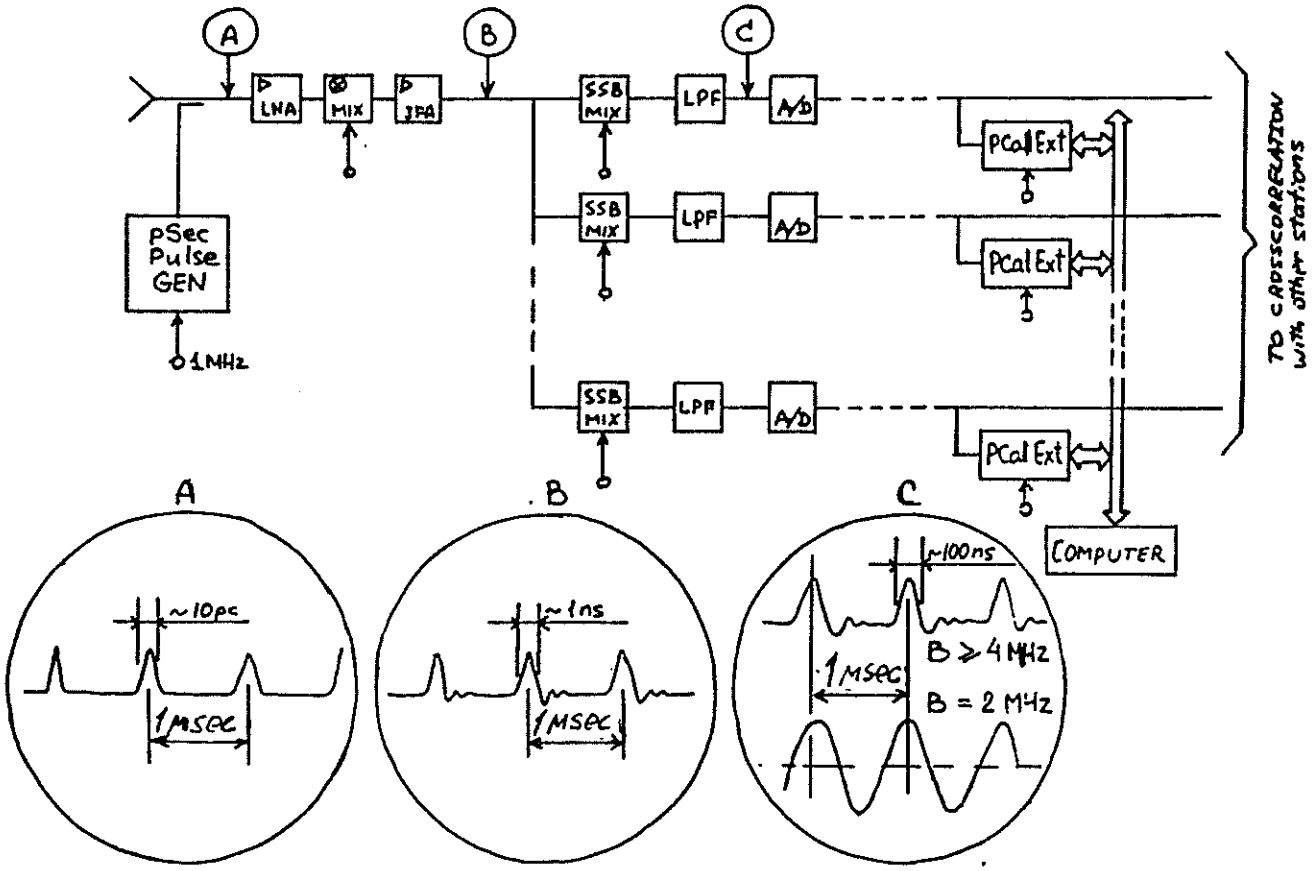

Fig.1.1. How PhCal Signals Look Like in the Time Domain at Different Points of a System.

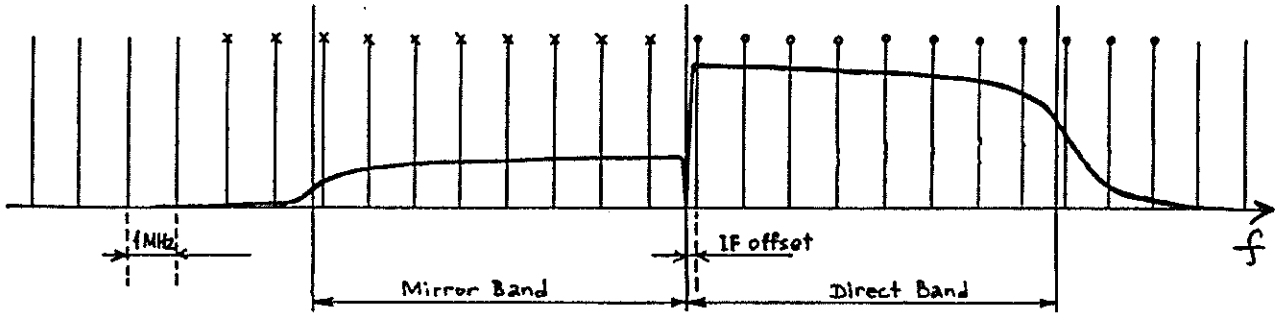

Fig.1.2. PhCal Signal Spectral Structure at the Front-End Frequency

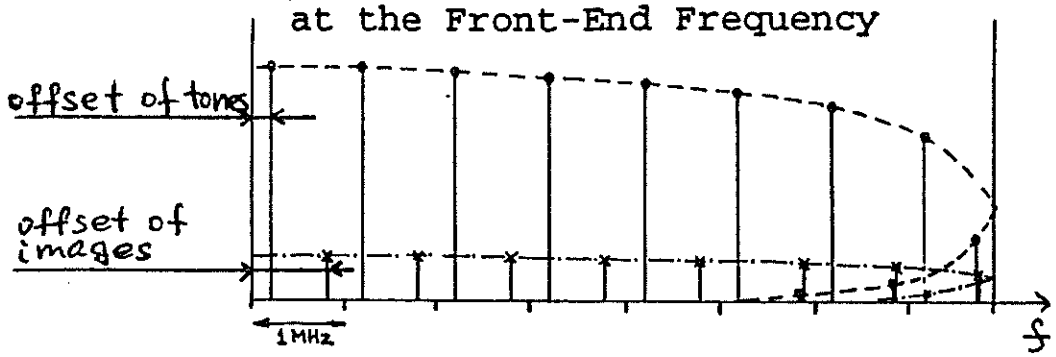

Fig.1.3. PhCal Signal Spectral Structure at the Videoband.

Fig.1. How PhCal Signals Look Like.

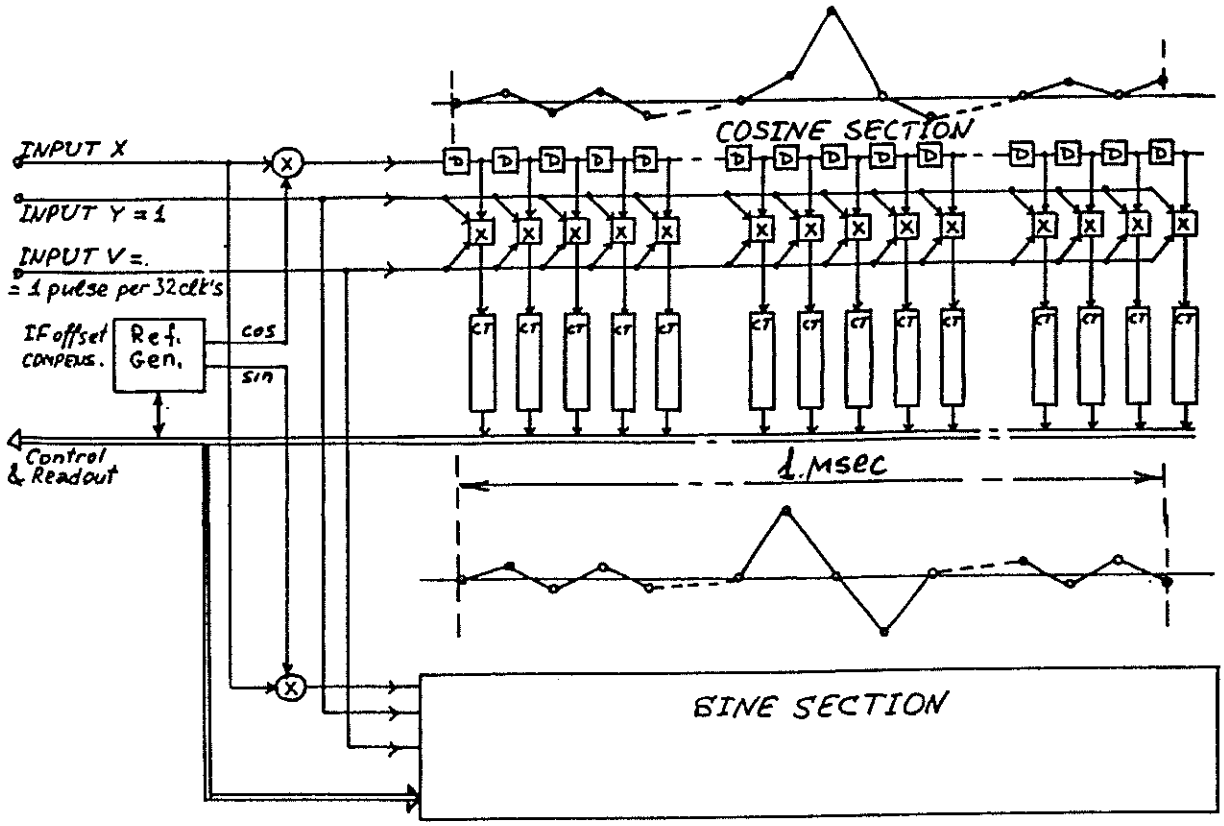

Fig.2. Stroboscopic Folding
and Accumulation of Pulses in the Correlator.

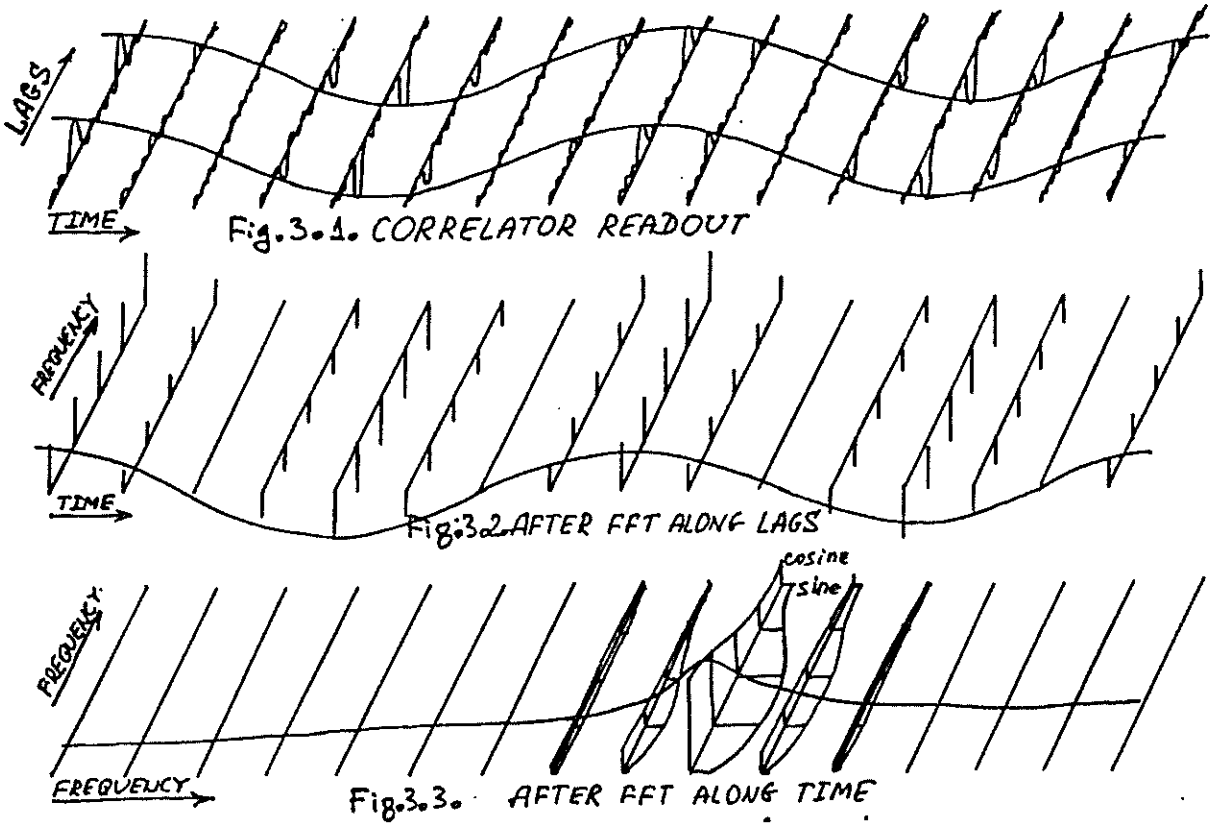

Fig.3. Correlator Readout Data
at Different Steps of Data Reduction.

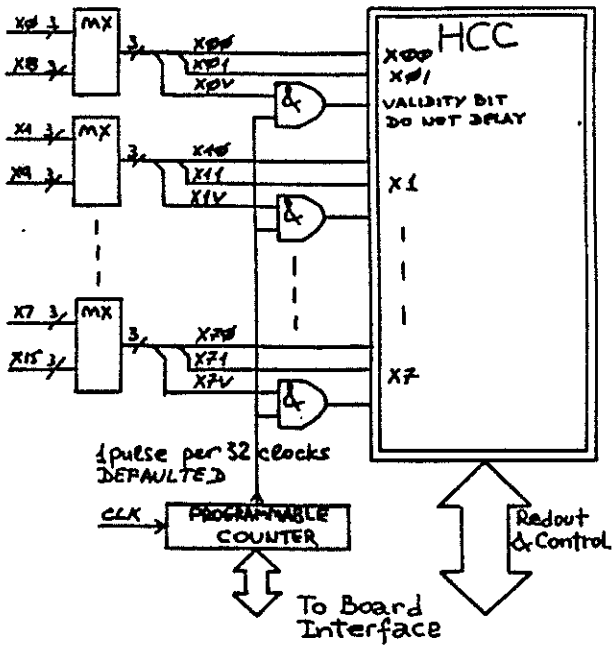

Fig.4.1.

Simplest Solution: 8-Bands 1-HCC Extractor with Multiplexer for 16 Bands analysis.

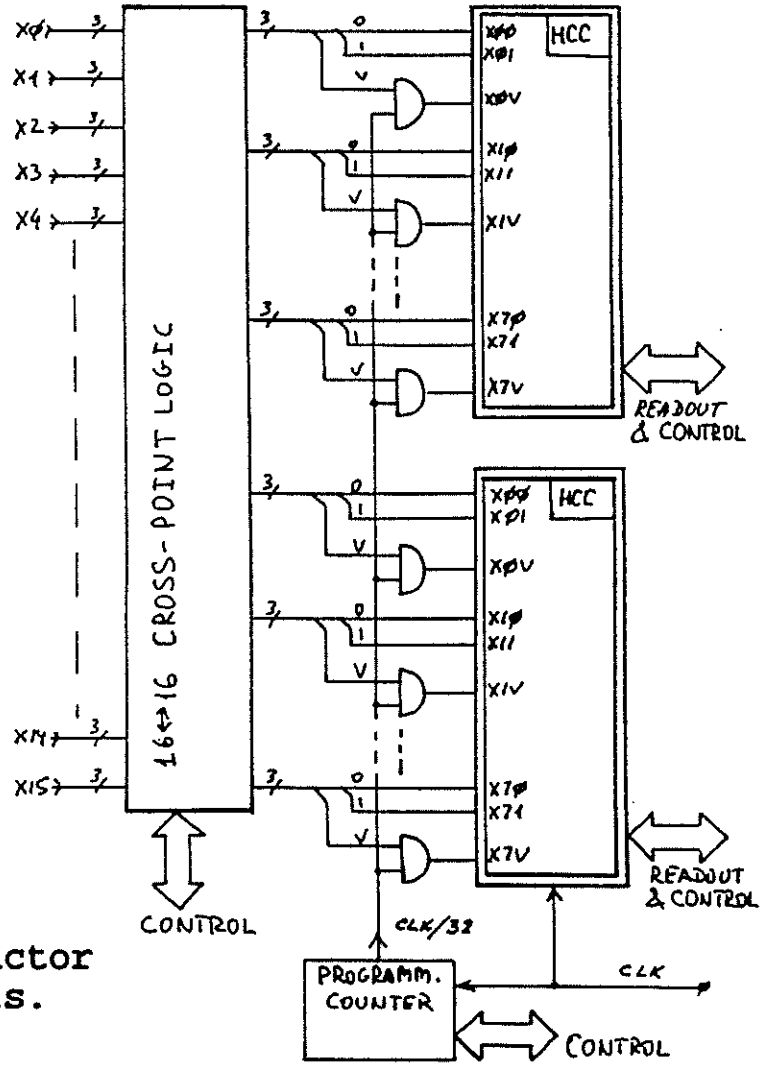

Fig.4.2. Two HCC-Based 16 Bands Extractor Block Diagram

Fig.4. HCC Based Multiband & Multiton PhCal Extractors Block Diagrams.